Sajad Eydivandi

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Research Interests

AI Accelerators, Low-power System Design, Computer Architecture, Internet of Things, Sensor networks

Education

2022 – Present **Iran University of Science and Technology (IUST)** – Tehran, Iran
M.Sc in Computer Engineering (Computer Architecture)
Mentor: Professor Hakem Beitollahi. *GPA: 18.05.*

2016 – 2021 **Isfahan University of Technology(IUT)** – Isfahan, Iran
BA in Electrical Engineering (Electronics)
Mentor: Professor Amir Khorsandi *GPA: 15.99.*

Honors and Scholarships

2022 Qualified to study in Iran University of Science and Technology after taking National Entrance Exam of the public universities of Iran for higher educations in computer engineering in 2022.

2016 Ranked 882 among 162879 participants in the National Entrance Exam of the public universities of Iran (Konkour), Iran, 2016.

Publications

2025 **Fair Benchmarking and Design Insights for FPGA-Based CNN Accelerators**
Sajad Eydivandi, Hakem Beitollahi.
Journal of something or the other.

2025 **SARPAR: Systolic ARray Pallet-Integrated AcceleratoR for YOLO Models on FPGA**
Sajad Eydivandi, Hakem Beitollahi.
Journal of Microprocessors and Microsystems (Under Review).

2024 **LoRPIA: Low-power Reconfigurable Pallet-Integrated Accelerator for Depthwise Separable Convolutions**
Sajad Eydivandi, Hakem Beitollahi.
IEEE Transactions on Emerging Topics in Computing (Under Review).

Research Experience

2023 – Present **A novel method to reduce power consumption in convolutional neural network accelerators**
Mentors: Hakem Beitollahi.
Focused on reducing power consumption in AI accelerators, I specialized in low-power design strategies for FPGA-based implementations. Drawing on in-depth knowledge of power-efficient hardware design, I introduced an innovative method for computing convolutions using HDL instead of HLS, substantially improving control over performance and energy efficiency. I successfully designed and implemented two distinct accelerators: one tailored for ultra-low power applications, and another for high-performance, energy-efficient computing. These designs formed the foundation of two strong research papers. Additionally, after an extensive literature review, I authored a comprehensive survey paper on FPGA convolution accelerator architectures and benchmarking approaches. I am currently pursuing three original ideas for further publications in this field.

2020 – 2021 **Implementation of a software infrastructure for supervision and recording events in IOT**
Mentors: Professor Amir Khorsandi.
As part of a collaborative embedded systems course, I worked in a team-based environment where 10 groups developed distinct IoT projects, each leveraging a shared server for specific functionalities. Building upon this foundation, I independently expanded the concept into my B.Sc. final project—developing a comprehensive, scalable system capable of interfacing with diverse hardware components and sensors. I implemented secure web based communication protocols to transmit real-time data to the server, which stored and processed the information efficiently. I also developed a user-friendly frontend web application that visually monitors the status and conditions of each device, enabling intuitive interaction and system management.

Industry Experience

Summer 2021 **Nezhoda (Frontend Developer)** – City, State
Developed a web-based admin panel for an antique shop, handling the full front-end implementation using React and Redux to enable efficient management of inventory and shop operations.

Summer 2019 **IUT Microelectronics Research Lab (Hardware Developer)** – Isfahan, Iran
Completed an 8-week internship under the supervision of Prof. M. Sayedi and Dr. R. Dehghani at IUT's Microelectronics Research Lab. During this program, I designed and implemented a CNN hardware accelerator using SystemVerilog in Xilinx Vivado and developed a corresponding ASIC chip using industry-standard design tools.

Projects

Fall 2023 **Complete Pipelined MIPS Processor with Full Instruction Set** – Advanced Computer Architecture
Designed and implemented a fully pipelined MIPS processor supporting over 20 instructions using Verilog. The processor was deployed and tested on a ZedBoard FPGA platform.

Fall 2023 **Cache Simulator** – Advanced Computer Architecture
Developed a comprehensive cache simulator in Python capable of modeling various cache configurations. The simulator supports multiple replacement policies, set associativity, indexing strategies, and eviction mechanisms.

Spring 2023 **Capsule Convolutional Neural Network on MNIST** – Artificial Intelligence and Deep Learning
Collaborated in a three-member team to study capsule networks by presenting related research papers. Implemented and trained a capsule neural network on the MNIST dataset using TensorFlow, achieving performance comparable to the original research.

Spring 2023 **In-Memory Computing Simulator Using Python and OrCAD** – Storage Systems
Analyzed several research papers on in-memory computing. Selected and replicated the circuit design from a novel approach using OrCAD and developed a Python-based simulator to model the computational behavior.

Fall 2022 **LoRa Protocol Analysis** – Advanced Networking
Conducted an in-depth study of the LoRa communication protocol. Reviewed and presented a novel enhancement method based on findings from a survey of current research.

Fall 2022 **Real-Time Processing over Blockchain** – Real-Time Systems
Explored the integration of real-time processing with blockchain technology. Investigated architectural and algorithmic methods to enable deterministic execution within decentralized environments.

Spring 2020 **Implementation of Educational System (Golestan)** – Advanced Programming
Designed and developed a university management system modeled after Golestan, supporting roles for students, faculty, and staff. The system featured course registration, grading, and mid-semester updates, implemented using C# and MySQL.

Fall 2019 **Custom Transport Layer Protocol Using Raw Sockets** – Networks
Designed a custom transport layer protocol using raw sockets. Constructed full network packets and demonstrated the protocol's functionality in a client-server communication model.

Fall 2019 **FPGA-Based Wave Generator** – Introduction to FPGA and Verilog
Developed an FPGA-based wave generator capable of producing triangular, sinusoidal, and square waves. Visualized signals using external circuits on an oscilloscope and displayed them using the VGA protocol.

Fall 2018 **Radio Receiver Using RTL-SDR** – Communication Systems
Built a software-defined radio (SDR) receiver using MATLAB and RTL-SDR hardware. Created a GUI to scan and play AM and FM radio frequencies.

2016–Present **Independent and Freelance Projects**
Engaged in a wide range of self-initiated and freelance technology projects throughout my undergraduate and graduate studies to explore personal interests in hardware, software, and system design.

Professional Memberships

2022 – Present **Computer Architecture Lab**
Research group under the supervision of Dr. Hakem Beitollahi, focused on advanced topics in computer architecture, hardware security, and hardware acceleration.

Teaching Assistant

Fall - 2023 **Computer Aided Design**
Prof. Hakem Beitollahi

Technical Skills

Programming languages
Proficient in: Verilog, SystemVerilog, Python, C, C++, C#, AVR Assembly, HTML and CSS, JavaScript, SQL, MongoDB.
Familiar with: VHDL, MATLAB, Java, Ladder logic.

Libraries and Frameworkss
Proficient in: Tensoflow, Keras, Pytorch, React+Redux, CUDA, pthread.

Software
LaTeX, Git, Vivado, ISE, Design compiler, Cadence Virtuoso, Cadence encounter, Synopsys design vision, HSPICE, OrCAD , Altium Designer, Hyperlynx , Simulink, PSIM, PI Expert, Packet Tracer, Proteus, Wireshark, Visual Studio Code, Visual Studio, Code::Blocks, Microsoft Office, Siemens TIA Portal, Relex, Disksim.

Languages
English (Fluent), Persian (Native).

Other Interests

Professional Chess, Recreational Muay Thai and Calisthenics, Watching Movies, Listening to Music, and Reading Books.