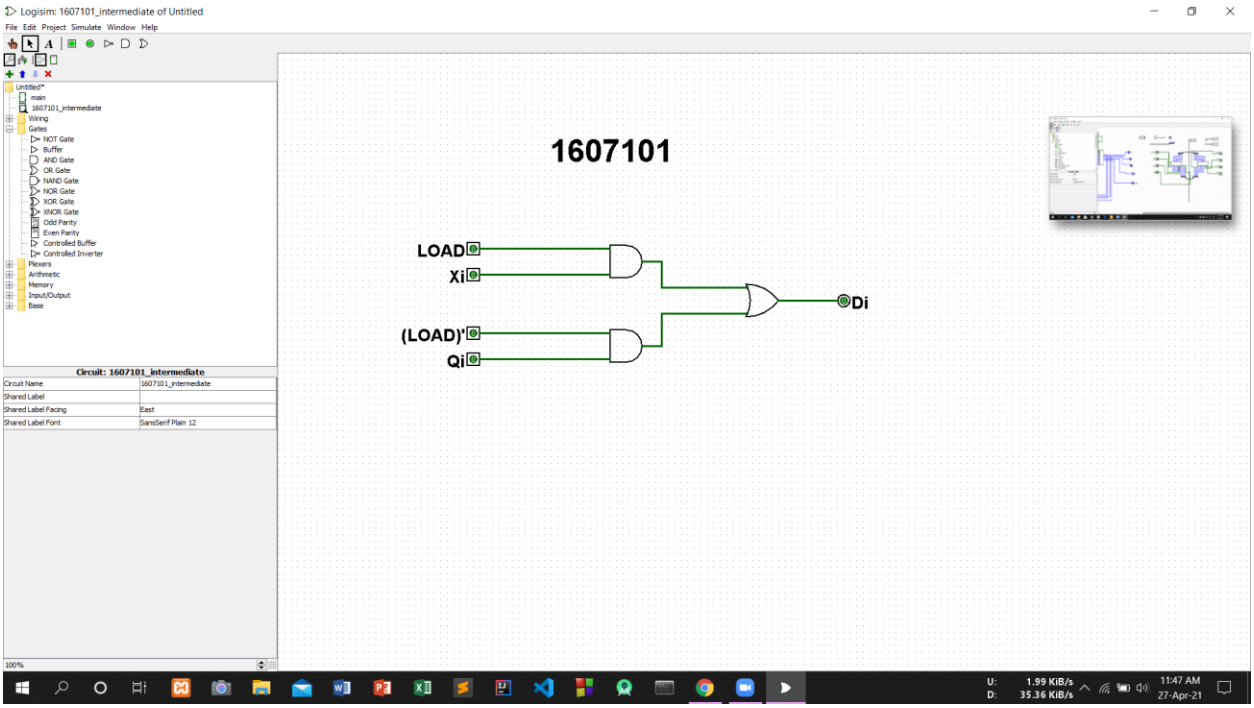
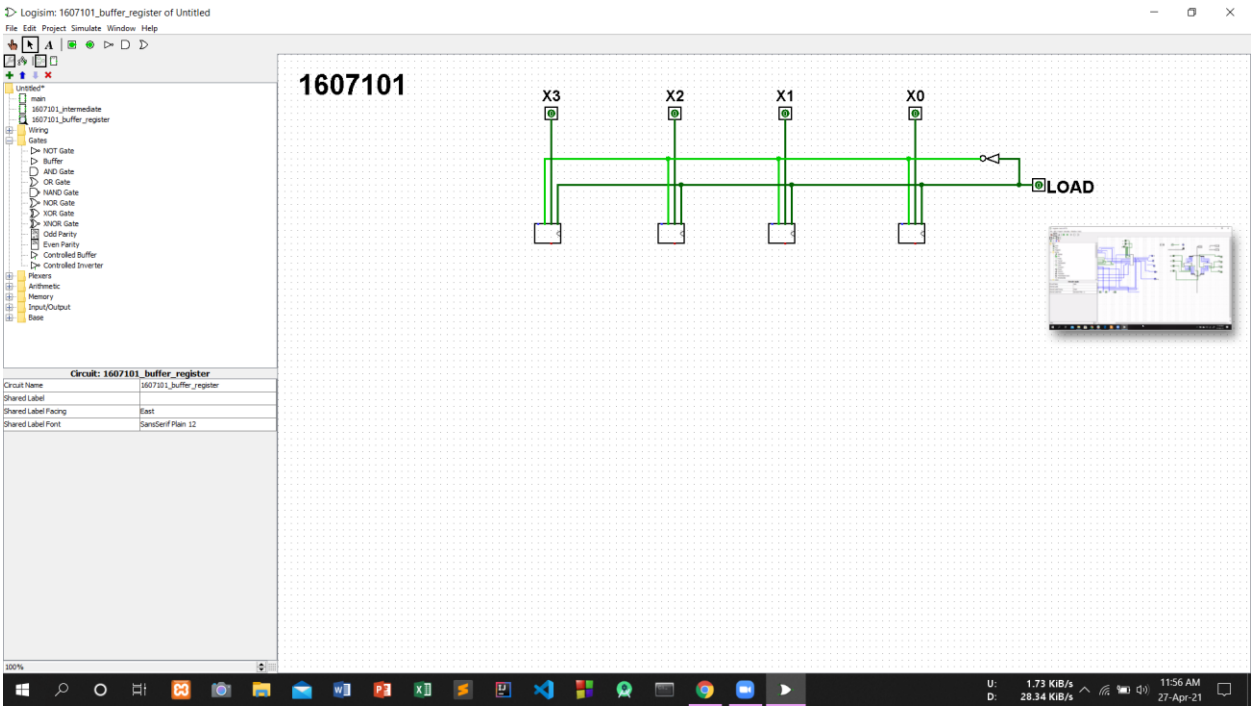
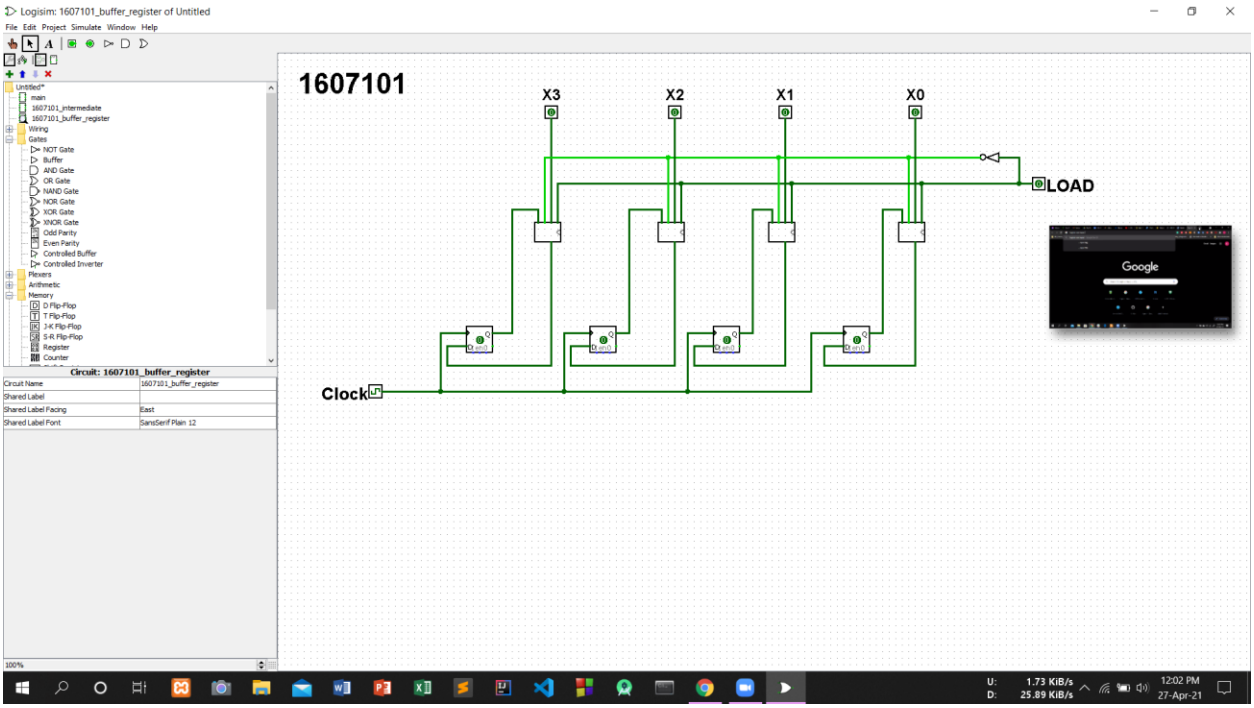
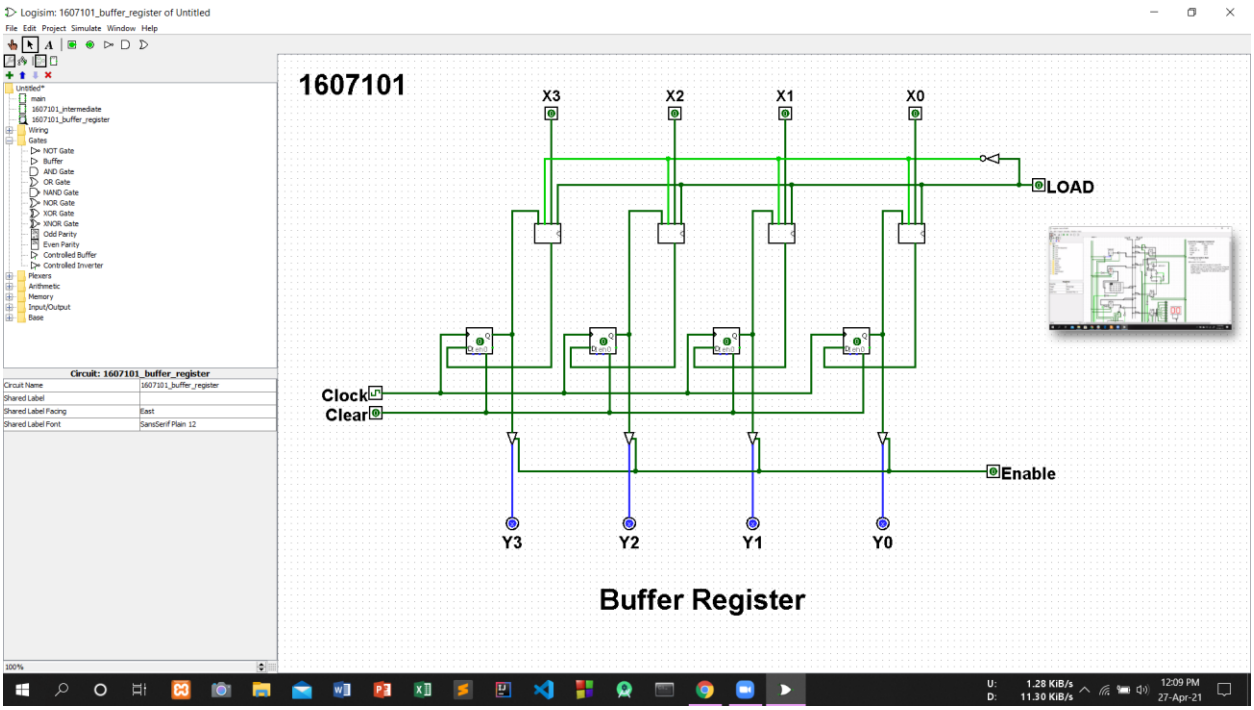
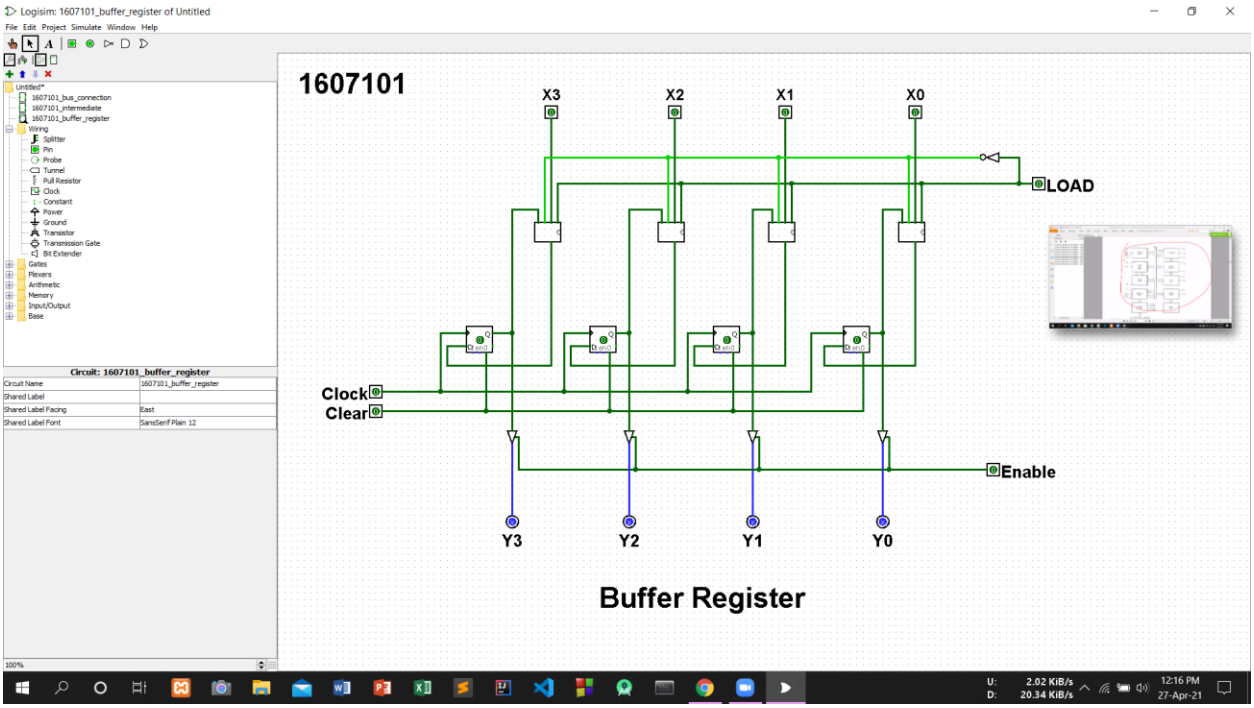
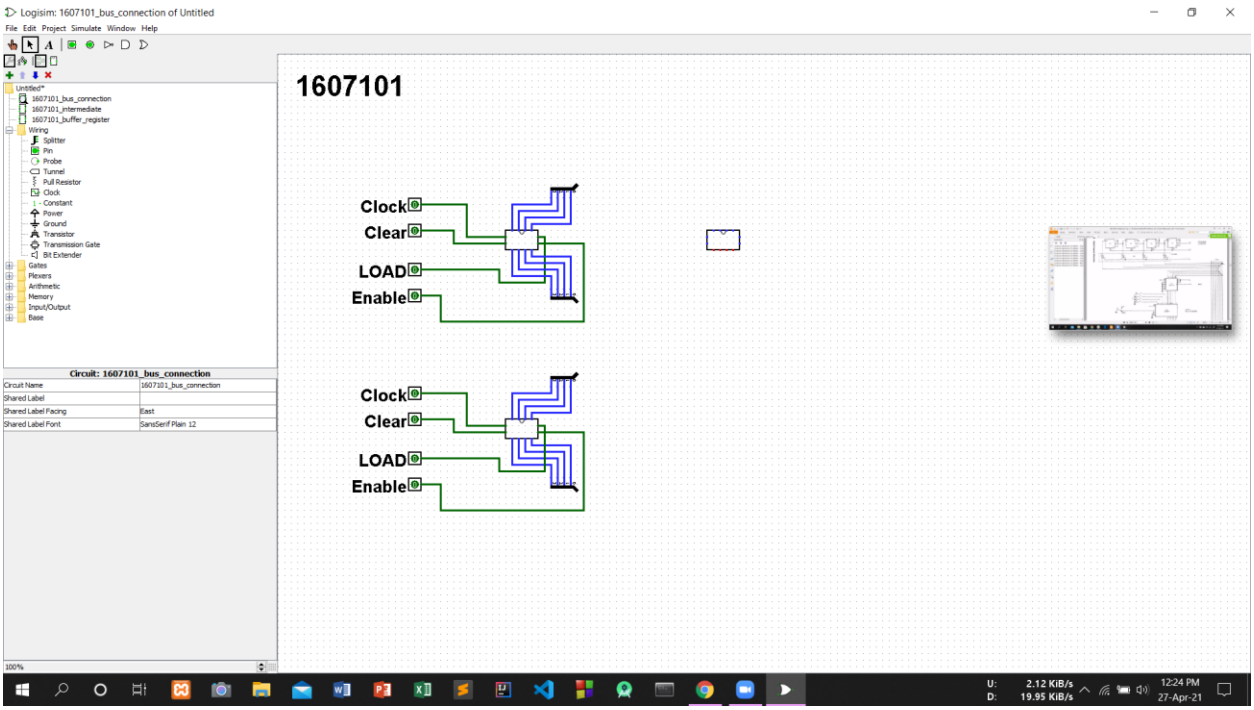

Logisim: 1607101_intermediate of Untitled
File Edit Project Simulate Window Help
Circuit: 1607101_intermediate
1607101
LOAD
Xi
(LOAD)'
Qi
Di

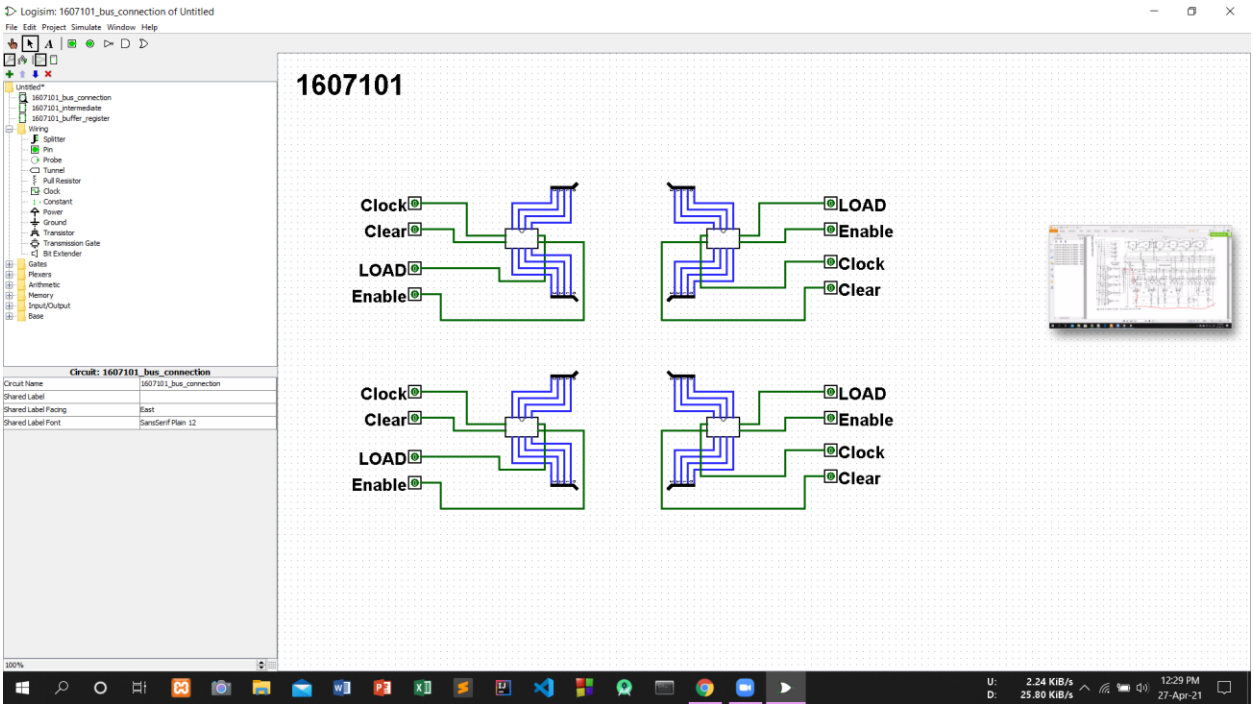

Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
Circuit: 1607101_buffer_register
1607101
X3
X2
X1
X0
LOAD

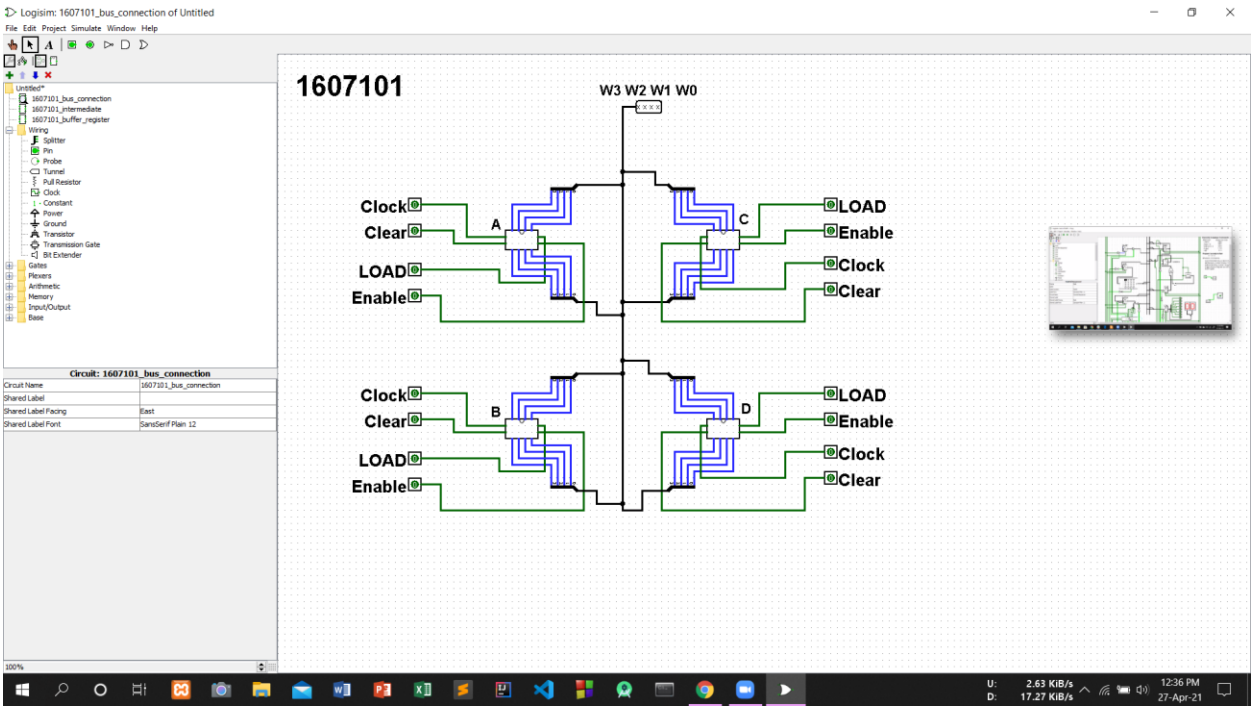

Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Google
Circuit: 1607101_buffer_register
Circuit Name 1607101_buffer_register
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
100%
U: 1.73 KiB/s
D: 25.89 KiB/s
12:02 PM
27-Apr-21

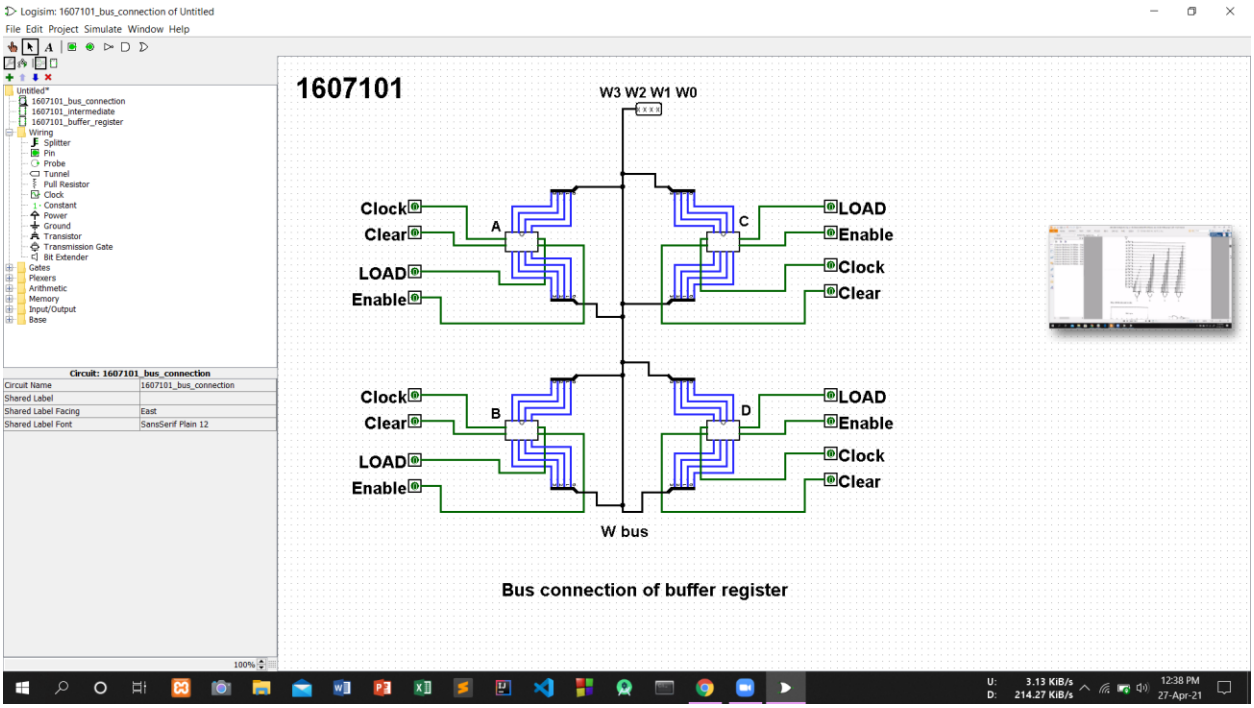

Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register
Circuit: 1607101_buffer_register
Circuit Name 1607101_buffer_register
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
100%
U: 1.28 KiB/s
D: 11.30 KiB/s
12:09 PM
27-Apr-21

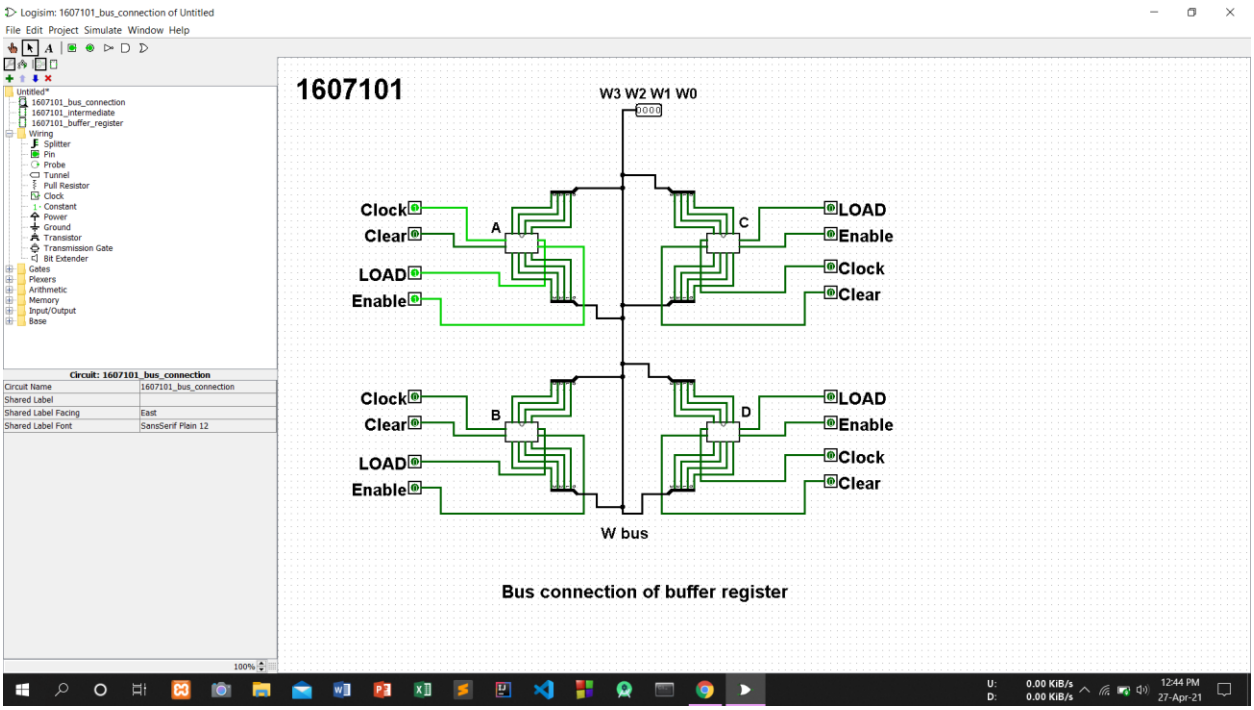

Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register
Circuit: 1607101_buffer_register
Circuit Name 1607101_buffer_register
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
U: 2.02 KiB/s
D: 20.34 KiB/s
12:16 PM
27-Apr-21

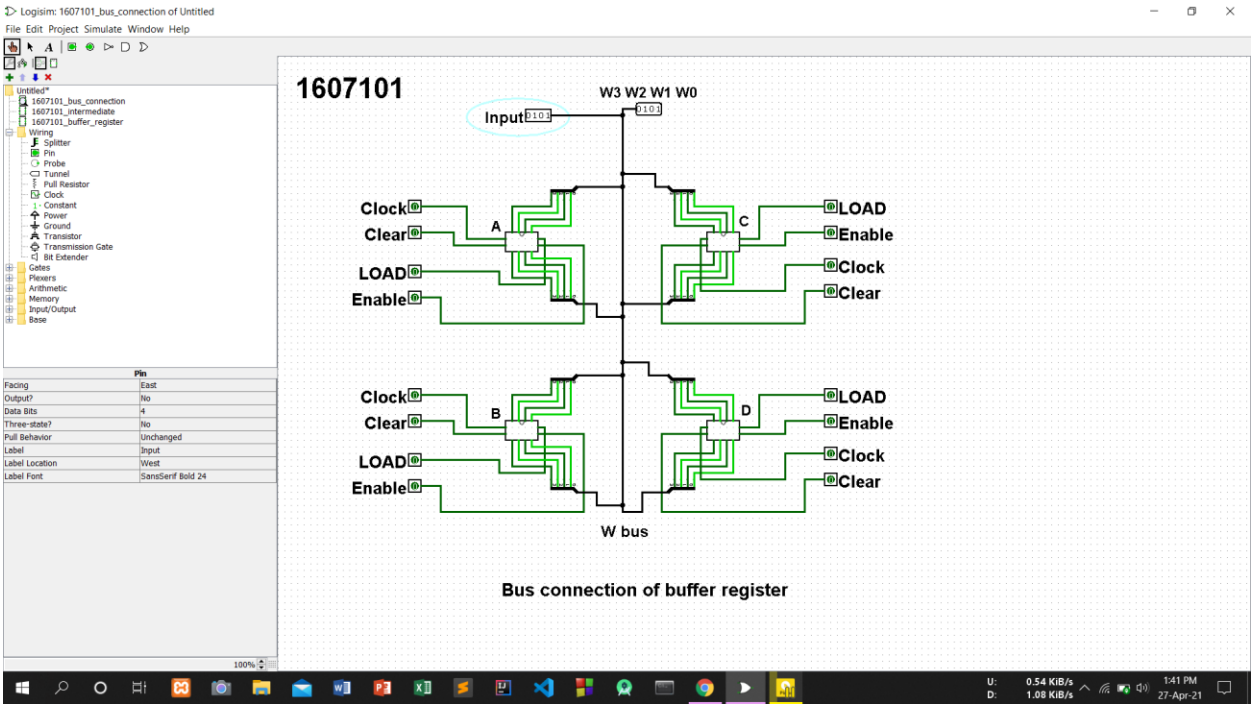

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
Clock
Clear
LOAD
Enable
Clock
Clear
LOAD
Enable
Circuit: 1607101_bus_connection
Circuit Name 1607101_bus_connection
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
U: 2.12 KiB/s
D: 19.95 KiB/s
12:24 PM
27-Apr-21

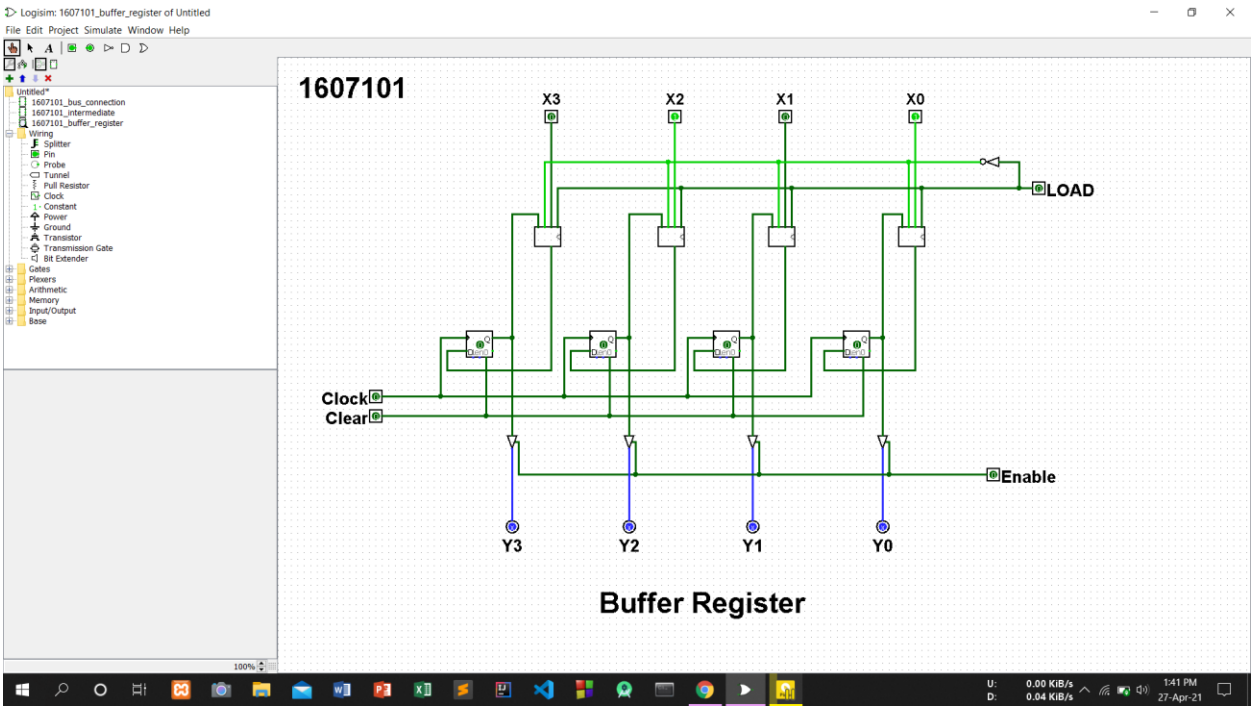

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
Clock
Clear
LOAD
Enable
LOAD
Enable
Clock
Clear
Clock
Clear
LOAD
Enable
LOAD
Enable
Clock
Clear
Circuit: 1607101_bus_connection
Circuit Name 1607101_bus_connection
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
U: 2.24 KiB/s
D: 25.80 KiB/s
12:29 PM
27-Apr-21

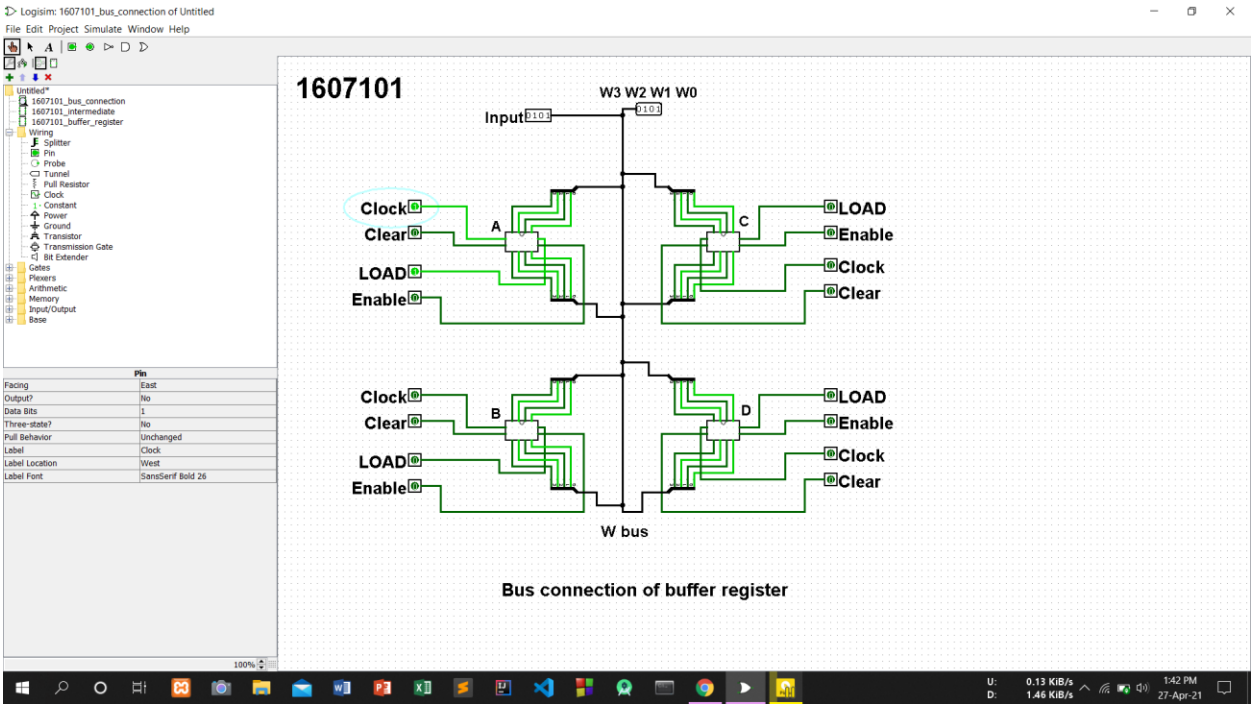

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
A
B
C
D
Clock
Clear
LOAD
Enable
LOAD
Enable
Clock
Clear
Clock
Clear
LOAD
Enable
LOAD
Enable
Clock
Clear
Circuit: 1607101_bus_connection
Circuit Name 1607101_bus_connection
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
U: 2.63 KiB/s
D: 17.27 KiB/s
12:36 PM
27-Apr-21

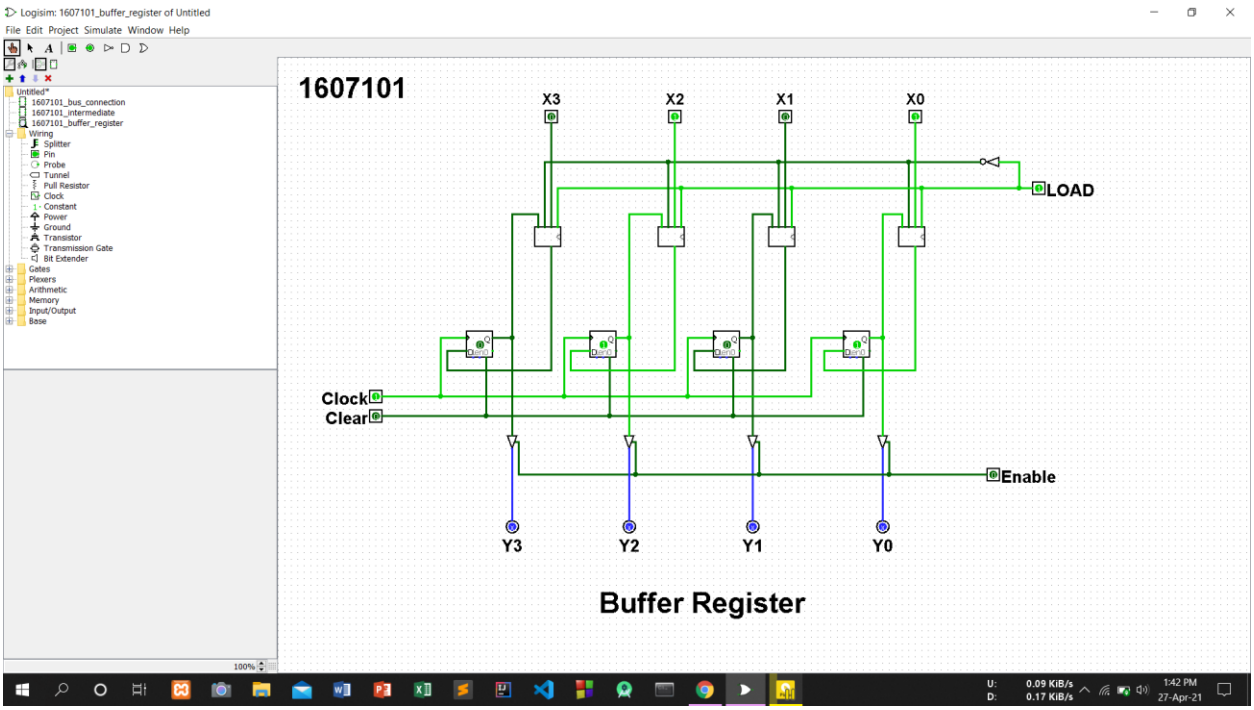

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
Clock
Clear
LOAD
Enable
A
B
C
D
W bus
Bus connection of buffer register
Circuit: 1607101_bus_connection
Circuit Name
1607101_bus_connection
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12

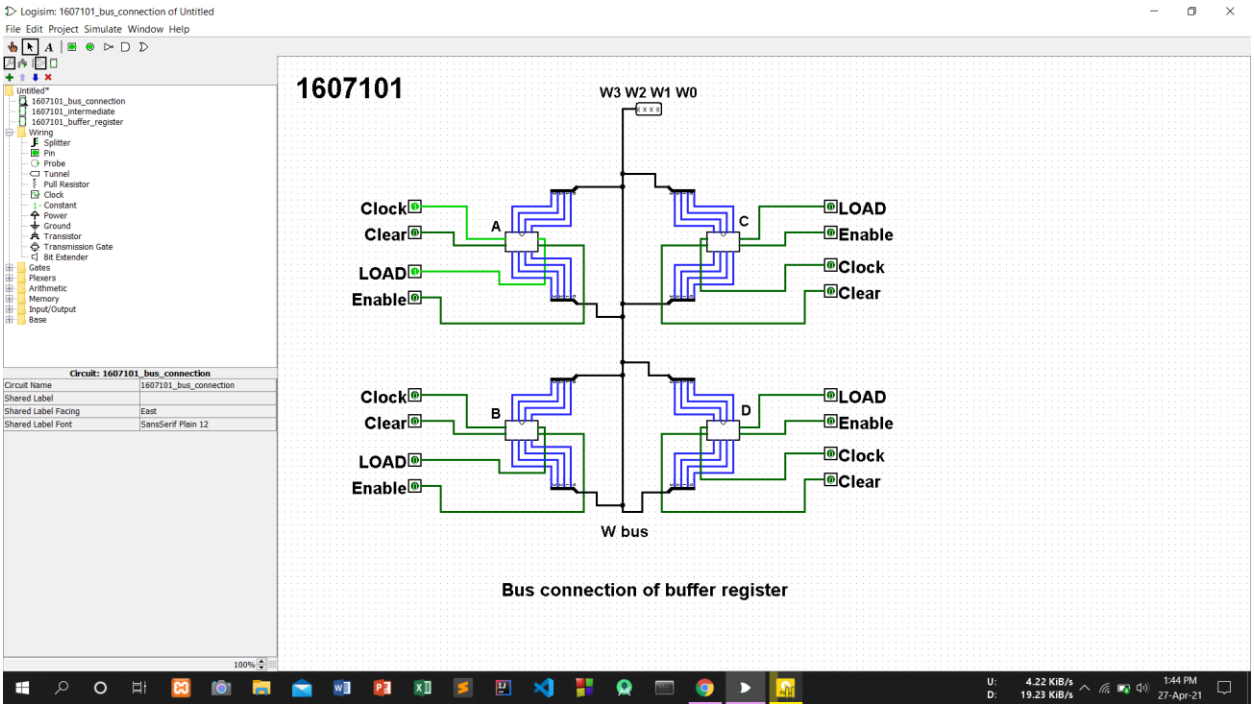

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
Clock
Clear
LOAD
Enable
A
B
C
D
W bus
Bus connection of buffer register
Circuit: 1607101_bus_connection
Circuit Name
1607101_bus_connection
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12

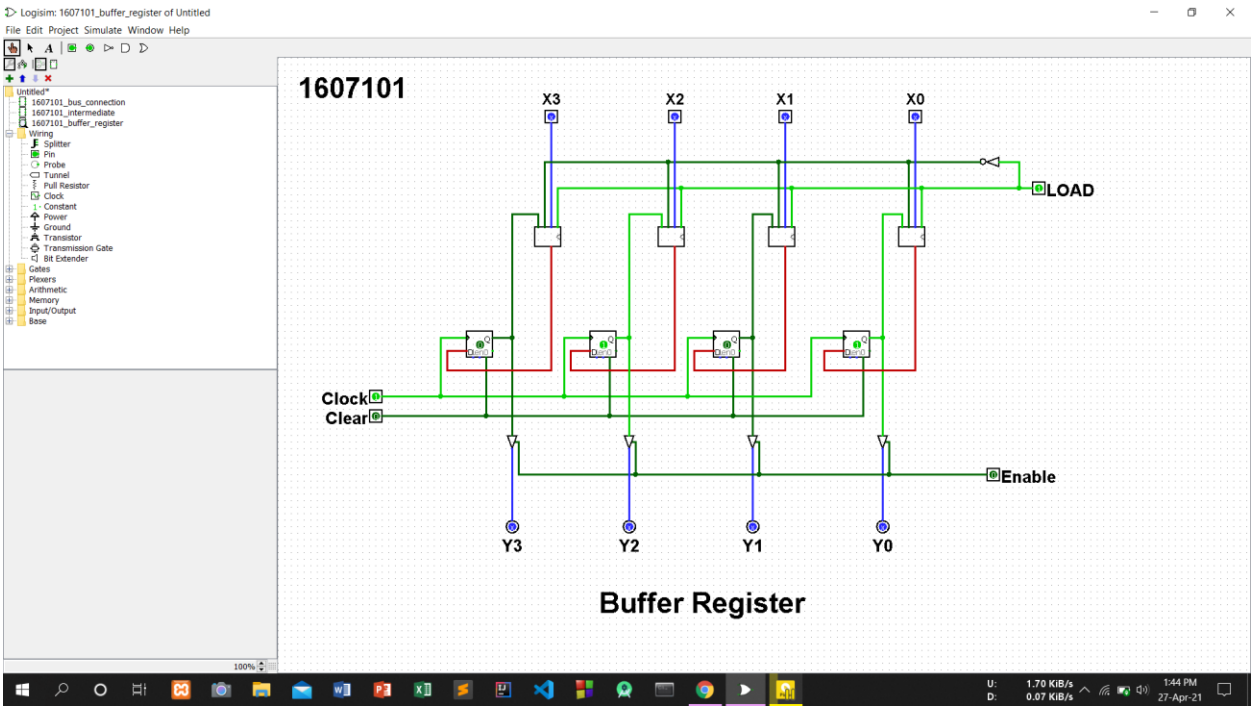

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
Input
Clock
Clear
LOAD
Enable
A
B
C
D
LOAD
Enable
Clock
Clear
W bus
Bus connection of buffer register
Pin
Facing East
Output? No
Data Bits 4
Three-state? No
Pull Behavior Unchanged
Label Input
Label Location West
Label Font SansSerif Bold 24

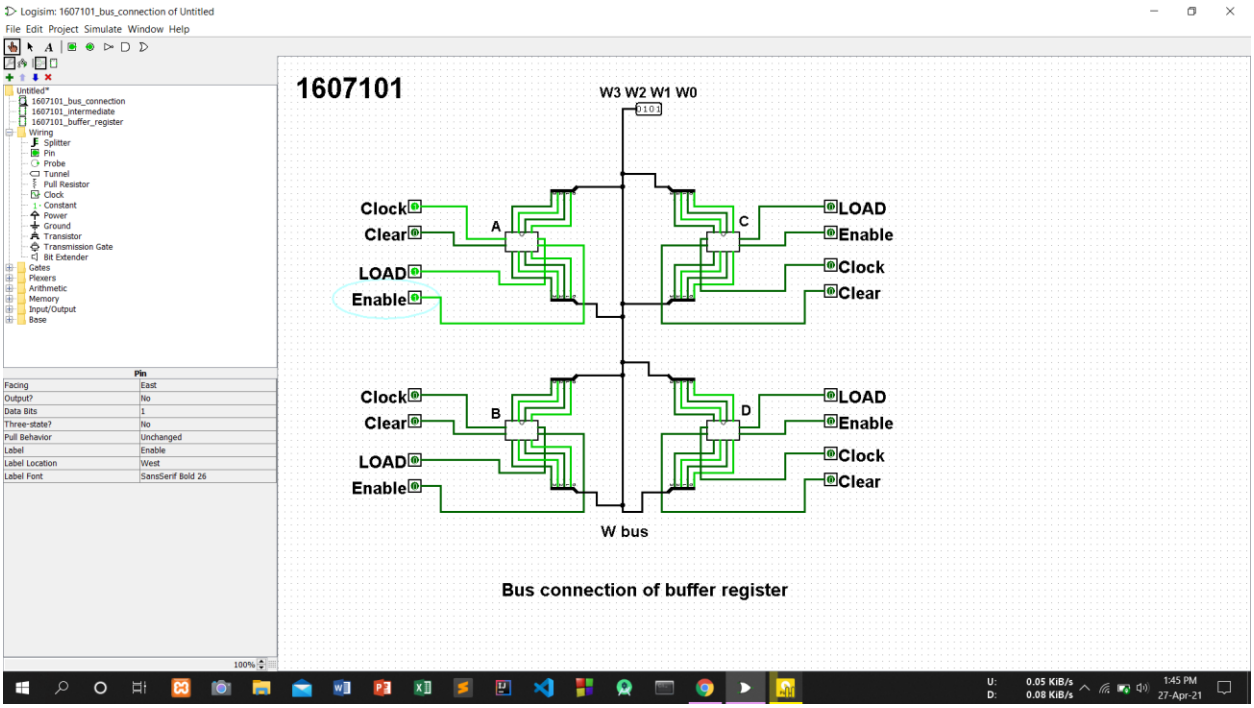

Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register

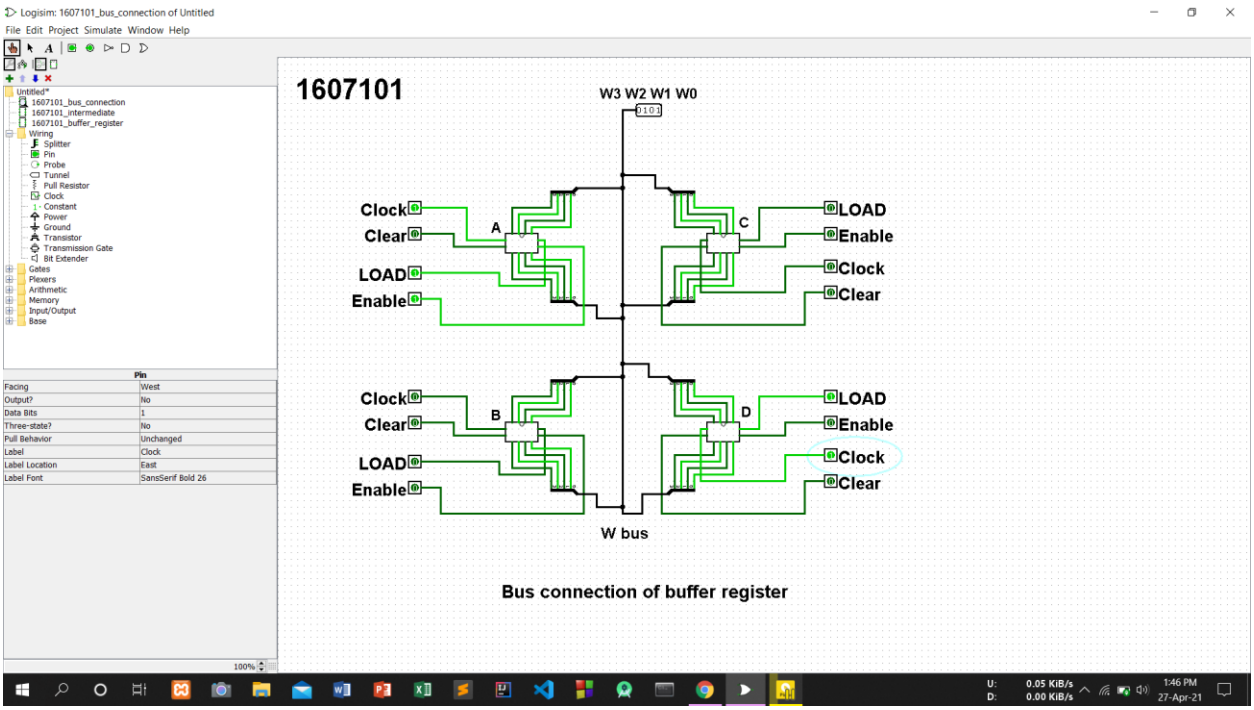

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
Input
Clock
Clear
LOAD
Enable
A
C
LOAD
Enable
Clock
Clear
Clock
Clear
LOAD
Enable
B
D
LOAD
Enable
Clock
Clear
W bus
Bus connection of buffer register

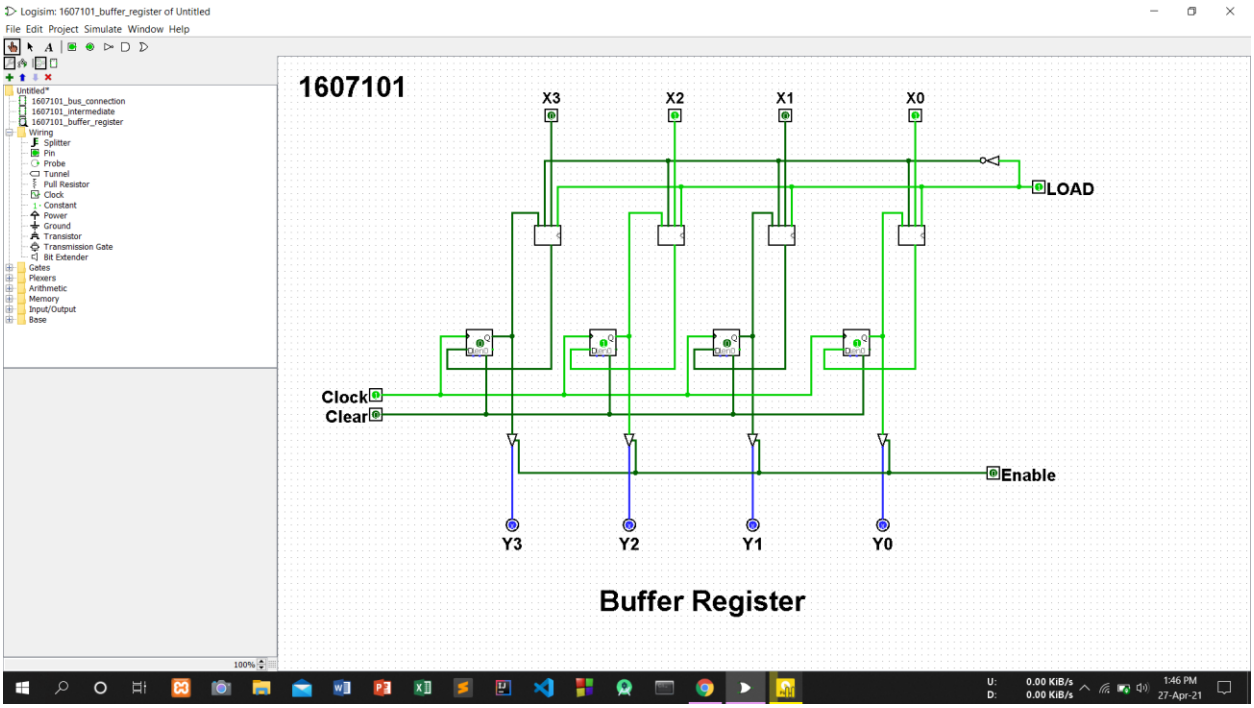

Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register

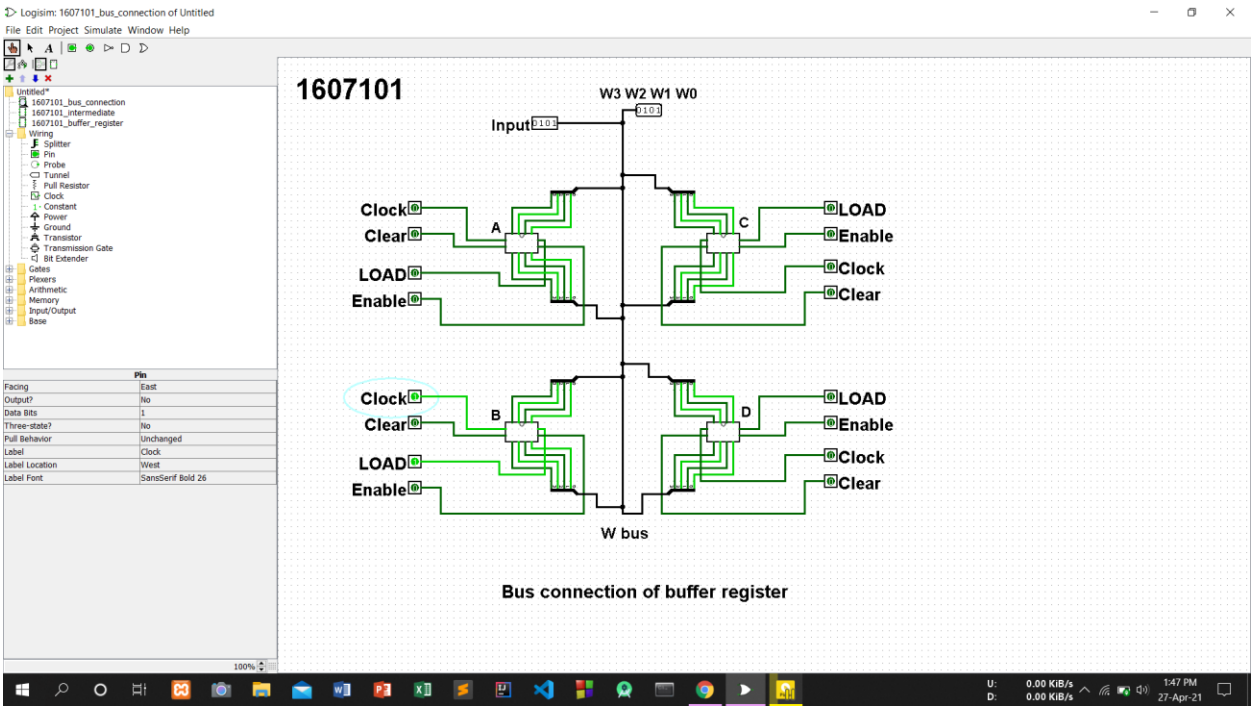

Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
Clock
Clear
LOAD
Enable
A
C
LOAD
Enable
Clock
Clear
Clock
Clear
LOAD
Enable
B
D
LOAD
Enable
Clock
Clear
W bus
Bus connection of buffer register

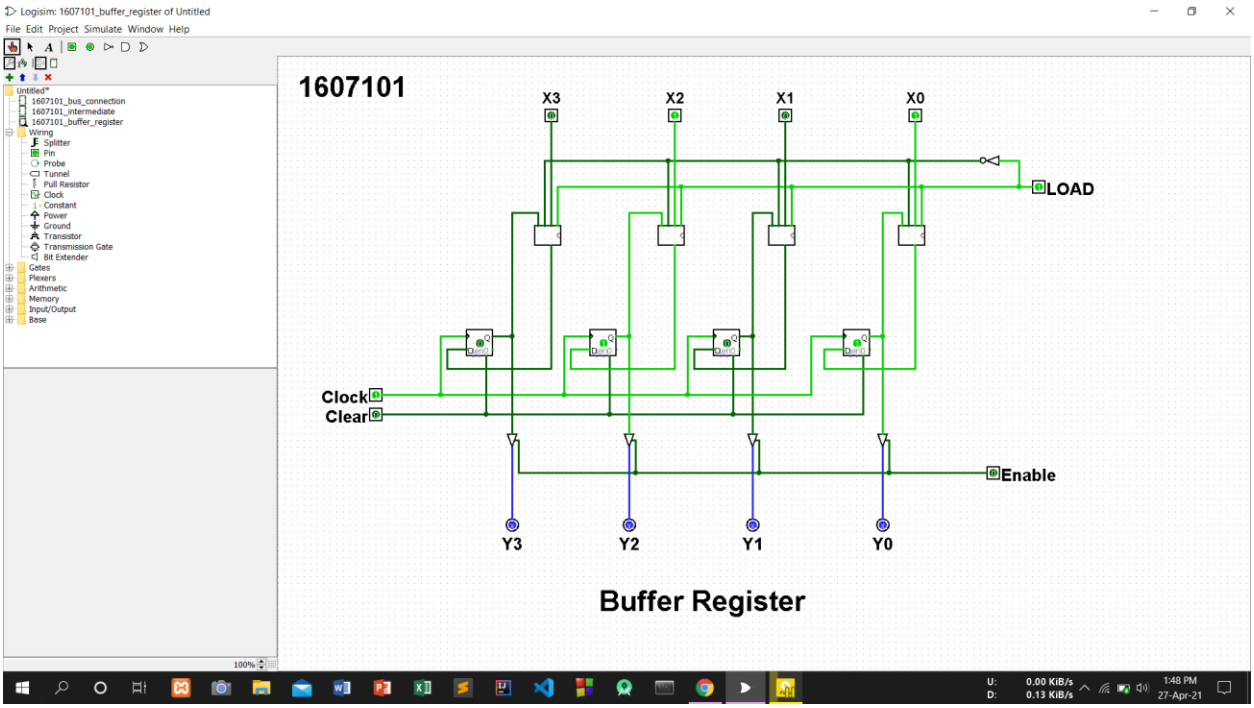

Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register


Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
0101
Clock
Clear
LOAD
Enable
A
B
C
D
LOAD
Enable
Clock
Clear
W bus
Bus connection of buffer register
Pin
Facing East
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label Enable
Label Location West
Label Font SansSerif Bold 26
U: 0.05 KiB/s
D: 0.08 KiB/s
1:45 PM
27-Apr-21


Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
0101
Clock
Clear
LOAD
Enable
A
B
C
D
LOAD
Enable
Clock
Clear
W bus
Bus connection of buffer register
Pin
Facing West
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label Clock
Label Location East
Label Font SansSerif Bold 26
U: 0.05 KiB/s
D: 0.00 KiB/s
1:46 PM
27-Apr-21


Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register


Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
Input
Clock
Clear
LOAD
Enable
A
B
C
D
W bus
Bus connection of buffer register


Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
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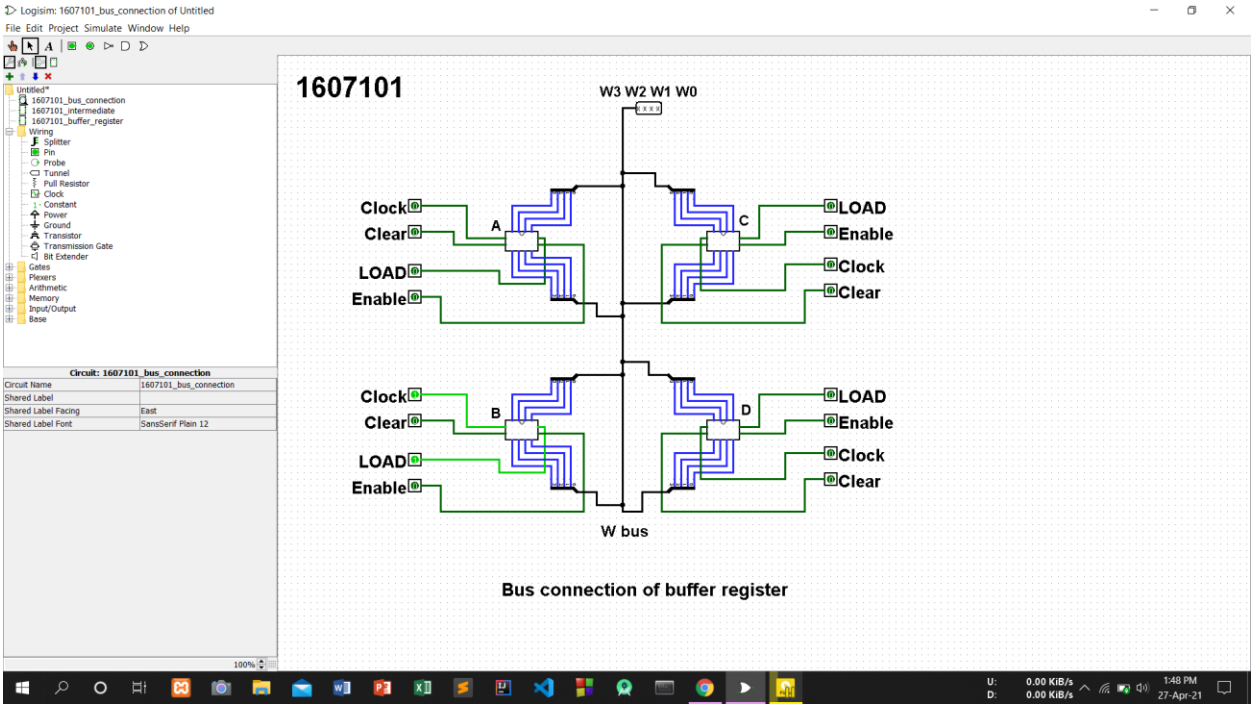
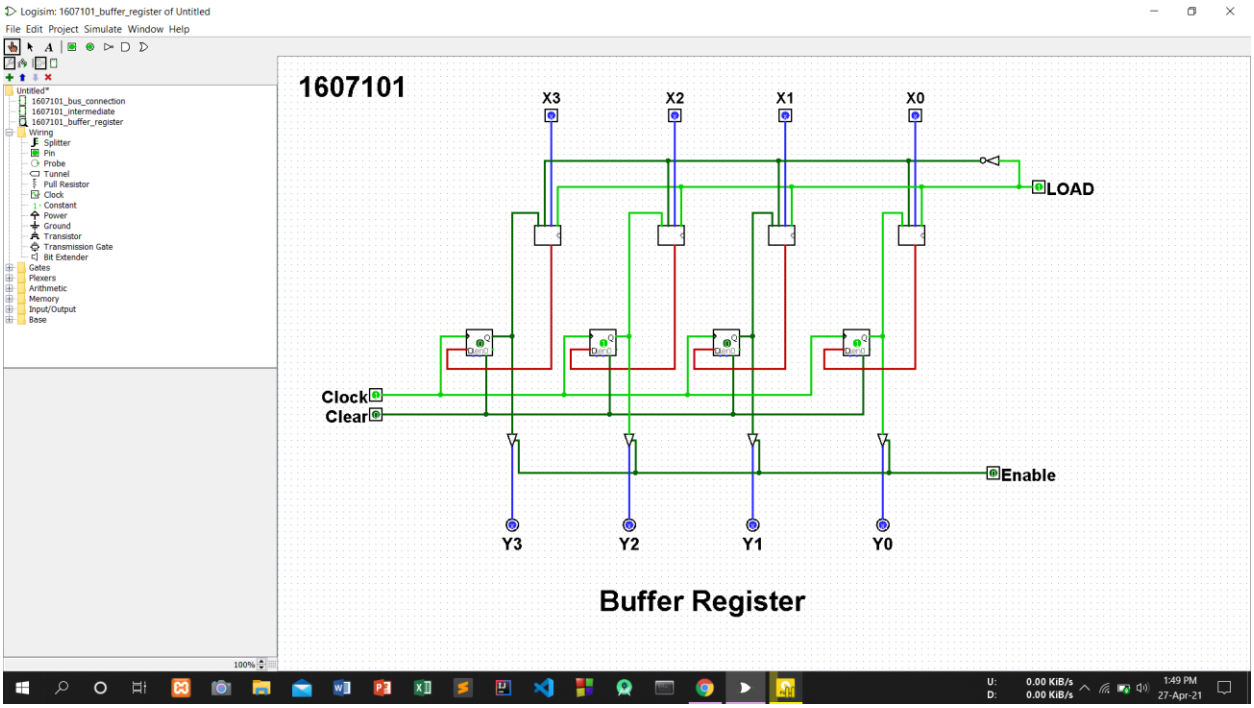
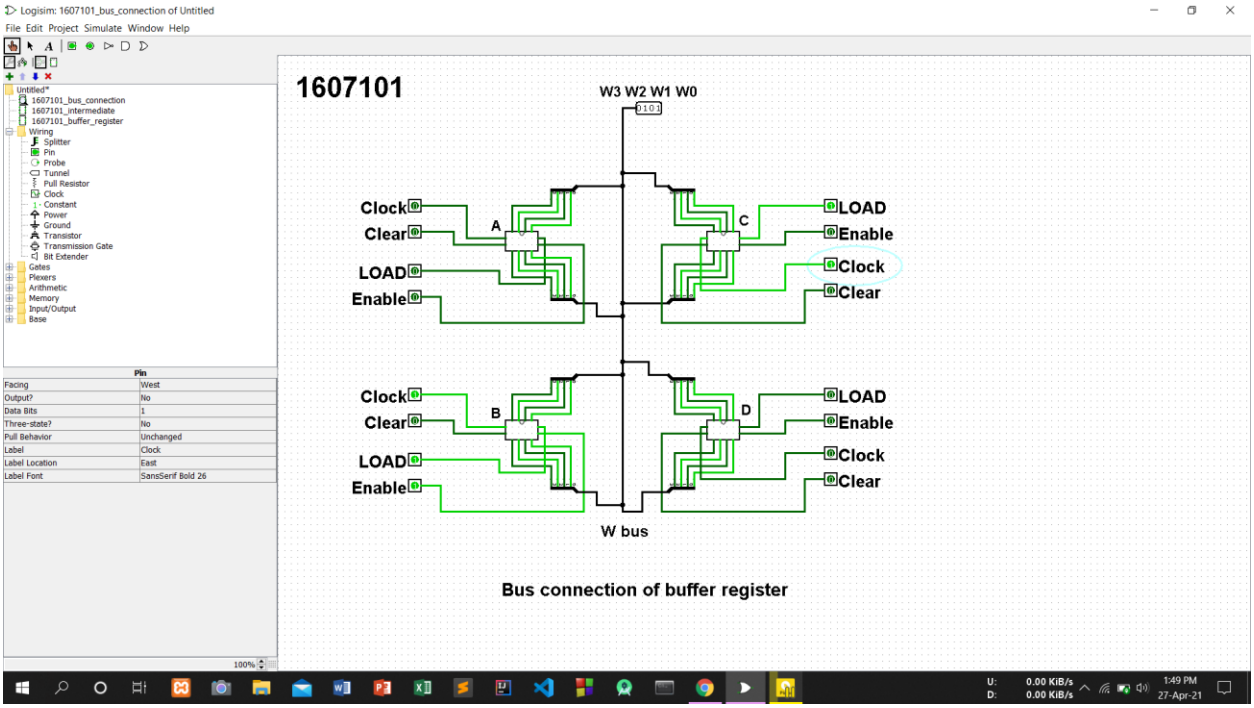
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register


Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
1607101
W3 W2 W1 W0
Clock
Clear
LOAD
Enable
A
B
C
D
W bus
Bus connection of buffer register


Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register


Logisim: 1607101_bus_connection of Untitled
File Edit Project Simulate Window Help
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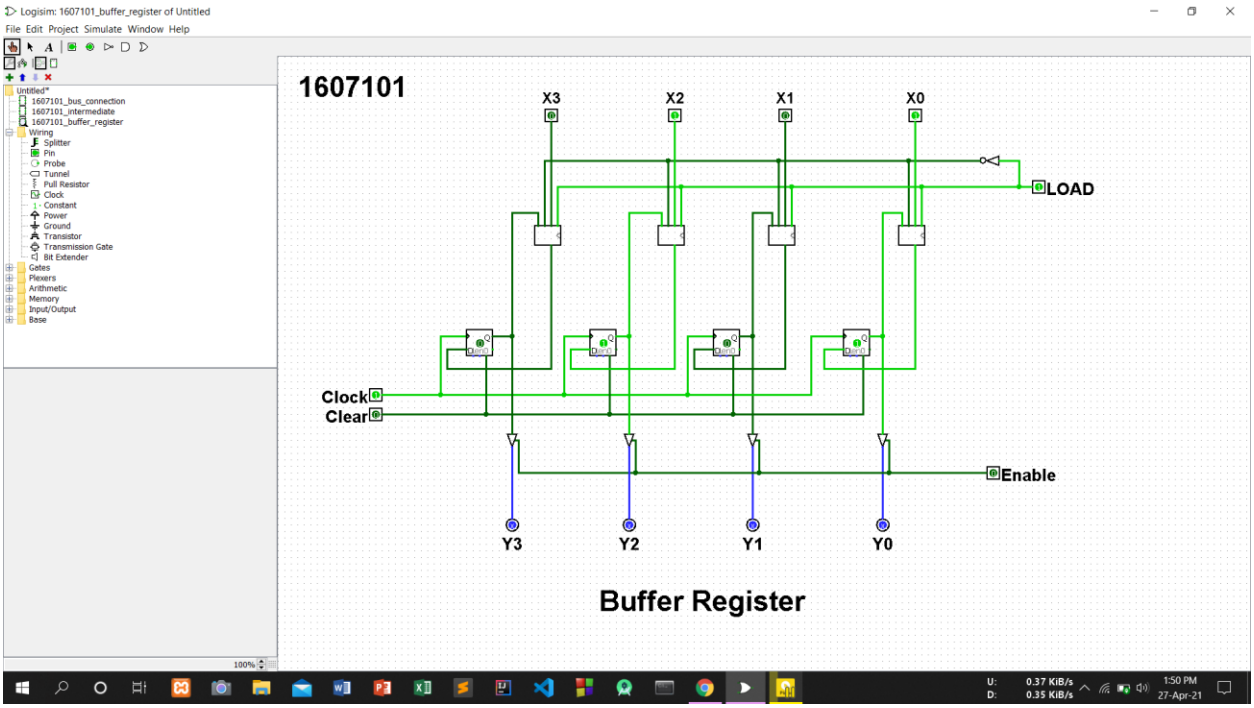
W3 W2 W1 W0
Clock
Clear
LOAD
Enable
A
B
C
D
W bus
Bus connection of buffer register


Logisim: 1607101_buffer_register of Untitled
File Edit Project Simulate Window Help
1607101
X3
X2
X1
X0
LOAD
Clock
Clear
Enable
Y3
Y2
Y1
Y0
Buffer Register