

#### Khulna University of Engineering & Technology (KUET)

Department of Computer Science and Engineering

**Course Code:** CSE 4224

**Course Title:** Digital System Design Laboratory

**Lab Report** 

Name of the experiment: Designing logic unit of ALU in logisim.

#### **Submitted by:**

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Year: 4th

Term: 2<sup>nd</sup>

**Date of Submission:** 26<sup>th</sup> April, 2021

## Objectives:

The main purposes of this lab are stated below:

-> gethering knowledge about half adder and full addert circevit.

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- gathering knowledge about k-map of full adder & arithmatic circuit.
- -> learning about ancithmatic and logical operation and implementation of arithmetic circuit.

# Introduction!

Greneral purepose ALU has eight areitematic operation and four logical operations. It has three selectors variable 82,81, 80 which select eight operations with another variable Cin (input carry bit).

For OR and AND operations we use Ai, Bi, Ci, Sz, S1, So as input and generate two consequences or outputs named of fi & City.

### for oR operation!

82=1, input carery (1 is zero in each stage and 3, So = 00; here the function ix fi=A. To change the OR operation we must change the input of each full adder circuit from Aito Ai+Bi.

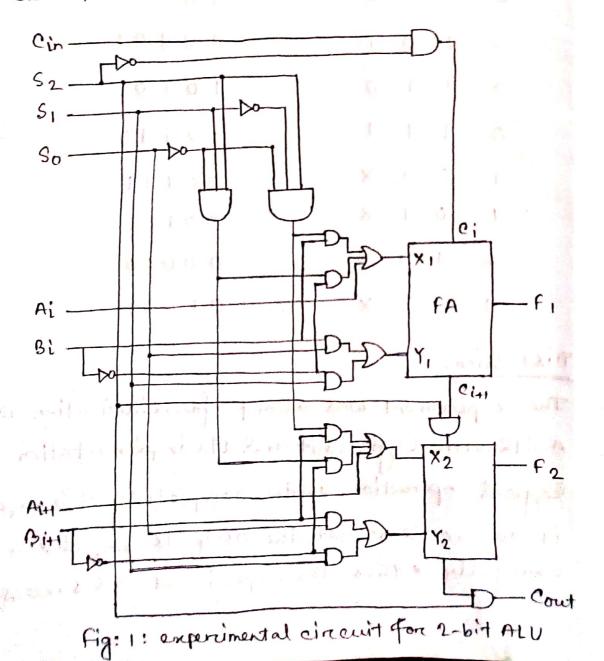
### for AND operation:

When  $S_2=1$ ,  $S_1S_0=10$ , it stands for AND operation.  $F=A_1 \bigcirc B_i$ , we generate AND operation  $f_1=AiBi$ , Some boolean function  $t_1 f_i$  is obtained when  $S_2 S_1 S_0=110$ , then

Fi = Xi @ Yi = (Ai @ Ki) @ Bi = Ai Bi+ ki Bi+ Ai Ki Bi'

#### Experimental Setup:

2-Bit ALU circuit for logical operationisane shown below:



#### Expercimental Result:

Herre, A= 0110 & B=0001

Selection			Dutput	
32 8,	50	Cin	Cout 46	
0 0	1 0	0 , 4	0000000	
0 0	0	1 300	00111	
0	0 1	O	00111	
0	0	L. Hipper	100 100 00 A	
0	1 0	0	10100	
0	1 0		10101	
0	1 1	D	10101	
0	1 1	1	10110	
1	0 0	×	00111	
1	0 1	X	00111	
por Montago III	1,20	×	0 0 0 0 0	
1	AL	×	01001	
		,	1 -	

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## Discussion:

The experiment was about familiarization with Arrithmatic Logic Unit and its implementation for Logical operation. After completing the experiment, it can be seen that, the outputs are observed carefully. Thus, the experiment was successful.

#### Conclusion:

In this lab, the arrithmatic and logical operations of ALU were observed. The circuit was implemented from scotach using full adder. The results are observed with the truth table as well.