

Logisim: 1607101_buffer_register of 1607101
File Edit Project Simulate Window Help

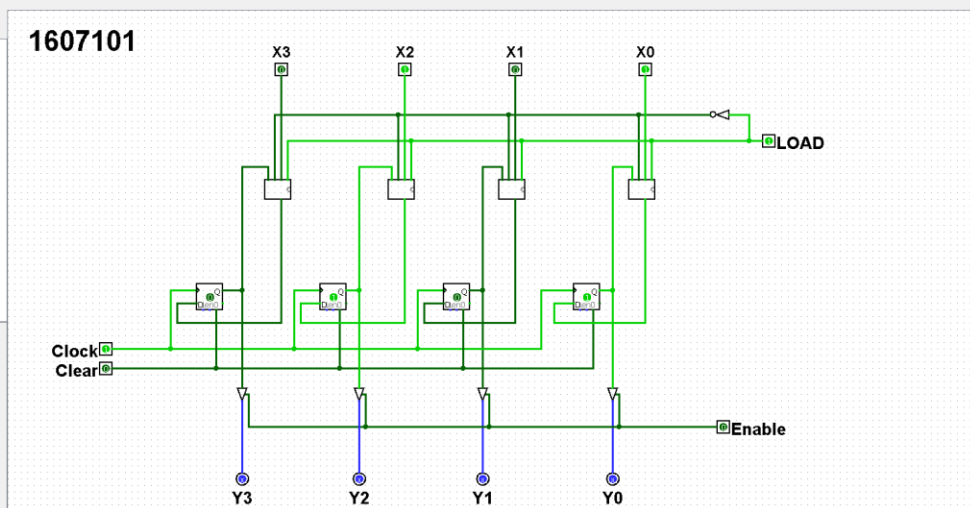
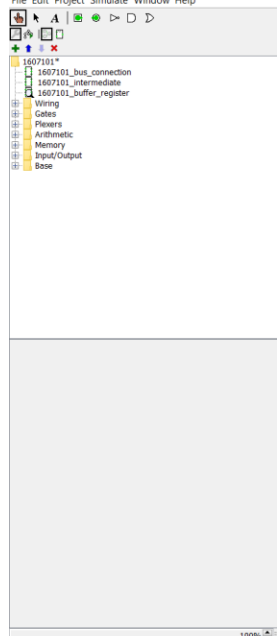


Fig. 2: Buffer Register

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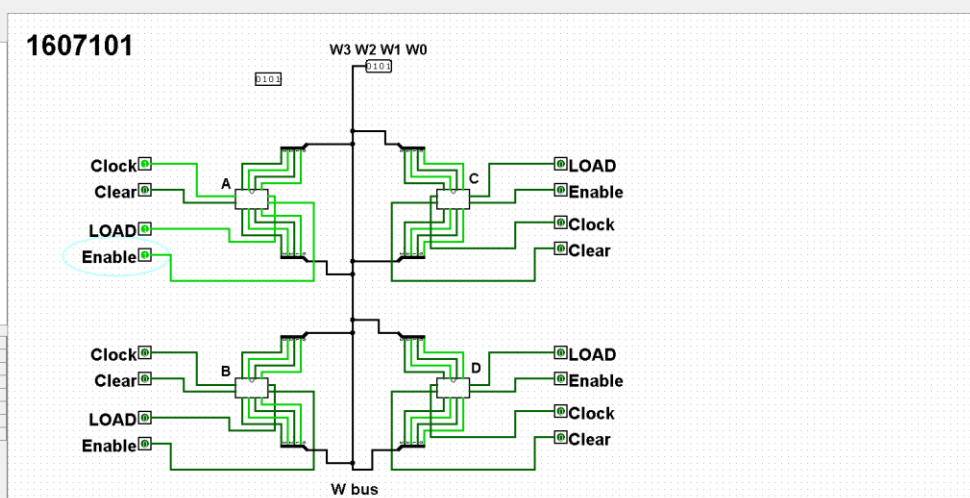
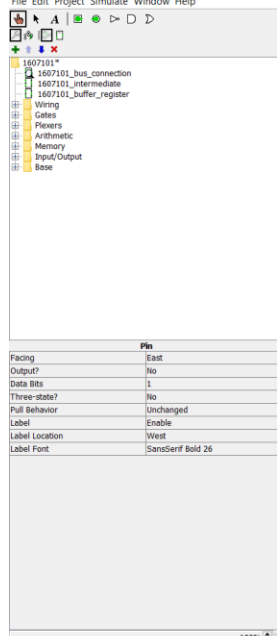


Fig. 3: Bus connection of buffer register

Logisim: 1607101_buffer_register of 1607101
File Edit Project Simulate Window Help

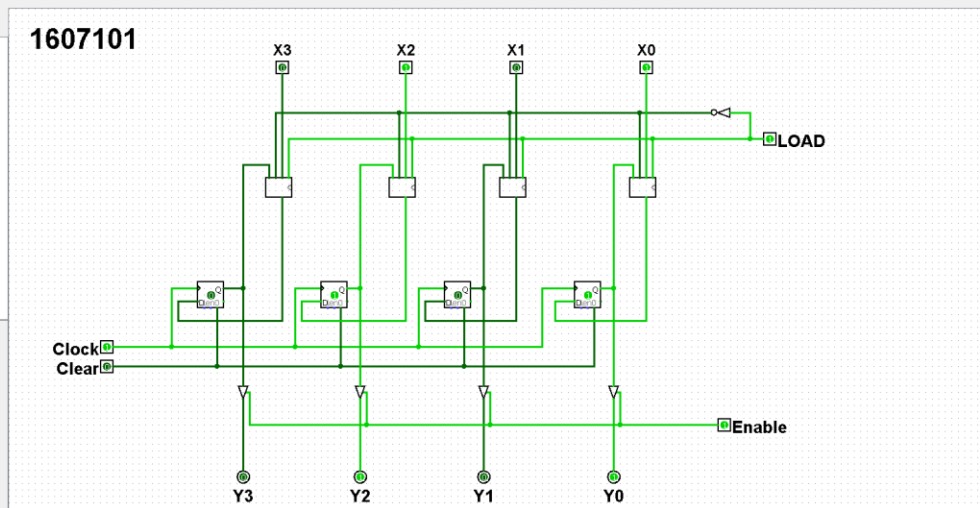
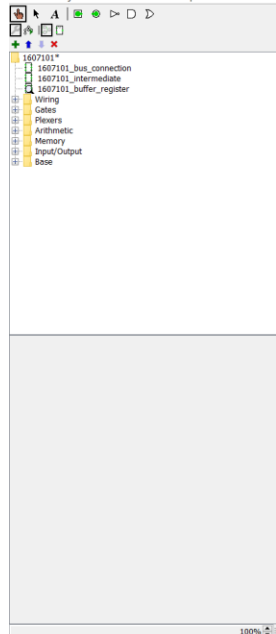


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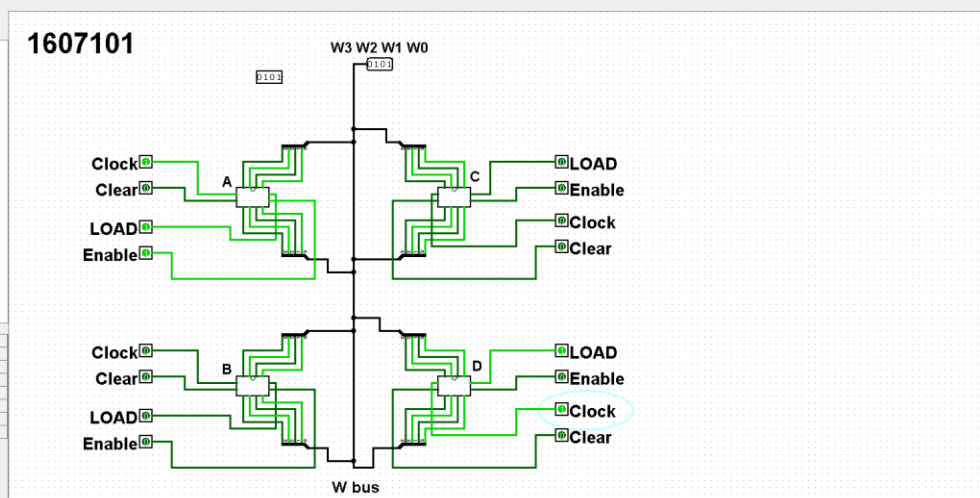
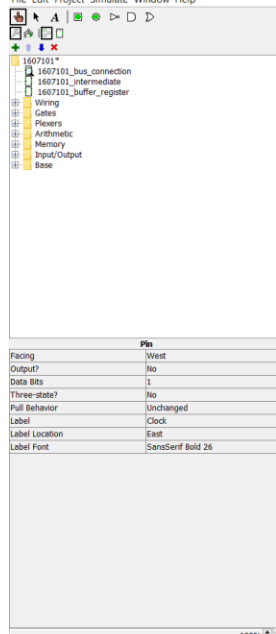


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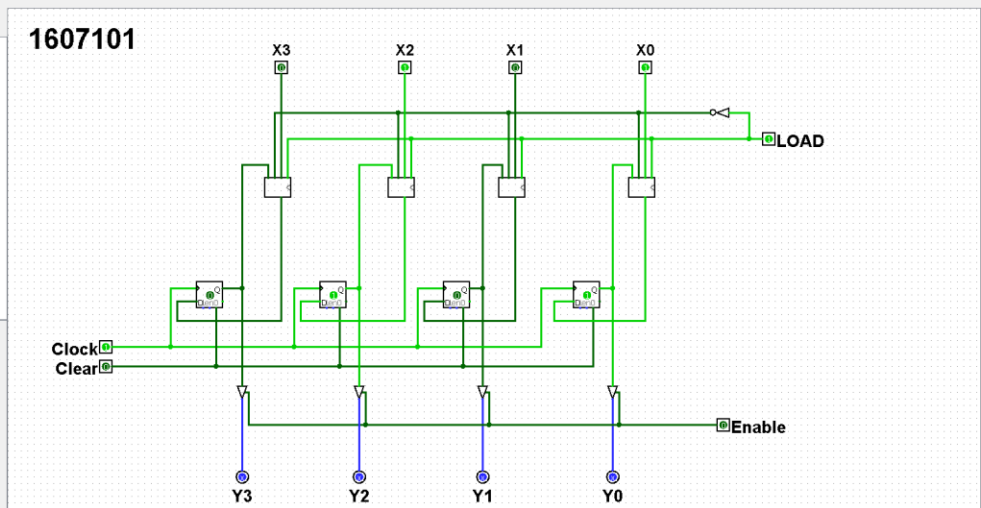
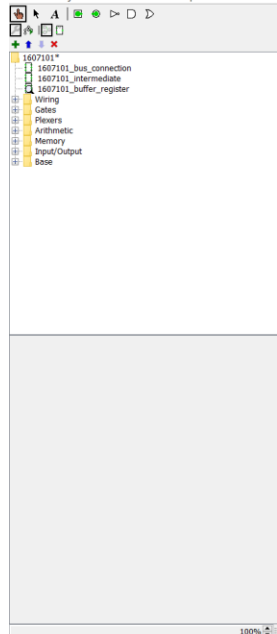


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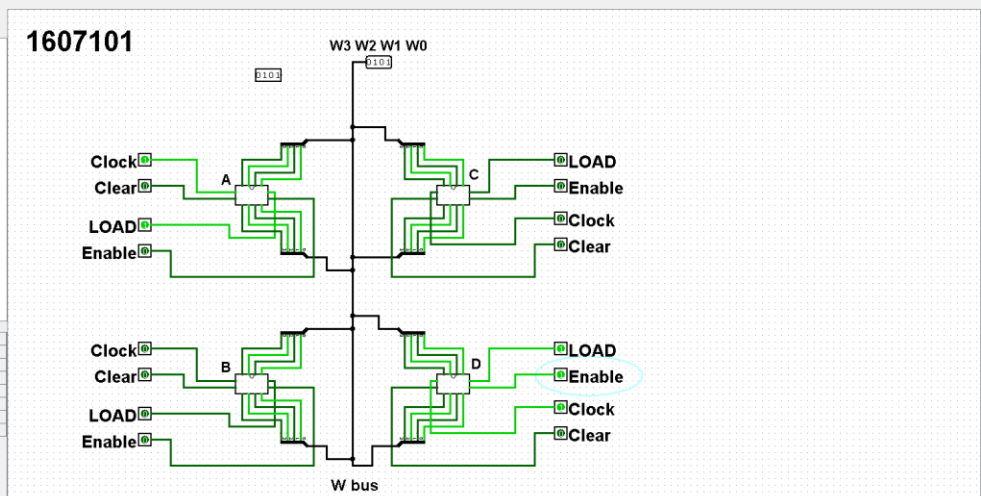
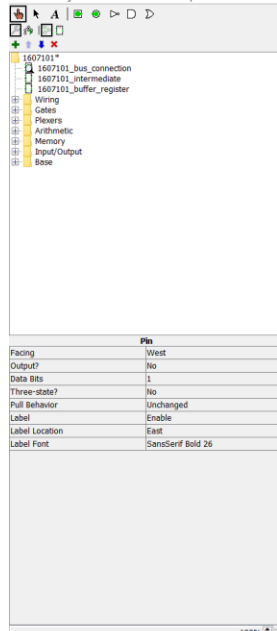


Fig. 3: Bus connection of buffer register

1607101*

- 1607101_bus_connection
- 1607101_intermediate
- 1607101_buffer_register
- Gates
- Plexers
- Arithmetic
- Memory
- Input/Output
- Base

Pin	Pin
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	Clock
Label Location	West
Label Font	SanSerif Bold 26

100%

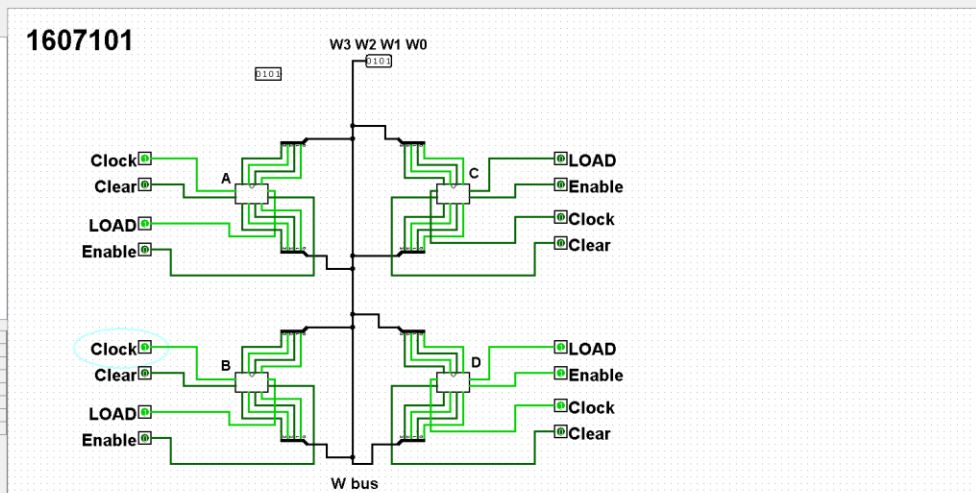


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100%

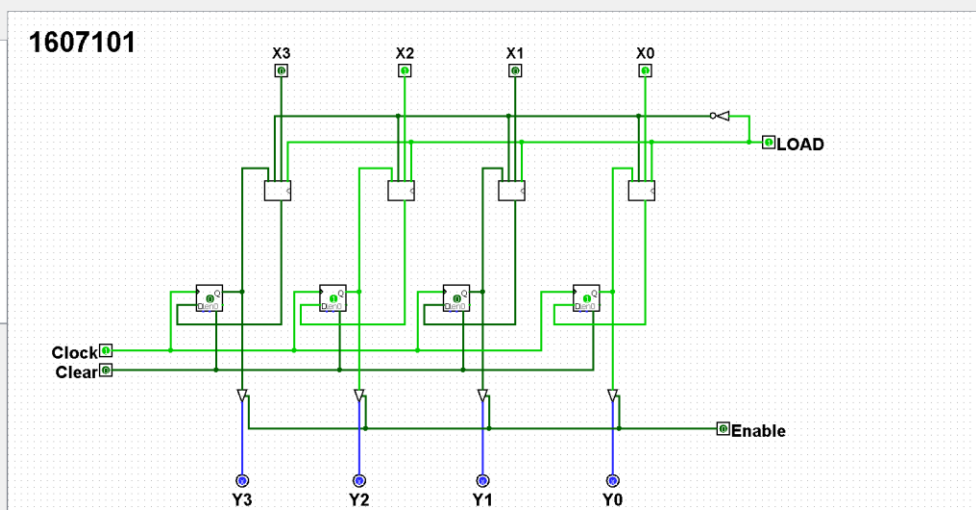


Fig. 2: Buffer Register

1607101*

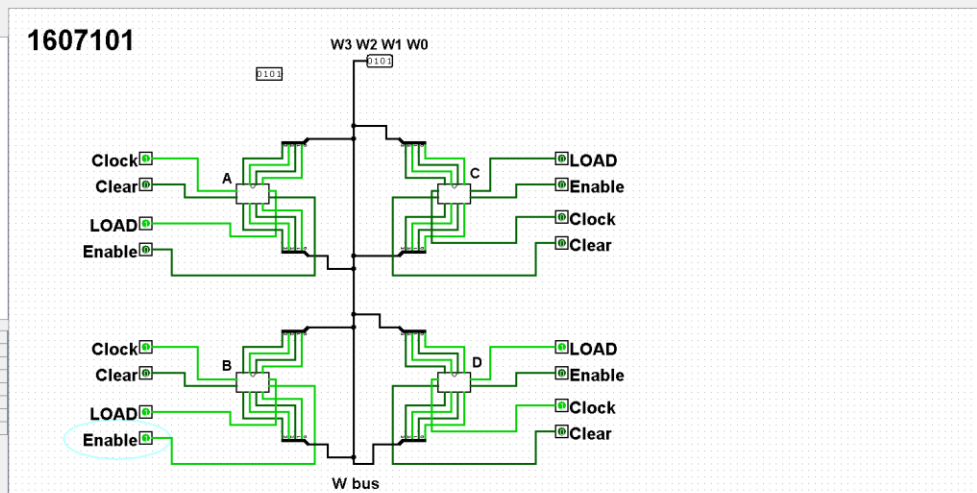
- 1607101_bus_connection
- 1607101_intermediate
- 1607101_buffer_register

Wiring

- Gates
- Plexers
- Arithmetic
- Memory
- Input/Output
- Base

Facing	Pin
Output?	East
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	Enable
Label Location	West
Label Font	SansSerif Bold 26

100%



1607101*

- 1607101_bus_connection
- 1607101_intermediate
- 1607101_buffer_register

Wiring

- Gates
- Plexers
- Arithmetic
- Memory
- Input/Output
- Base

Facing	Pin
Output?	West
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	Clock
Label Location	East
Label Font	SansSerif Bold 26

100%

