KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY

Department

Of

Computer Science and Engineering

SESSIONAL REPORT

On

Design of SAP-1 Architecture

Course No: CSE 4224

Course Title: Digital System Design

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Objectives:

The purpose of this project are given below:-

(i) To learn about SAP-1 computer.

(ii) To learn about different components of SAP-1 computer.

(iii) To design a SAP-1 computer using logisim.

Introduction:

The simple-as-possible (SAP-1) computer is a very basic model of micro processor explained by Albert Paul Malvino. The SAP-1 Design contains the basic necessities for a functional micro-processor. Its primary purpose is to develop basic understanding of how a microprocessor works interacts with memory and other parts of the system like input and output. The instruction set is very limited and simple. SAP-1 is the first state in the evaluation towards modern computers.

Fig-1 shows the architecture of SAP-1 a bus organised computer. All registers outputs to the 8 bus are three-state, this allows orderly transfer of data. All other register outputs are two state, these outputs continuously drive the boxes they are connected to.

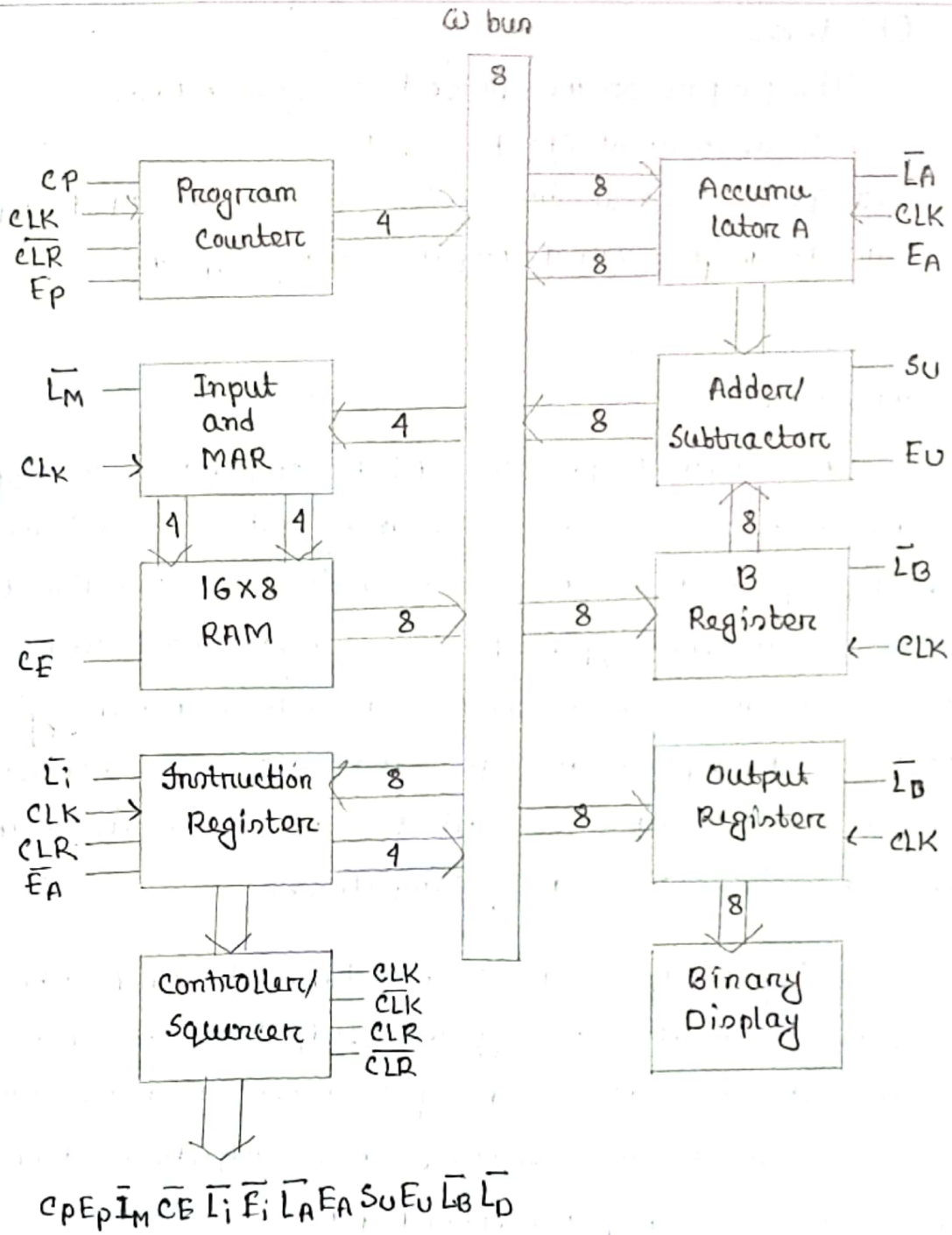


Figure 1: SAP-1 architecture

Program Counter:

The program counter is reset to 0000 before each computer run. When the computer run begins, the PC sends address 0000 to memory. The PC then is incremented to get 0001. After the first instruction is fetched and executed, the PC sends address 0001 to memory. Again the PC is incremented. After the second instruction is fetched and executed, the PC sends next address to memory. In this way, PC is keeping track of the next instruction to be fetched and executed.

Input and MAR:

It includes the address and data switch registers. These switch registers which are a part of input unit, allow to send 4 address bits and 8 data bits to the RAM. As recalled, instruction and data words are written into RAM before a computer run.

The MAR is part of SAP-1 memory. During a computer run, the address in PC is latched into MAR. A bit later, the MAR applies this 4-bit address to RAM where a read operation is performed.

The RAM:

The RAM is a 16X8 static TTL RAM. This allows one to store a program and data in the memory before computer run. During a computer run, RAM receives a 4-bit addresses from MAR and a read operation is performed. In this way, the data or instruction word in RAM is placed

on the W bus for use in some other part of the computer.

Instruction Register (IR):

IR is a part of control unit. To fetch an instruction the computer does a memory operation. This places the contents of addressed memory location on W bus. At the same time, IR is set up for loading on the next positive clock edge. The contents of the IR are split into two nibbles. The upper nibble is a two-state output that goes directly to the block labeled "control-sequencer". The other lower nibble is a three state output that is read into W bus when needed.

Control-sequencer:

Before each computer run a $\overline{CLR}$ is sent to PC and a CLR signal to the IR. This resets the PC to 0000 and wipes out the last instruction to the IR.

A clock signal in CLK is sent to all buffer registers, this synchronizes the operation of the computer, ensuring that all register transfer occur on the positive edge of common CLK signal.

The 12 bits that come out of controller from a word controlling the rest of the computer. The 12 wires carrying the control word are called the control bus.

The control word has the format of—

$$CON = C_P E_P \overline{L_M}\ \overline{CE}\quad \overline{L_I}\ \overline{E_I}\ \overline{L_A} E_A\quad S_U E_U \overline{L_B}\ \overline{L_O}$$

This word determines how the registers will react to the next positive clock edge.

Accumulator:

An accumulator (A) is a buffer register that stores intermediate answers. During a computer run. It has two outputs. The two-state output goes directly to adder-subtractor. The three-state output goes to the ω-bus. Therefore, the 8 bit accumulator word continuously drives the adder-subtractor. the same word appears on ω bus when E_A is high.

The Adder-Subtractor:

SAP-1 uses a 2's complement adder-subtractor. When S_u is low, the sum output of adder-subtractor is

$$S = A + B$$

when S_u is high, the difference appears

$$A = A + B'$$

It is asynchronous. When E_u is high, the contents appear on the ω bus.

B register:

The B register is another buffer register. It is used to in arithmetic operations. A low L_B and positive clock edge load the word on ω bus into B register. The two-state output of B register drives the adder-subtractor, supplying the number to be added or subtracted from the contents of the accumulator.

Output register:

At the end of computer run, the accumulator contains the answer to the problem being solved. When E_A is high and $\overline{L_O}$ is low the next positive clock edge loads the accumulator word into the output register.

The output register is often called an output port because processed data can leave the computer through this register.

Binary Display:

The binary display is a row of eight LEDs. Because each LED connects to one flip-flop of the output port, the binary display shows the contents of the output port.

Instruction set of SAP-1:

The SAP-1 instruction set follows:

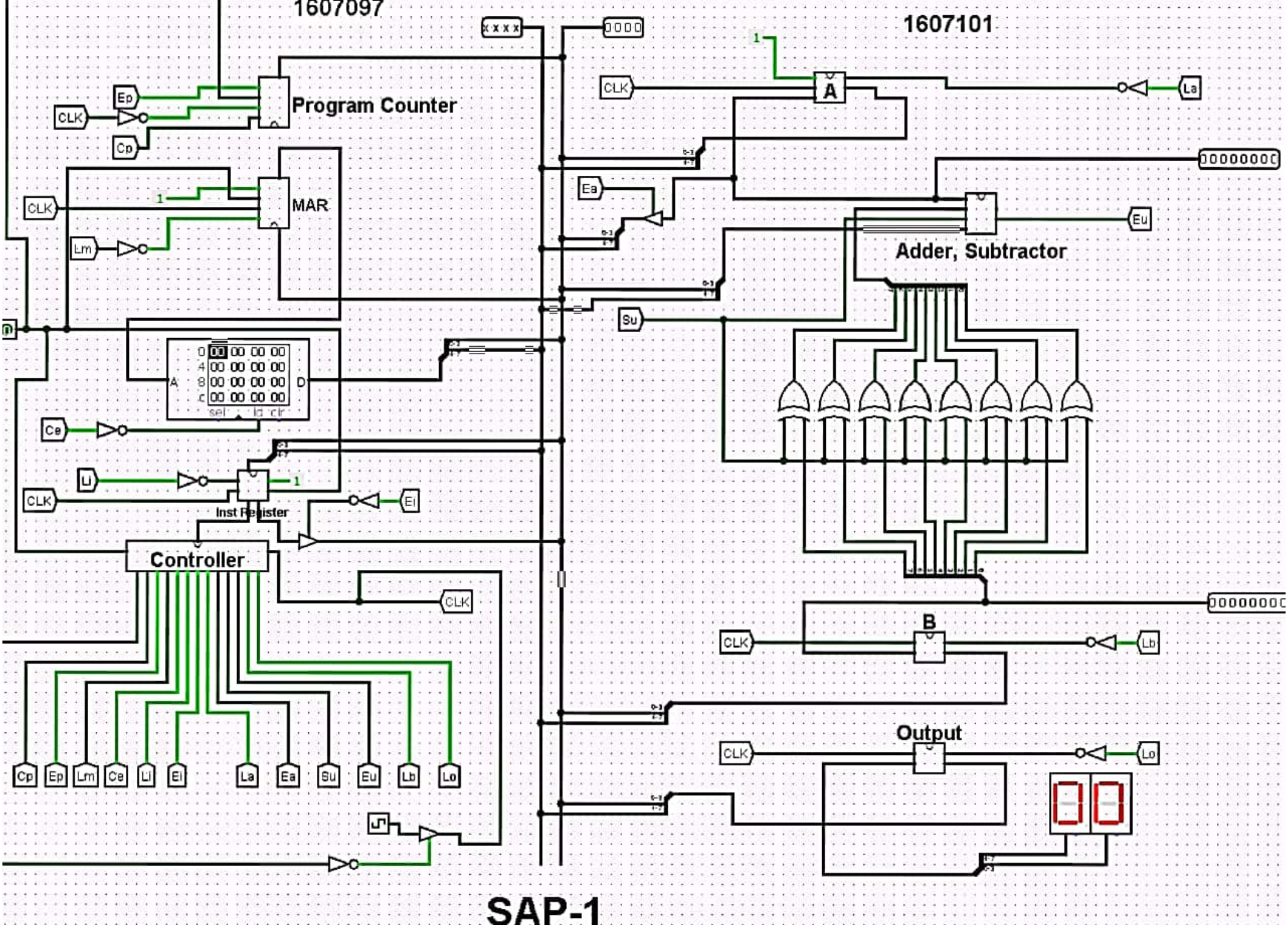
I. LDA: LDA stands for "Load the Accumulator". A complete LDA instruction includes the hexadecimal address of the data to be loaded.

II. ADD: A complete ADD instruction includes the address of the word to be ~~loaded~~ added. For instance, ADD 9H means "add the contents of memory location 9H to accumulation, replace the original contents of accumulator

III. SUB: A complete SUB instruction includes the address of word to be subtracted. For example, SUB CH means subtract the contents of memory locations CH from the content of the accumulator.

IV. OUT: The OUT instruction tells the SAP-1 computer to transfer the accumulator contents to the output port. Out is completed by itself, you do not have to include an address when using OUT because the instruction doesn't involve data in the memory.

V. HLT: HLT stands for halt. It tells the computer to stop processing data. HIT makes the end of a program. You must use a HLT instruction at the end of every SAP-1 program.



Conclusion:

In this project, we learnt about SAP-1 computer design process. We also learnt how to design every components of SAP-1 computer in Logisim. We implemented SAP-1 computer in Logisim using those components. Finally we ran a program in Logisim and checked the output using LEDs and display module.