in the name of God
FPGA Project
Phase4
LAN 802.11a-1999
Sharif University of Technology

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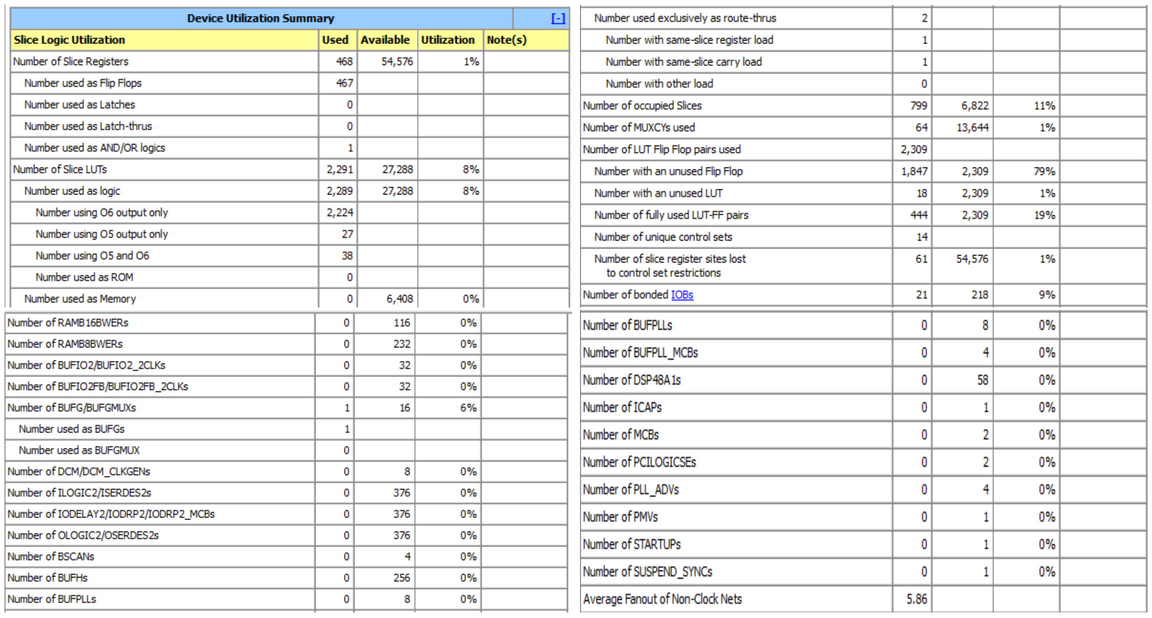
July 9, 2021

1 Introduction

In this project, the final goal was to implement the transmitter and the receiver side of the standard LAN802.11a-1999 in HDL Verilog. (Scrambler, Convlutiona Encoder and Data Inteleaver for TX side in their inverse for RX side.)
in this phase, i connected these modules together using piplining and conrolling techniques and FSM's to connect the modules was implemented in previous sections.

2 TX Side

Connectin the modules in this part of the project was easy; the modules that were implementin for the transmitter side does not have such a complexity that make it hard for us to implement them. i used just piplining techniques ti connect theis modules together and because one latency for each module in the tranmitter side, the final output (scrambled, coded, interleaved) from the tranmitter is come out with a latency of three clock cycle.
i use three local piplined reset to reset each of the three module when there is a new frame to transmite.
i also assumed that initial seed for scrambling is given by the MAC layer to this module(in the receiver i have assumed that this is 1011101). i also assumed that the MAC layer will give the length of pad pluse tail bits that are at the end of data part of frame. this is because that the MAC layers are cpu based system and doing this by them is better than to calculating by the hardware.
I also assumed that the DAC in the transmitter side works with a data rate of 2 time of the syste clock. it is beacuse that the transmitter in each clock receive one bit from the MAC layer and transmitt two bit from the convlutiona encoder. so we must handle this functionality to never lost any data. normally and DAC, we used some microcontroller that can work with frequencies of 100MHz that is ok with the maximom frequency of data generation rate of our syste(2(24) = 48MHz). so in each clock cycle, there is two bits of data out from the transmitter module.
there also may be some data out that are not real data's that means they must not transmite. i used a signa *AB_out_valid* to say that to the next module (the simulated serial link in this project) this is not data and don't transfer this data. notice to these approches, the transmiiter module was designed and implemented in FPGA and the recources used by it is listed in the following figures:



Device Utilization Summary [-]

Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	468	54,576	1%	
Number used as Flip Flops	467			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	1			
Number of Slice LUTs	2,291	27,288	8%	
Number used as logic	2,289	27,288	8%	
Number using O6 output only	2,224			
Number using O5 output only	27			
Number using O5 and O6	38			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number used exclusively as route-thrus	2			
Number with same-slice register load	1			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	799	6,822	11%	
Number of MUXCYs used	64	13,644	1%	
Number of LUT Flip Flop pairs used	2,309			
Number with an unused Flip Flop	1,847	2,309	79%	
Number with an unused LUT	18	2,309	1%	
Number of fully used LUT-FF pairs	444	2,309	19%	
Number of unique control sets	14			
Number of slice register sites lost to control set restrictions	61	54,576	1%	
Number of bonded IOBs	21	218	9%	
Number of RAMB16BWERs	0	116	0%	
Number of RAMB8BWERs	0	232	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	0	376	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	5.86			

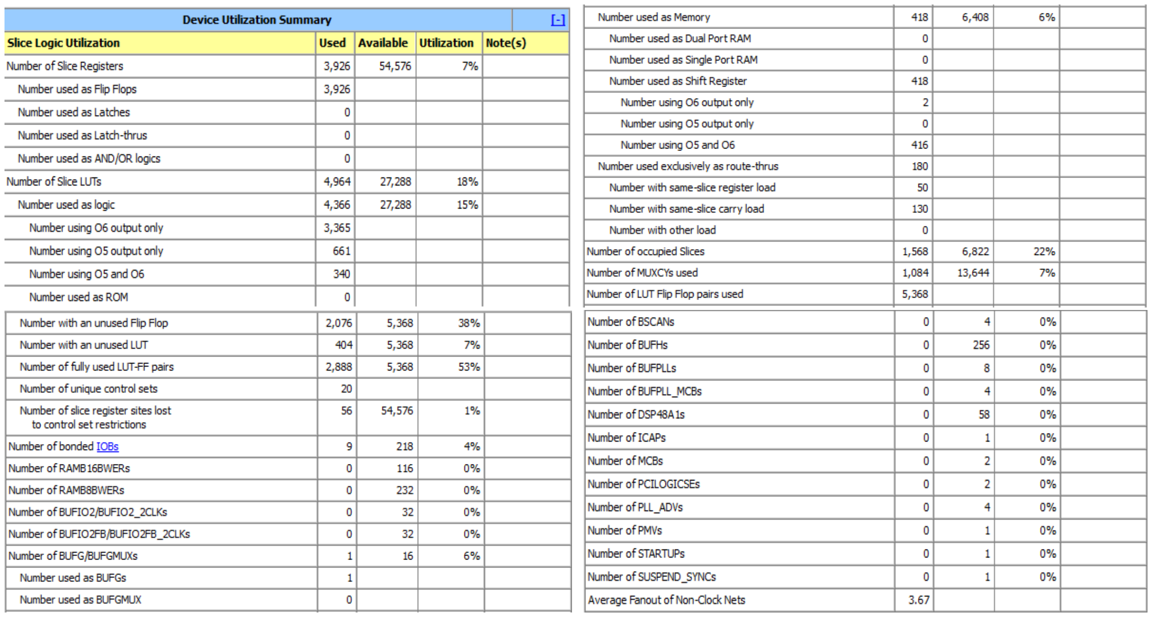
Figure 1: Recurces used in Transmitter

3 RX Side

In this part, i connected the deinterleaver, viterbi decoder, data descrambler modules together. as there was some complexity on the viterbi decoder, there was needed to handle the good handshaking between these modules to receive, deinterleav, decode and descrable the data bits of the frame. to do so, this handshking was more complec than in transmitter side beacause of complecicities on viterbi decoder.
at first m clock cycle, when the receiver detect that there is a new data (by seeing the preamble pattern), there take some clock cycles to decoder input valid data to descrambler module. the number of the clock cycles that it take fo the receiver to have valid data output is dependent to the rate of the signal field. in this project i have assummed that the rate in the receiver side is khnown(top modules before the deinterleaver modules detects the rate notice to the digital modulation has been used in received frame). this dependency to the rate is given in the following formula:

$$m = \begin{cases} 4\times 48+36+3+0=231 & rate=6MHz \\ 4\times 48+36+3+48=279 & rate=12MHz \\ 4\times 48+36+3+3\times 48=375 & rate=24MHz \end{cases}$$

the paramete m in the above formulas is the number of clock cycles that it takes for receiver to transmite a valid data (first bit of the signal field of the frame) to the output. this changeble rate-dependent laency is because the features and the correspondign latecies in viterbi decoder and data deinterleaver in RX side.
after this number of clock cycle (m) we have at each 48 clock cycle, 24 available data output. this is because of our viterbi decoder. as it was sain in the report document of phase2 of the project, the depth of the viterbi decoder is 48 and notice to the parameter $R=\frac{1}{2}$, there is 24 bit of available of data for each 48 bit of received data.
notice to the above approches, i designe my receiver for standard LAN802.1a-1999; you can see the recources was used by my module in the following figure:



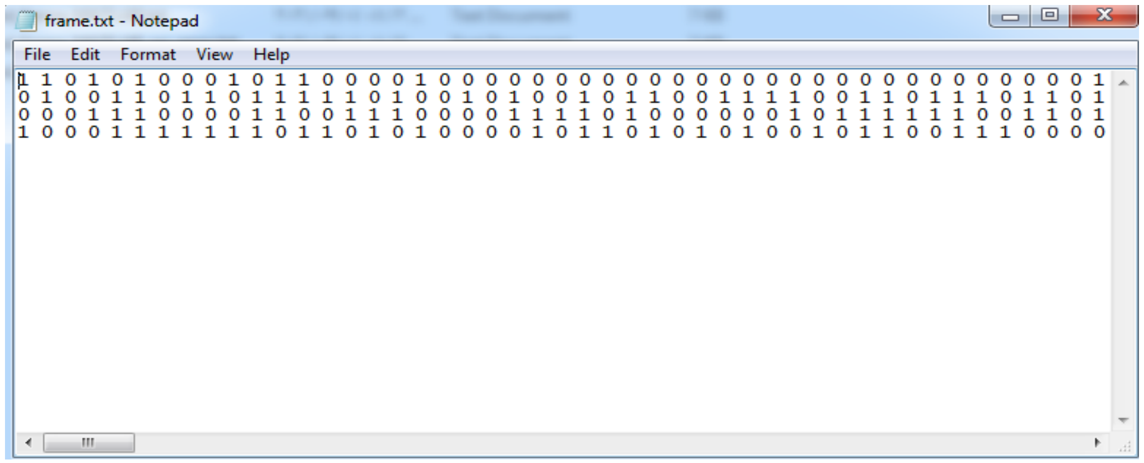
Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	3,926	54,576	7%	
Number used as Flip Flops	3,926			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	4,964	27,288	18%	
Number used as logic	4,366	27,288	15%	
Number using O6 output only	3,365			
Number using O5 output only	661			
Number using O5 and O6	340			
Number used as ROM	0			
Number used as Memory	418	6,408	6%	
Number used as Dual Port RAM	0			
Number used as Single Port RAM	0			
Number used as Shift Register	418			
Number using O6 output only	2			
Number using O5 output only	0			
Number using O5 and O6	416			
Number used exclusively as route-thrus	180			
Number with same-slice register load	50			
Number with same-slice carry load	130			
Number with other load	0			
Number of occupied Slices	1,568	6,822	22%	
Number of MUXCYs used	1,084	13,644	7%	
Number of LUT Flip Flop pairs used	5,368			
Number with an unused Flip Flop	2,076	5,368	38%	
Number with an unused LUT	404	5,368	7%	
Number of fully used LUT-FF pairs	2,888	5,368	53%	
Number of unique control sets	20			
Number of slice register sites lost to control set restrictions	56	54,576	1%	
Number of bonded IOBs	9	218	4%	
Number of RAMB16BWERs	0	116	0%	
Number of RAMB8BWERs	0	232	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.67			

Figure 2: Recurces used in Receiver

4 Result

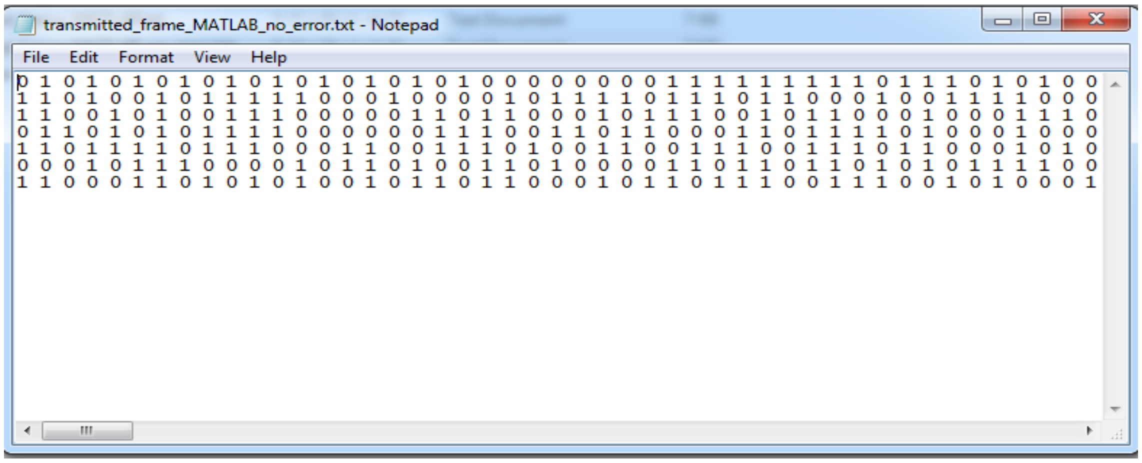
As there is three value for the rate, i built three diffrent frame to simulate the transmitter an the receiver notice to 6MHz, 12MHz and 24MHz rate. i added smoe noise in the simulated serial link in MATLAB to data to check the correctness of the viterbi decoder.(0.3% of bits of transmitted frame except the preamble ones). you can see the result of these simulations in the following figures:

4.1 rate = 1101(6MHz)



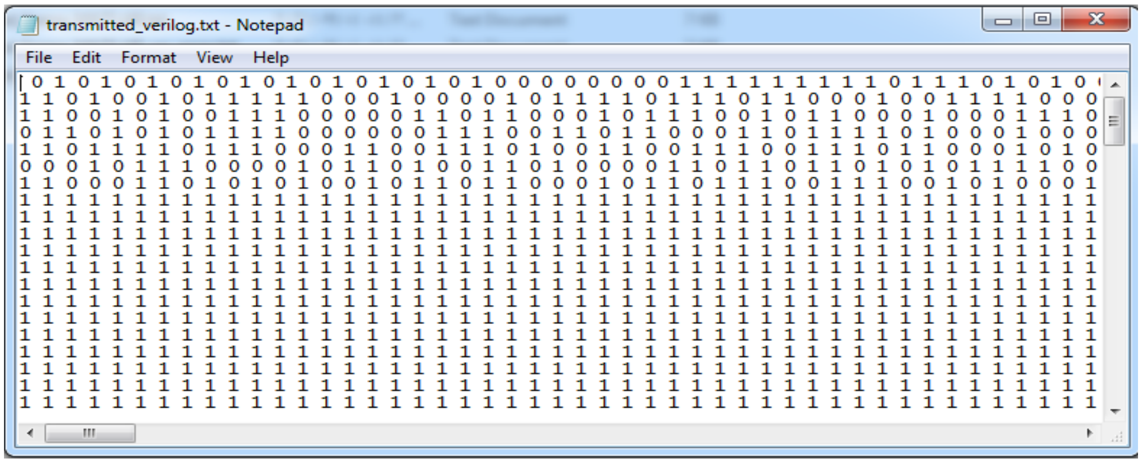
```
1 1 0 1 0 1 0 0 0 1 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
0 1 0 0 1 1 0 1 1 0 1 1 1 1 1 0 1 0 0 1 0 1 0 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1 0 1 1 1 0 1 1 0 1
0 0 0 1 1 1 0 0 0 0 1 1 0 0 1 1 1 0 0 0 0 1 1 1 1 0 1 0 0 0 0 0 0 1 0 1 1 1 1 1 1 0 0 1 1 0 1
1 0 0 0 1 1 1 1 1 1 1 0 1 1 0 1 0 1 0 0 0 0 1 0 1 1 0 1 0 1 0 1 0 0 1 0 1 1 0 0 1 1 1 0 0 0 0
```

Figure 3: Frame



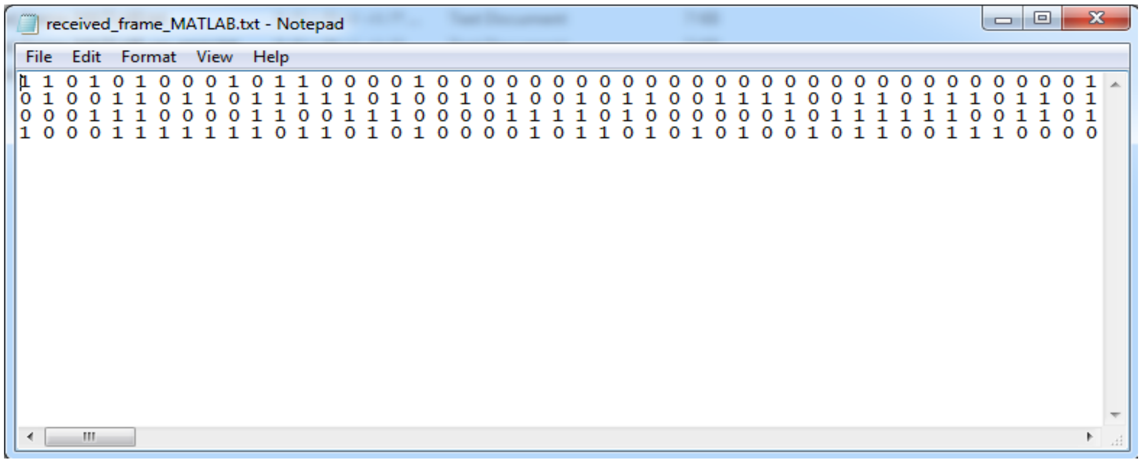
```
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 1 1 1 0 1 0 1 0 0
1 1 0 1 0 0 1 0 1 1 1 1 1 0 0 0 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 0 0 0 1 0 0 1 1 1 1 0 0 0
1 1 0 0 1 0 1 0 0 1 1 1 0 0 0 0 0 1 1 0 1 1 0 0 0 1 0 1 1 1 0 0 1 0 1 1 0 0 0 1 0 0 0 1 1 1 0
0 1 1 0 1 0 1 0 1 1 1 1 0 0 0 0 0 0 1 1 1 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1 1 1 0 1 0 0 0 1 0 0 0
1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 1 1 0 1 0 0 1 1 0 0 1 1 1 0 0 1 1 1 0 1 1 0 0 0 1 0 1 0
0 0 0 1 0 1 1 1 0 0 0 0 1 0 1 1 0 1 0 0 1 1 0 1 0 0 0 0 1 1 0 1 1 0 1 1 0 1 0 1 0 1 1 1 1 0 0
1 1 0 0 0 1 1 0 1 0 1 0 1 0 0 1 0 1 1 0 1 1 0 0 0 1 0 1 1 0 1 1 1 0 0 1 1 1 0 0 1 0 1 0 0 0 1
```

Figure 4: Transmitted Frame in MATLAB with no error



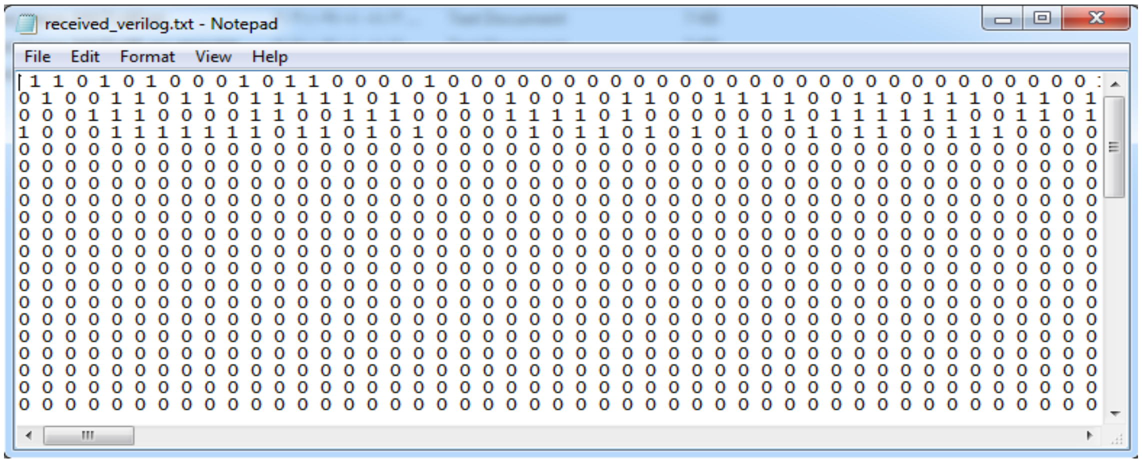
```
 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 1 1 1 0 1 0 1 0
1 1 0 1 0 0 1 0 1 1 1 1 1 0 0 0 1 0 0 0 0 1 0 1 1 1 1 0 1 1 1 0 1 1 0 0 0 1 0 0 1 1 1 1 0 0 0
1 1 0 0 1 0 1 0 0 1 1 1 0 0 0 0 0 1 1 0 1 1 0 0 0 1 0 1 1 1 0 0 1 0 1 1 0 0 0 1 0 0 0 1 1 1 0
0 1 1 0 1 0 1 0 1 1 1 1 0 0 0 0 0 0 1 1 1 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1 1 1 0 1 0 0 0 1 0 0 0
1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 1 1 0 1 0 0 1 1 0 0 1 1 1 0 0 1 1 1 0 1 1 0 0 0 1 0 1 0
0 0 0 1 0 1 1 1 0 0 0 0 1 0 1 1 0 1 0 0 1 1 0 1 0 0 0 0 1 1 0 1 1 0 1 1 0 1 0 1 0 1 1 1 1 0 0
1 1 0 0 0 1 1 0 1 0 1 0 1 0 0 1 0 1 1 0 1 1 0 0 0 1 0 1 1 0 1 1 1 0 0 1 1 1 0 0 1 0 1 0 0 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
```

Figure 5: Transmitted Frame in Verilog with no error



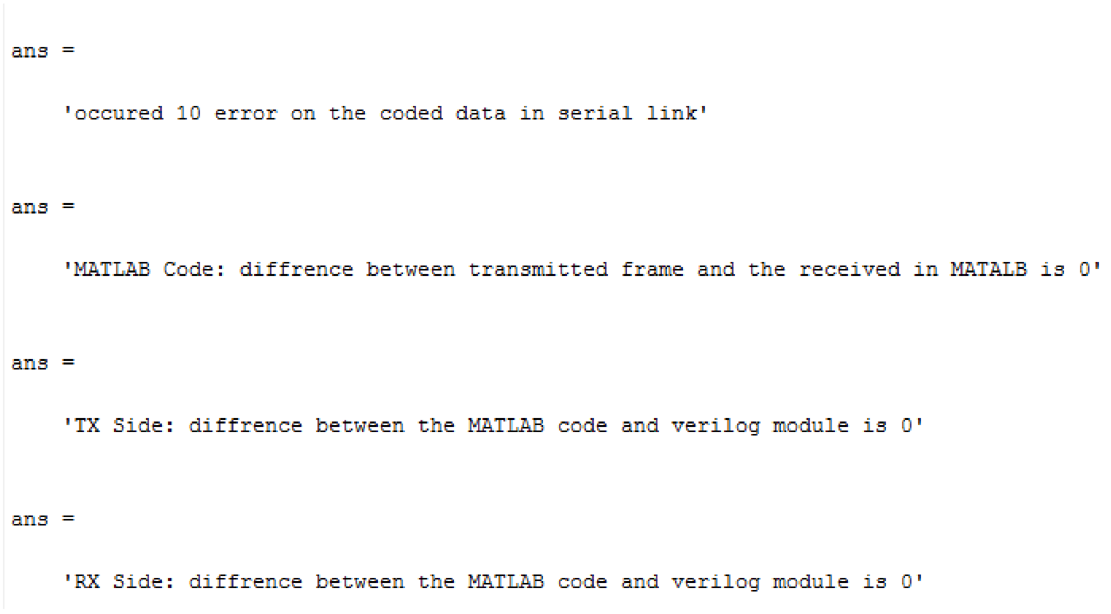
```
1 1 0 1 0 1 0 0 0 1 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
0 1 0 0 1 1 0 1 1 0 1 1 1 1 1 0 1 0 0 1 0 1 0 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1 0 1 1 1 0 1 1 0 1
0 0 0 1 1 1 0 0 0 0 1 1 0 0 1 1 1 0 0 0 0 1 1 1 1 0 1 0 0 0 0 0 0 1 0 1 1 1 1 1 1 0 0 1 1 0 1
1 0 0 0 1 1 1 1 1 1 1 0 1 1 0 1 0 1 0 0 0 0 1 0 1 1 0 1 0 1 0 1 0 0 1 0 1 1 0 0 1 1 1 0 0 0 0
```

Figure 6: Received Frame In MATLAB with corrected Errors



```
 1 1 0 1 0 1 0 0 0 1 0 1 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 1 0 0 1 1 0 1 1 0 1 1 1 1 1 0 1 0 0 1 0 1 0 0 1 0 1 1 0 0 1 1 1 1 0 0 1 1 0 1 1 1 0 1 1 0 1
0 0 0 1 1 1 0 0 0 0 1 1 0 0 1 1 1 0 0 0 0 1 1 1 1 0 1 0 0 0 0 0 0 1 0 1 1 1 1 1 1 0 0 1 1 0 1
1 0 0 0 1 1 1 1 1 1 1 0 1 1 0 1 0 1 0 0 0 0 1 0 1 1 0 1 0 1 0 1 0 0 1 0 1 1 0 0 1 1 1 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

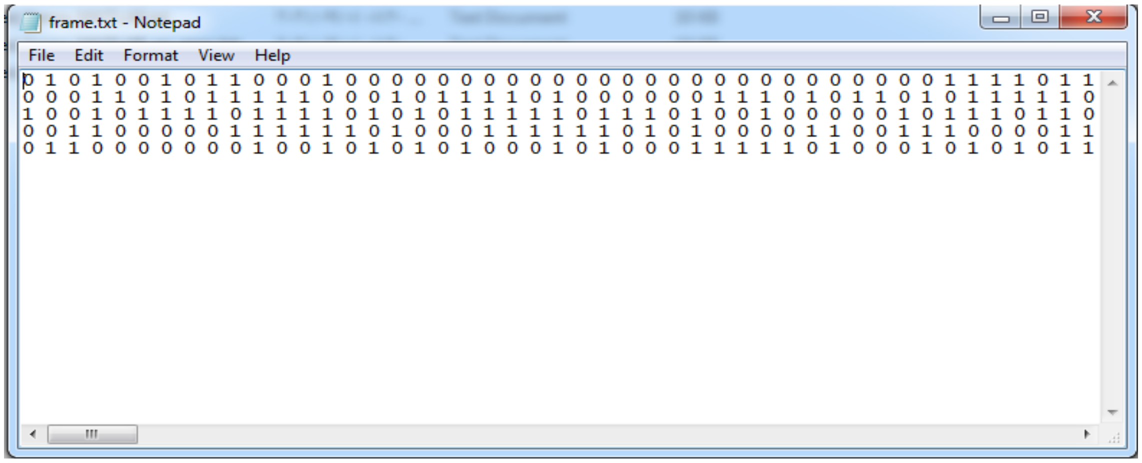
Figure 7: Received Frame In Verilog with corrected Errors



```
ans =

    'occured 10 error on the coded data in serial link'


ans =

    'MATLAB Code: diffrence between transmitted frame and the received in MATALB is 0'


ans =

    'TX Side: diffrence between the MATLAB code and verilog module is 0'


ans =

    'RX Side: diffrence between the MATLAB code and verilog module is 0'
```

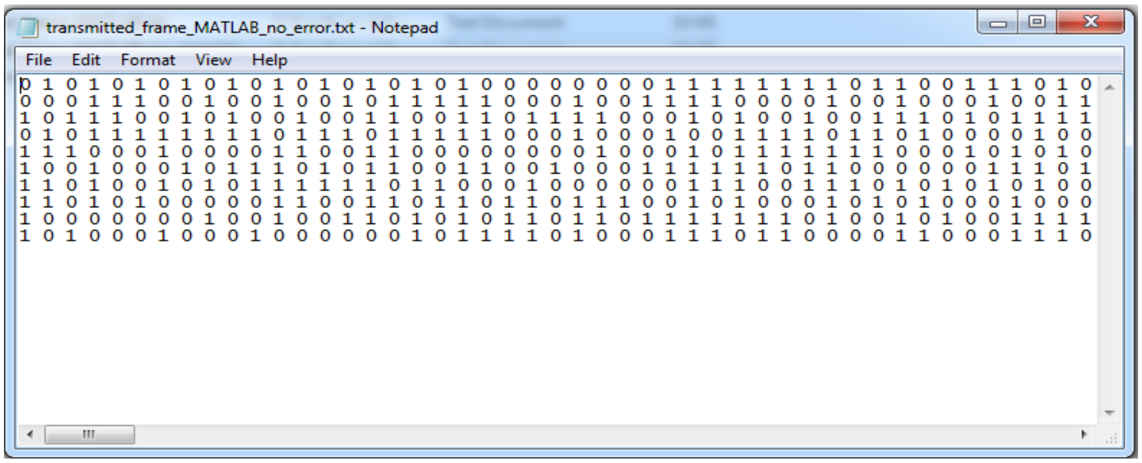
Figure 8: Compare the Result of MATLAB and Verilog in MATLAB

4.2 rate = 0101(12MHz)



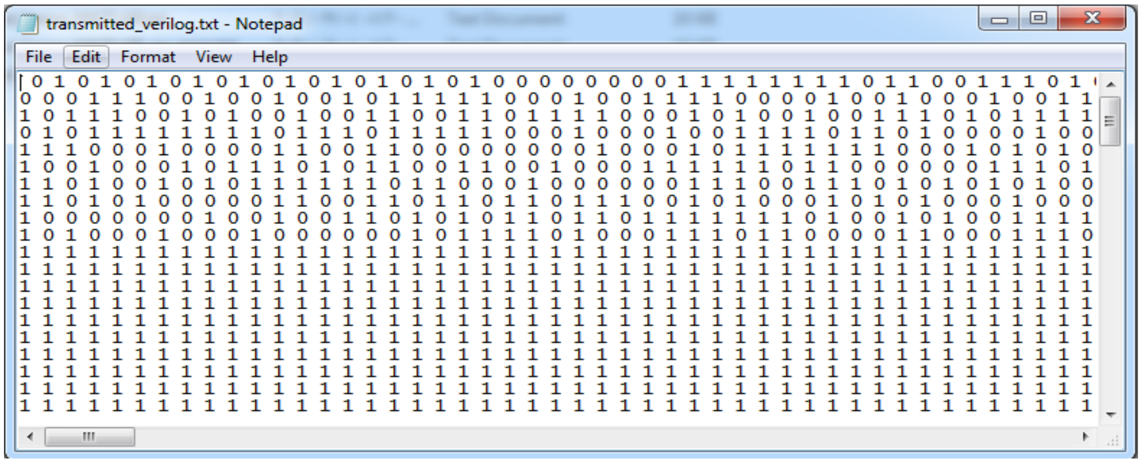
```
0 1 0 1 0 0 1 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 1 1
0 0 0 1 1 0 1 0 1 1 1 1 1 0 0 0 1 0 1 1 1 1 0 1 0 0 0 0 0 0 1 1 1 0 1 0 1 1 0 1 0 1 1 1 1 1 0
1 0 0 1 0 1 1 1 1 0 1 1 1 1 0 1 0 1 0 1 1 1 1 1 0 1 1 1 0 1 0 0 1 0 0 0 0 0 1 0 1 1 1 0 1 1 0
0 0 1 1 0 0 0 0 0 1 1 1 1 1 1 0 1 0 0 0 1 1 1 1 1 1 0 1 0 1 0 0 0 0 1 1 0 0 1 1 1 0 0 0 0 1 1
0 1 1 0 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 1 0 0 0 1 0 1 0 0 0 1 1 1 1 1 0 1 0 0 0 1 0 1 0 1 0 1 1
```

Figure 9: Frame


transmitted_frame_MATLAB_no_error.txt - Notepad
File Edit Format View Help

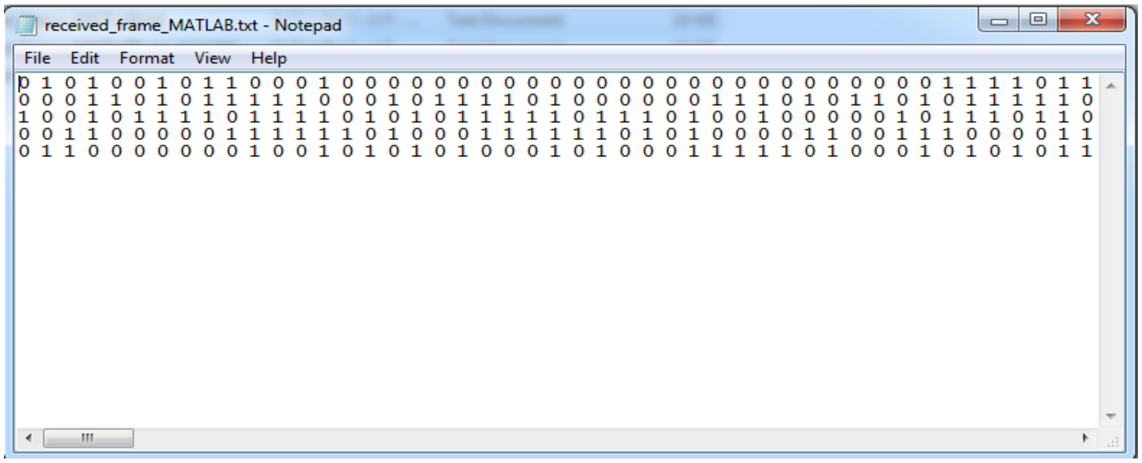
```
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 1 1 0 0 1 1 1 0 1 0
0 0 0 1 1 1 0 0 1 0 0 1 0 0 1 0 1 1 1 1 1 0 0 0 1 0 0 1 1 1 1 0 0 0 0 1 0 0 1 0 0 0 1 0 0 1 1
1 0 1 1 1 0 0 1 0 1 0 0 1 0 0 1 1 0 0 1 1 0 1 1 1 1 0 0 0 1 0 1 0 0 1 0 0 1 1 1 0 1 0 1 1 1 1
0 1 0 1 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 1 1 0 0 0 1 0 0 0 1 0 0 1 1 1 1 0 1 1 0 1 0 0 0 0 1 0 0
1 1 1 0 0 0 1 0 0 0 0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 1 0 0 0 1 0 1 1 1 1 1 1 1 0 0 0 1 0 1 0 1 0
1 0 0 1 0 0 0 1 0 1 1 1 0 1 0 1 1 0 0 1 1 0 0 1 0 0 0 1 1 1 1 1 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1
1 1 0 1 0 0 1 0 1 0 1 1 1 1 1 1 0 1 1 0 0 0 1 0 0 0 0 0 0 1 1 1 0 0 1 1 1 0 1 0 1 0 1 0 1 0 0
1 1 0 1 0 1 0 0 0 0 0 1 1 0 0 1 1 0 1 1 0 1 1 0 1 1 1 0 0 1 0 1 0 0 0 1 0 1 0 1 0 0 0 1 0 0 0
1 0 0 0 0 0 0 0 1 0 0 1 0 0 1 1 0 1 0 1 0 1 1 0 1 1 0 1 1 1 1 1 1 1 0 1 0 0 1 0 1 0 0 1 1 1 1
1 0 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 1 0 1 1 1 1 0 1 0 0 0 1 1 1 0 1 1 0 0 0 0 1 1 0 0 0 1 1 1 0
```

Figure 10: Transmitted Frame in MATLAB with no error



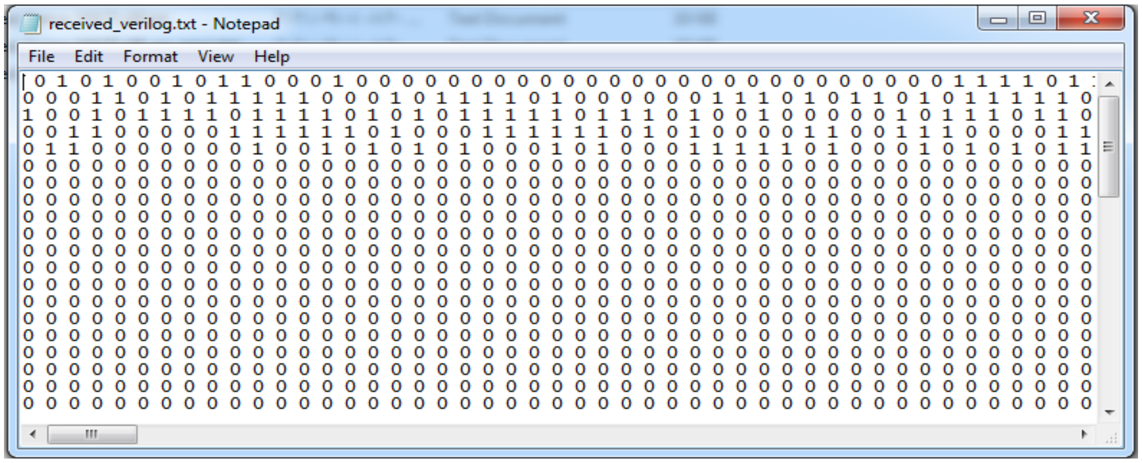
```
 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 1 1 0 0 1 1 1 0 1
0 0 0 1 1 1 0 0 1 0 0 1 0 0 1 0 1 1 1 1 1 0 0 0 1 0 0 1 1 1 1 0 0 0 0 1 0 0 1 0 0 0 1 0 0 1 1
1 0 1 1 1 0 0 1 0 1 0 0 1 0 0 1 1 0 0 1 1 0 1 1 1 1 0 0 0 1 0 1 0 0 1 0 0 1 1 1 0 1 0 1 1 1 1
0 1 0 1 1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 1 1 0 0 0 1 0 0 0 1 0 0 1 1 1 1 0 1 1 0 1 0 0 0 0 1 0 0
1 1 1 0 0 0 1 0 0 0 0 1 1 0 0 1 1 0 0 0 0 0 0 0 0 1 0 0 0 1 0 1 1 1 1 1 1 1 0 0 0 1 0 1 0 1 0
1 0 0 1 0 0 0 1 0 1 1 1 0 1 0 1 1 0 0 1 1 0 0 1 0 0 0 1 1 1 1 1 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1
1 1 0 1 0 0 1 0 1 0 1 1 1 1 1 1 0 1 1 0 0 0 1 0 0 0 0 0 0 1 1 1 0 0 1 1 1 0 1 0 1 0 1 0 1 0 0
1 1 0 1 0 1 0 0 0 0 0 1 1 0 0 1 1 0 1 1 0 1 1 0 1 1 1 0 0 1 0 1 0 0 0 1 0 1 0 1 0 0 0 1 0 0 0
1 0 0 0 0 0 0 0 1 0 0 1 0 0 1 1 0 1 0 1 0 1 1 0 1 1 0 1 1 1 1 1 1 1 0 1 0 0 1 0 1 0 0 1 1 1 1
1 0 1 0 0 0 1 0 0 0 1 0 0 0 0 0 0 1 0 1 1 1 1 0 1 0 0 0 1 1 1 0 1 1 0 0 0 0 1 1 0 0 0 1 1 1 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
```

Figure 11: Transmitted Frame in Verilog with no error



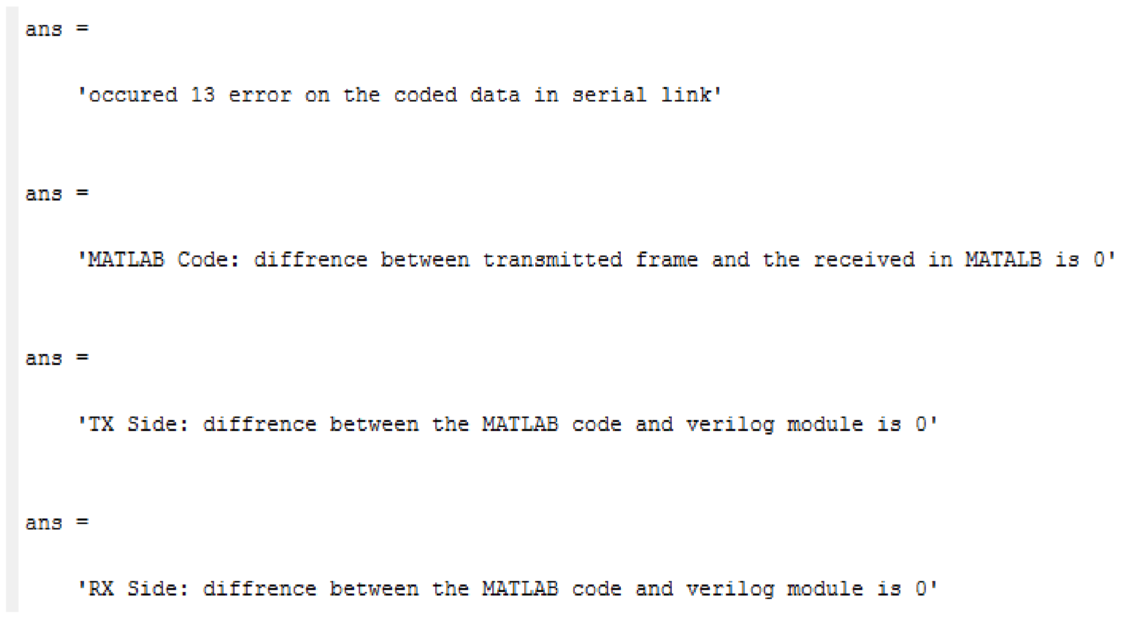
```
0 1 0 1 0 0 1 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 1 1
0 0 0 1 1 0 1 0 1 1 1 1 1 0 0 0 1 0 1 1 1 1 0 1 0 0 0 0 0 0 1 1 1 0 1 0 1 1 0 1 0 1 1 1 1 1 0
1 0 0 1 0 1 1 1 1 0 1 1 1 1 0 1 0 1 0 1 1 1 1 1 0 1 1 1 0 1 0 0 1 0 0 0 0 0 1 0 1 1 1 0 1 1 0
0 0 1 1 0 0 0 0 0 1 1 1 1 1 1 0 1 0 0 0 1 1 1 1 1 1 0 1 0 1 0 0 0 0 1 1 0 0 1 1 1 0 0 0 0 1 1
0 1 1 0 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 1 0 0 0 1 0 1 0 0 0 1 1 1 1 1 0 1 0 0 0 1 0 1 0 1 0 1 1
```

Figure 12: Received Frame In MATLAB with corrected Errors



```
 0 1 0 1 0 0 1 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 1
0 0 0 1 1 0 1 0 1 1 1 1 1 0 0 0 1 0 1 1 1 1 0 1 0 0 0 0 0 0 1 1 1 0 1 0 1 1 0 1 0 1 1 1 1 1 0
1 0 0 1 0 1 1 1 1 0 1 1 1 1 0 1 0 1 0 1 1 1 1 1 0 1 1 1 0 1 0 0 1 0 0 0 0 0 1 0 1 1 1 0 1 1 0
0 0 1 1 0 0 0 0 0 1 1 1 1 1 1 0 1 0 0 0 1 1 1 1 1 1 0 1 0 1 0 0 0 0 1 1 0 0 1 1 1 0 0 0 0 1 1
0 1 1 0 0 0 0 0 0 0 1 0 0 1 0 1 0 1 0 1 0 0 0 1 0 1 0 0 0 1 1 1 1 1 0 1 0 0 0 1 0 1 0 1 0 1 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

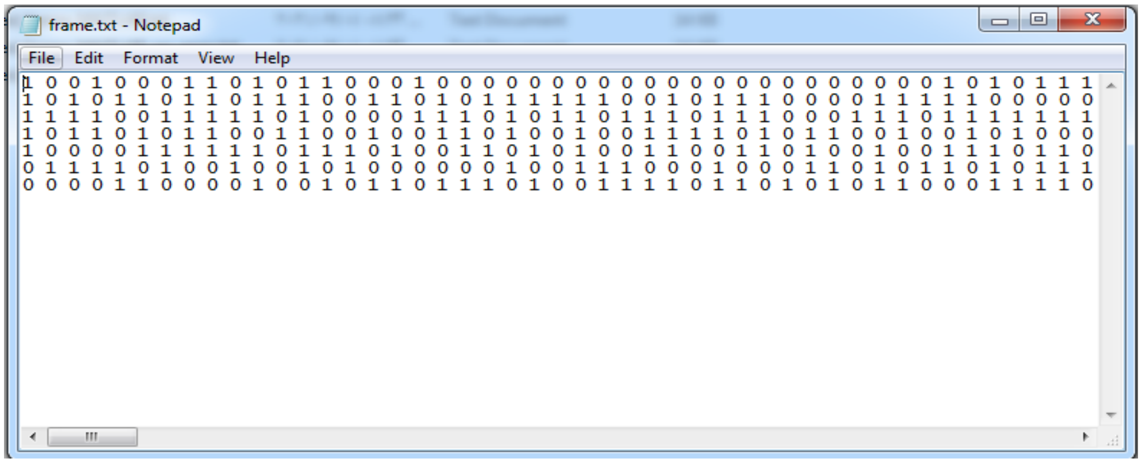
Figure 13: Received Frame In Verilog with corrected Errors



```
ans =

    'occured 13 error on the coded data in serial link'


ans =

    'MATLAB Code: diffrence between transmitted frame and the received in MATALB is 0'


ans =

    'TX Side: diffrence between the MATLAB code and verilog module is 0'


ans =

    'RX Side: diffrence between the MATLAB code and verilog module is 0'
```

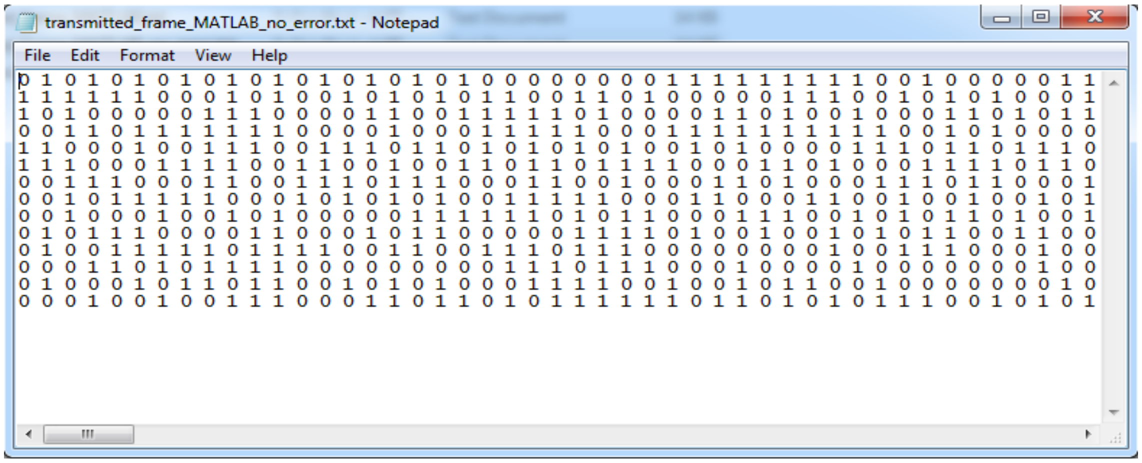
Figure 14: Compare the Result of MATLAB and Verilog in MATLAB

4.3 rate = 1001(24MHz)



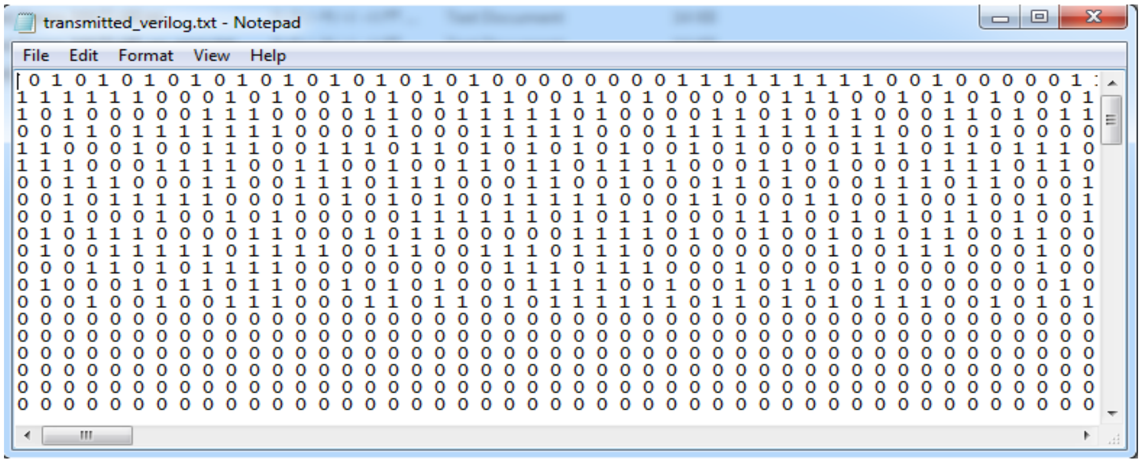
```
1 0 0 1 0 0 0 1 1 0 1 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 1 1
1 0 1 0 1 1 0 1 1 0 1 1 1 0 0 1 1 0 1 0 1 1 1 1 1 1 0 0 1 0 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 0 0
1 1 1 1 0 0 1 1 1 1 1 0 1 0 0 0 0 1 1 1 0 1 0 1 1 0 1 1 1 0 1 1 1 0 0 0 1 1 1 0 1 1 1 1 1 1 1
1 0 1 1 0 1 0 1 1 0 0 1 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 1 1 0 1 0 1 1 0 0 1 0 0 1 0 1 0 0 0
1 0 0 0 0 1 1 1 1 1 1 0 1 1 1 0 1 0 0 1 1 0 1 0 1 0 0 1 1 0 0 1 1 0 1 0 0 1 0 0 1 1 1 0 1 1 0
0 1 1 1 1 0 1 0 0 1 0 0 1 0 1 0 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0 0 1 1 0 1 0 1 1 0 1 0 1 1 1
0 0 0 0 1 1 0 0 0 0 1 0 0 1 0 1 1 0 1 1 1 0 1 0 0 1 1 1 1 0 1 1 0 1 0 1 0 1 1 0 0 0 1 1 1 1 0
```

Figure 15: Frame



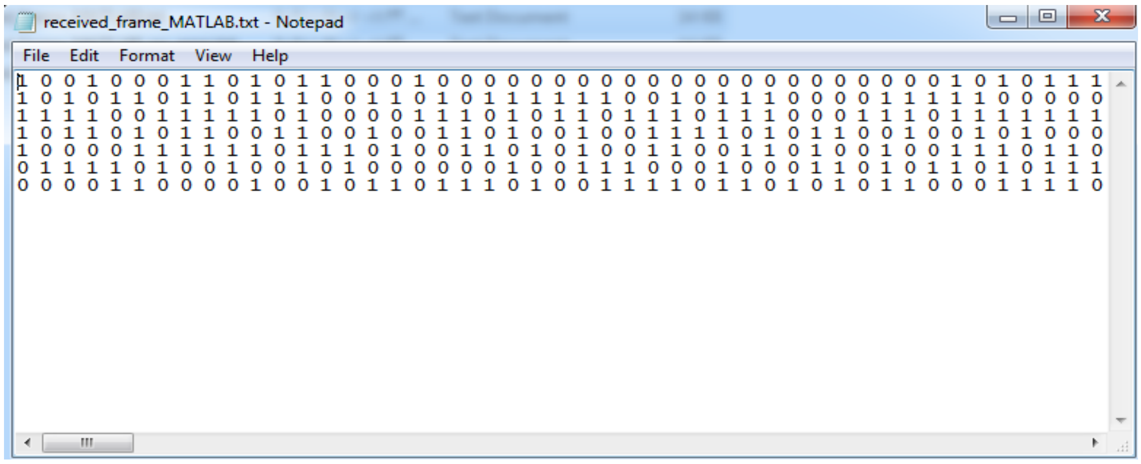
```
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 1 0 0 0 0 0 1 1
1 1 1 1 1 1 0 0 0 1 0 1 0 0 1 0 1 0 1 0 1 1 0 0 1 1 0 1 0 0 0 0 0 1 1 1 0 0 1 0 1 0 1 0 0 0 1
1 0 1 0 0 0 0 0 1 1 1 0 0 0 0 1 1 0 0 1 1 1 1 1 0 1 0 0 0 0 1 1 0 1 0 0 1 0 0 0 1 1 0 1 0 1 1
0 0 1 1 0 1 1 1 1 1 1 1 0 0 0 0 1 0 0 0 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 1 0 1 0 0 0 0
1 1 0 0 0 1 0 0 1 1 1 0 0 1 1 1 0 1 1 0 1 0 1 0 1 0 1 0 0 1 0 1 0 0 0 0 1 1 1 0 1 1 0 1 1 1 0
1 1 1 0 0 0 1 1 1 1 0 0 1 1 0 0 1 0 0 1 1 0 1 1 0 1 1 1 1 0 0 0 1 1 0 1 0 0 0 1 1 1 1 0 1 1 0
0 0 1 1 1 0 0 0 1 1 0 0 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 1 1 0 1 1 0 0 0 1
0 0 1 0 1 1 1 1 1 0 0 0 1 0 1 0 1 0 1 0 0 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 1 0 0 1 0 0 1 0 1
0 0 1 0 0 0 1 0 0 1 0 1 0 0 0 0 0 1 1 1 1 1 1 0 1 0 1 1 0 0 0 1 1 1 0 0 1 0 1 0 1 1 0 1 0 0 1
0 1 0 1 1 1 0 0 0 0 1 1 0 0 0 1 0 1 1 0 0 0 0 0 1 1 1 1 0 1 0 0 1 0 0 1 0 1 0 1 1 0 0 1 1 0 0
0 1 0 0 1 1 1 1 1 0 1 1 1 1 0 0 1 1 0 0 1 1 1 0 1 1 1 0 0 0 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0
0 0 0 1 1 0 1 0 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 0 1 1 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0
0 1 0 0 0 1 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0 0 1 1 1 1 0 0 1 0 0 1 0 1 1 0 0 1 0 0 0 0 0 0 0 1 0
0 0 0 1 0 0 1 0 0 1 1 1 0 0 0 1 1 0 1 1 0 1 0 1 1 1 1 1 1 0 1 1 0 1 0 1 0 1 1 1 0 0 1 0 1 0 1
```

Figure 16: Transmitted Frame in MATLAB with no error



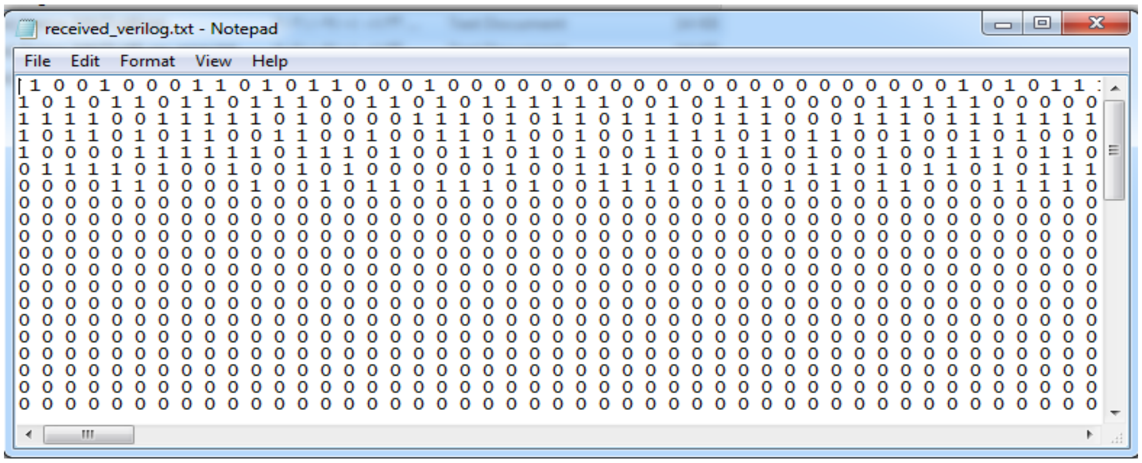
```
 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 1 0 0 0 0 0 1
1 1 1 1 1 1 0 0 0 1 0 1 0 0 1 0 1 0 1 0 1 1 0 0 1 1 0 1 0 0 0 0 0 1 1 1 0 0 1 0 1 0 1 0 0 0 1
1 0 1 0 0 0 0 0 1 1 1 0 0 0 0 1 1 0 0 1 1 1 1 1 0 1 0 0 0 0 1 1 0 1 0 0 1 0 0 0 1 1 0 1 0 1 1
0 0 1 1 0 1 1 1 1 1 1 1 0 0 0 0 1 0 0 0 1 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 1 0 1 0 0 0 0
1 1 0 0 0 1 0 0 1 1 1 0 0 1 1 1 0 1 1 0 1 0 1 0 1 0 1 0 0 1 0 1 0 0 0 0 1 1 1 0 1 1 0 1 1 1 0
1 1 1 0 0 0 1 1 1 1 0 0 1 1 0 0 1 0 0 1 1 0 1 1 0 1 1 1 1 0 0 0 1 1 0 1 0 0 0 1 1 1 1 0 1 1 0
0 0 1 1 1 0 0 0 1 1 0 0 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 1 1 0 1 1 0 0 0 1
0 0 1 0 1 1 1 1 1 0 0 0 1 0 1 0 1 0 1 0 0 1 1 1 1 1 0 0 0 1 1 0 0 0 1 1 0 0 1 0 0 1 0 0 1 0 1
0 0 1 0 0 0 1 0 0 1 0 1 0 0 0 0 0 1 1 1 1 1 1 0 1 0 1 1 0 0 0 1 1 1 0 0 1 0 1 0 1 1 0 1 0 0 1
0 1 0 1 1 1 0 0 0 0 1 1 0 0 0 1 0 1 1 0 0 0 0 0 1 1 1 1 0 1 0 0 1 0 0 1 0 1 0 1 1 0 0 1 1 0 0
0 1 0 0 1 1 1 1 1 0 1 1 1 1 0 0 1 1 0 0 1 1 1 0 1 1 1 0 0 0 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0
0 0 0 1 1 0 1 0 1 1 1 1 0 0 0 0 0 0 0 0 0 1 1 1 0 1 1 1 0 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 1 0 0
0 1 0 0 0 1 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0 0 1 1 1 1 0 0 1 0 0 1 0 1 1 0 0 1 0 0 0 0 0 0 0 1 0
0 0 0 1 0 0 1 0 0 1 1 1 0 0 0 1 1 0 1 1 0 1 0 1 1 1 1 1 1 0 1 1 0 1 0 1 0 1 1 1 0 0 1 0 1 0 1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

Figure 17: Transmitted Frame in Verilog with no error



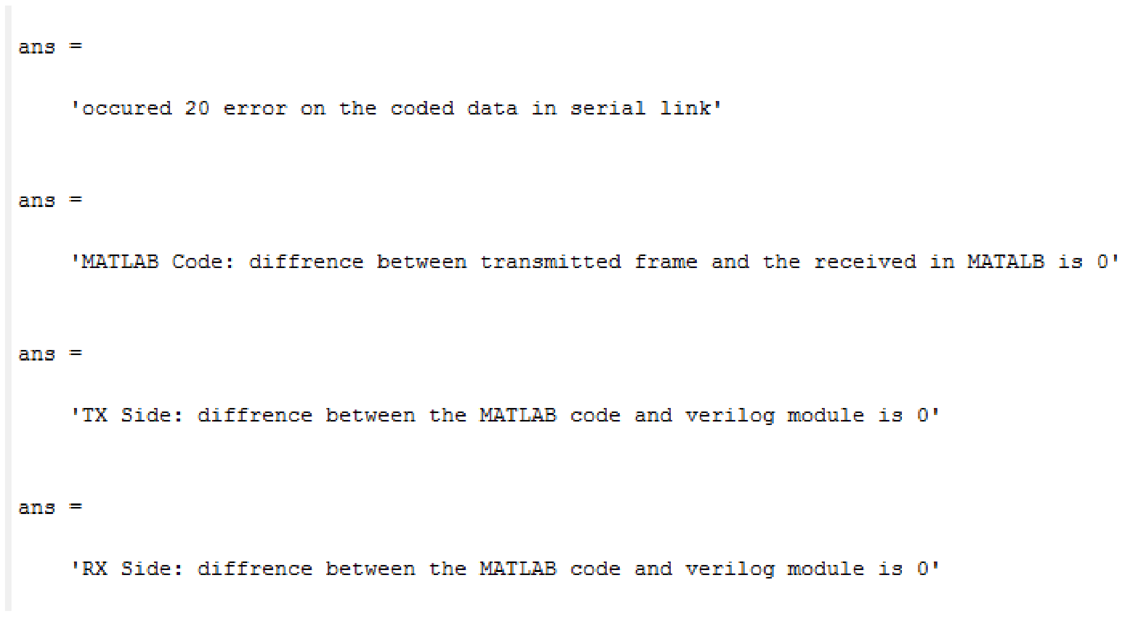
```
1 0 0 1 0 0 0 1 1 0 1 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 1 1
1 0 1 0 1 1 0 1 1 0 1 1 1 0 0 1 1 0 1 0 1 1 1 1 1 1 0 0 1 0 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 0 0
1 1 1 1 0 0 1 1 1 1 1 0 1 0 0 0 0 1 1 1 0 1 0 1 1 0 1 1 1 0 1 1 1 0 0 0 1 1 1 0 1 1 1 1 1 1 1
1 0 1 1 0 1 0 1 1 0 0 1 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 1 1 0 1 0 1 1 0 0 1 0 0 1 0 1 0 0 0
1 0 0 0 0 1 1 1 1 1 1 0 1 1 1 0 1 0 0 1 1 0 1 0 1 0 0 1 1 0 0 1 1 0 1 0 0 1 0 0 1 1 1 0 1 1 0
0 1 1 1 1 0 1 0 0 1 0 0 1 0 1 0 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0 0 1 1 0 1 0 1 1 0 1 0 1 1 1
0 0 0 0 1 1 0 0 0 0 1 0 0 1 0 1 1 0 1 1 1 0 1 0 0 1 1 1 1 0 1 1 0 1 0 1 0 1 1 0 0 0 1 1 1 1 0
```

Figure 18: Received Frame In MATLAB with corrected Errors



```
1 0 0 1 0 0 0 1 1 0 1 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 1
1 0 1 0 1 1 0 1 1 0 1 1 1 0 0 1 1 0 1 0 1 1 1 1 1 1 0 0 1 0 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 0 0
1 1 1 1 0 0 1 1 1 1 1 0 1 0 0 0 0 1 1 1 0 1 0 1 1 0 1 1 1 0 1 1 1 0 0 0 1 1 1 0 1 1 1 1 1 1 1
1 0 1 1 0 1 0 1 1 0 0 1 1 0 0 1 0 0 1 1 0 1 0 0 1 0 0 1 1 1 1 0 1 0 1 1 0 0 1 0 0 1 0 1 0 0 0
1 0 0 0 0 1 1 1 1 1 1 0 1 1 1 0 1 0 0 1 1 0 1 0 1 0 0 1 1 0 0 1 1 0 1 0 0 1 0 0 1 1 1 0 1 1 0
0 1 1 1 1 0 1 0 0 1 0 0 1 0 1 0 0 0 0 0 0 1 0 0 1 1 1 0 0 0 1 0 0 0 1 1 0 1 0 1 1 0 1 0 1 1 1
0 0 0 0 1 1 0 0 0 0 1 0 0 1 0 1 1 0 1 1 1 0 1 0 0 1 1 1 1 0 1 1 0 1 0 1 0 1 1 0 0 0 1 1 1 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

Figure 19: Received Frame In Verilog with corrected Errors



```
ans =

    'occured 20 error on the coded data in serial link'


ans =

    'MATLAB Code: diffrence between transmitted frame and the received in MATALB is 0'


ans =

    'TX Side: diffrence between the MATLAB code and verilog module is 0'


ans =

    'RX Side: diffrence between the MATLAB code and verilog module is 0'
```

Figure 20: Compare the Result of MATLAB and Verilog in MATLAB