Designing RS Decoder for DVB-T Receivers

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DVB-T

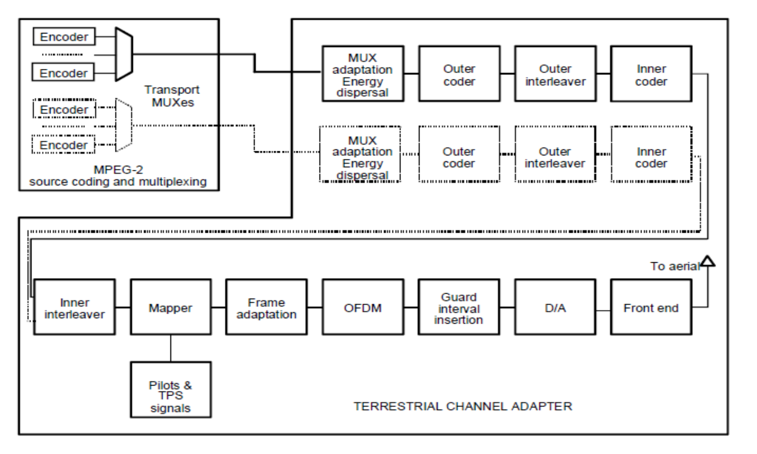

Figure: Functional Block Diagram of DVB-T System

RS Decoder
DVB-T Structure

- using RS(255, 239)
- DVB-T Structure of RS Decoder

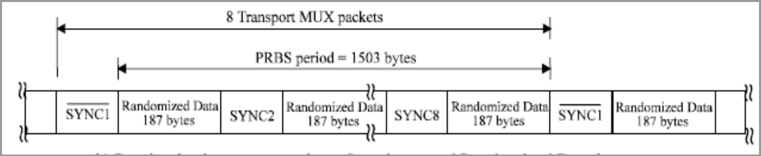

Figure: DVB-T Structure

- every 188 bytes of data is followe by 51 zero bytes in TX side
- Now the coding is done by Trnasmitter

RS Decoder

Decoder Structure

Decoder Structure

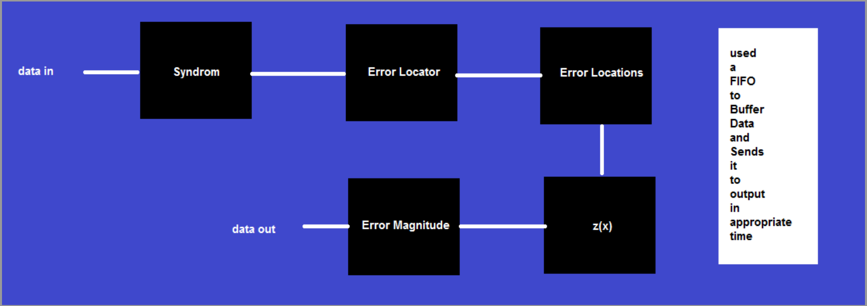

Figure: Decoder Structure

Syndrom

- in Rx side we have the following polynomial:

$$f(x) = a_{254}x^{254} + a_{253}x^{253} + \cdots + a_0x^0$$

- $S_1 = f(\alpha^1), S_2 = f(\alpha^2), \ldots, S_{16} = f(\alpha^{16})$
- all $+$ and $.$ operations is done in $GF(2^8)$
- If all S are zero, it means that there is no error in frame

Error Locator($\sigma(x)$)

- we calculate $sigma(x)$ using $S_1, S_2, \ldots, S_16$
- It is a polynomial at least dergree 8:

$$\sigma(x) = \sigma_8 x^8 + \sigma_7 x^7 + \cdots + \sigma_1 x + 1$$

- the degree of $Sigma(x)$ shows the number of error in a frame
- so decoder can just correct 8 bytes of error in each frame.
- the performance of the system increase using outer interleaver. now there is possible that 100 sequential frames becomes noisy and the decoder can correct all of them!!!

Error Locations

- calculate the location of errors using $\sigma(x)$
- if α^w is a root of $\sigma(x)$, it means the the w.th of the frame is noisy.
- we just need to calculate $\sigma(\alpha^1), \sigma(\alpha^2), \ldots, \sigma(\alpha^{255})$

$z(x)$ & Error Magnitude

- we calculate $z(x)$ with $S_1, S_2, \ldots, S_{16}$ and $\sigma(x)$ and also error locations.
- if the bytes in locations $l_1, l_2, l_3, \ldots l_8$ are noisy, ther the error magnitude for the byte in location l_1 is:

$$EM(l_1) = \frac{z(\alpha^{l_1})}{(1+\alpha^{l_1-l_2})(1+\alpha^{l_1-l_3})\ldots(1+\alpha^{l_1-l_8})}$$

- the correct byte at location l_1 is:

$$corrected(l_1) = EM(l_1) + received(l_1)$$

- all operations are done in $GF(2^8)$

Diffrent Algorithms

- On designing every digital system:
  1. power
  2. speed
  3. area
- Different algorithms
  1. GZP Algorithm
     - a parallel algorithm
     - high speed
     - use large area
  2. BM algorithm
     - a serial algorithm
     - satisfy speed we need
     - use smaller area than GZP

Results

Spartan6 Family, XC6SLX45 Device, XSG324 Package

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	1,498	54,576	2%	
Number used as Flip Flops	1,485			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	13			
Number of Slice LUTs	9,646	27,288	35%	
Number used as logic	4,192	27,288	15%	
Number using O6 output only	3,417			
Number using O5 output only	37			
Number using O5 and O6	738			
Number used as ROM	0			
Number used as Memory	5,420	6,408	84%	

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Number used as Dual Port RAM	5,216			
Number using O6 output only	5,216			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as Single Port RAM	144			
Number using O6 output only	144			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as Shift Register	60			
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	60			
Number used exclusively as route-thrus	34			

Number used exclusively as route-thrus	34			
Number with same-slice register load	14			
Number with same-slice carry load	20			
Number with other load	0			
Number of occupied Slices	3,047	6,822	44%	
Number of MUXCYs used	688	13,644	5%	
Number of LUT Flip Flop pairs used	10,002			
Number with an unused Flip Flop	8,619	10,002	86%	
Number with an unused LUT	356	10,002	3%	
Number of fully used LUT-FF pairs	1,027	10,002	10%	
Number of unique control sets	32			
Number of slice register sites lost to control set restrictions	91	54,576	1%	
Number of bonded IOBs	18	218	8%	

Number of RAMB16BWERs	0	116	0%	
Number of RAMB8BWERs	0	232	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	0	376	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	

Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	7.17			

Refrences

- DVB-T Standard
- **Error Control Coding:** fundumental and applications, SHU LIN \ DANIEL J.COSTELLO,Jr.
- Reed Solomon.pdf
- Master Thesis.pdf
- GENERIC REES SOLOMON ENCODER.pdf
- FPGA implementation of Reed Solomon codec for 40Gbps Forward Erro.pdf
- 10.1.1.403.6859.pdf
- 08.4_3.pdf


Thank You