## New Developments for Real Time Plasma Control System of TCV Tokamak based on FPGA

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Abstract—The vertical instability problem of highly-elongated plasmas has been investigated. A reduced-order model for control purpose has been derived from the full-order plasma RZIP model. Based on reduced model, an optimal control has been designed which gives better performance than a legacy PID control in the presence of measurement noise. The control algorithm is programmed in user-friendly Matlab-Simulink environment. The VHDL code is generated automatically with HDL coder. The control algorithm has been implemented into a COTS FPGA-based system. Hardware in the loop simulation has been performed to test the algorithm in the real world.

## I. INTRODUCTION

 $T^{
m HE}$  Tokamak is currently the most promising configuration to obtain controlled nuclear fusion energy. The Tokamak à Configuration Variable (TCV) has extensive plasma control possibilities thanks to an extremely flexible set of actuators that consists of poloidal field (PF) coils, gas valves, electron cyclotron (EC) powers and launchers. There are 16 independently powered PF coils that control plasma shape and position. This leads to a unique shaping capability with high elongation and triangularity [1]. High elongation is favourable as it increases energy stored in the plasma, but it also leads to the instability of the plasma vertical position [2]. A set of invessel coils, driven by a fast power supply which requires a control bandwidth of 100 kHz, is used to stabilize the vertical position. An optimal control for the plasma vertical stability was designed using a reduced-order model which has been derived from the TCV rigid displacement full-order model (RZIP) [3].

## II. RESULTS AND IMPLEMENTATION

The optimal control presented in this paper is a combination of a Kalman observer and a state feedback control. The control law is synthesized to minimize the cost function (1) subject to dynamic constraint (2)

$$\min_{u} J = \int_{T_{i}}^{T_{f}} [(y_{ref} - y)^{T} Q(y_{ref} - y) + u^{T} Ru] dt$$
 (1)

subject to

$$\begin{cases} \dot{x} = Ax + Bu + v \\ v = Cx + w \end{cases} \tag{2}$$

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where y is the plasma vertical position,  $y_{ref}$  is the vertical position reference, Q and R are weighting matrices, v is system noise, w is measurement noise, x is system state vector.

The optimal control is compared with a legacy PID control in Fig. 1. While both controls present good tracking of reference, the optimal control is less sensitive to measurement noise

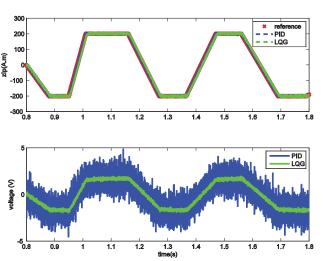


Fig. 1. Comparison between the PID control (blue) and the optimal LQG control (green).

The controller is implemented on a Field Programmable Gate Array (FPGA) chip. FPGAs are reconfigurable integrated circuits consisting of elementary cells and interconnections that are fully programmable by the end user to build specific hardware architectures. The massive parallelism computation capability of a FPGA is suitable to process large amounts of data rapidly. As no data is transferred to an external PC, the control algorithm executes with very low latency. Hence, the power and flexibility of FPGAs is now being recognized and used within the fusion community [4]. However, programming FPGA using VHDL (Very High Speed Integrated Circuit Hardware Description Language) hand-written code is notoriously difficult for non FPGA-expert physics users. This issue was bypassed by using Matlab-Simulink and the HDL coder package. The control algorithms are designed in userfriendly Matlab-Simulink environment, and tested in simulation.

Figure 2 shows the Simulink model used for code generation with Xilinx System Generator [5]. The *System Generator* token block is used to specify how code generation and simulation should be handled. The two blocks *Gateway In-Out* define Xilinx portion of Simulink model, i.e. VHDL

codes are only generated for Simulink blocks that are between these two blocks.

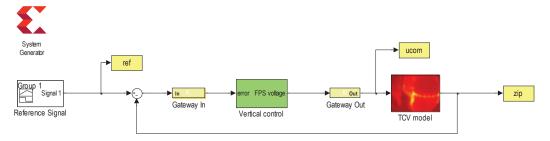


Fig. 2. Simulink model for code generation.

The VHDL codes are generated automatically then compiled into a configuration ".bit" file and implemented on the FPGA. The prototype system consists of the COTS components which are the Spartan 6 FPGA, 12-bit resolution A/D and D/A converter cards and can result latency of <5us even using what is essentially a commercial FPGA demonstration board.

The developed controller was found fully functional by performing FPGA-in-the-Loop (FIL) verification. Figure 3 shows the Simulink model used for testing the control algorithm in the real world. The FIL block generated from HDL code provides the communication interface between the FPGA and the Simulink model. When the simulation is run, firstly the configuration "bit" file is uploaded to FPGA board via JTAG cable, and then during simulation the data exchange between the hardware and the Simulink model is performed by the Ethernet cable.

The results are illustrated in Fig. 4 showing that the control algorithm behaved as expected in the real world.

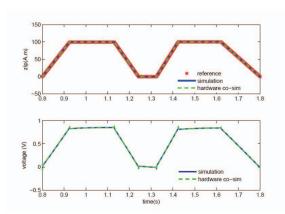


Fig. 4. Comparison between simulation result (blue -) and that of hardware (green --).

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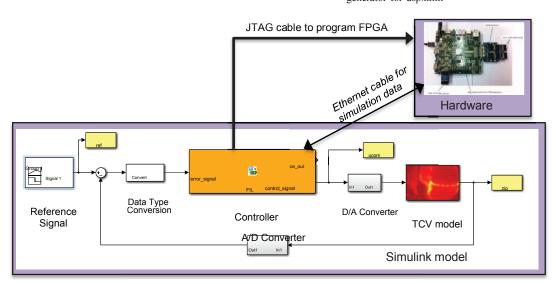


Fig. 3. Simulink model for Hardware in the loop verification.