ATCA digital controller hardware for vertical stabilization of plasmas in tokamaks

A. J. N. Batista, J. Sousa, and C. A. F. Varandas
Associação EURATOM/IST, Centro de Fusão Nuclear, Avenida Rovisco Pais 1, 1049-001 Lisbon, Portugal

(Received 6 May 2006; presented on 11 May 2006; accepted 2 June 2006; published online 16 October 2006)

The efficient vertical stabilization (VS) of plasmas in tokamaks requires a fast reaction of the VS controller, for example, after detection of edge localized modes (ELM). For controlling the effects of very large ELMs a new digital control hardware, based on the Advanced Telecommunications Computing Architecture™ (ATCA), is being developed aiming to reduce the VS digital control loop cycle (down to an optimal value of 10 μs) and improve the algorithm performance. The system has 1 ATCA™ processor module and up to 12 ATCA™ control modules, each one with 32 analog input channels (12 bit resolution), 4 analog output channels (12 bit resolution), and 8 digital input/output channels. The Aurora™ and PCI Express™ communication protocols will be used for data transport, between modules, with expected latencies below 2 μs. Control algorithms are implemented on a ix86 based processor with 6 Gflops and on field programmable gate arrays with 80 GMACS, interconnected by serial gigabit links in a full mesh topology. © *2006 American Institute of Physics.* [DOI: 10.1063/1.2221906]

I. INTRODUCTION

Tokamak[1] plasmas with vertically elongated poloidal sections have higher beta limits and better confinement than circular plasmas. The drawback is the coupled instability of the plasma vertical position.[2] Unstable plasma vertical position, especially on large tokamaks, cannot be allowed due to heavy loads on the surrounding metallic structures. A passive shell and active feedback coils for vertical stabilization (VS) associated with the use of feedback for plasma position control is therefore crucial.

Edge localized modes (ELMs) interfere with the vertical position control system and this interference must be compensated in the real-time control algorithms. In the case of large ELMs, the interference can lead to saturation of control coil voltages and currents resulting on vertical displacement events (VDEs) and disruptions.[3] ELMs are relevant to high performance plasma operation and ELM-triggered VDEs set a practical operation limit for high growth rate configurations.[4]

Two methods are widely used to reduce the effect of ELMs on the vertical position control system: (A) switching off the vertical feedback for a short time interval during each ELM; (B) use of a nonlinear controller which applies an optimized control scenario during the ELM perturbation.

The hardware of the VS digital controller, described in this work, was designed to accomplish the demands of (B). The signal processing of the VS system must be as fast as possible (ideally 0 μs) in order to decrease the control loop delay after an ELM detection. In the case of the Joint European Torus (JET) the maximum time latency allowed, for the VS digital controller to be able to counteract the effects of large ELMs, is 50 μs. However, the optimal required time latency for the VS digital controller is 10 μs and the authors aim to attain this value which also depends on algorithm complexity.

The following section describes the hardware architecture of the VS digital controller. This system is an evolution of previous control and data acquisition architectures[5–7] designed for maintainability, upgradability, scalability, and low cost per channel. Small delays on the signal acquisition/generation end points and data interconnect links associated with high data transfer rates and high processing power are key features. Synchronism for the digitizer/generator end points is also provided.

II. VS DIGITAL CONTROLLER ARCHITECTURE

The VS digital controller is based on the Advanced Telecommunications Computing Architecture™ (ATCA) specification PICMG 3.0, on the PCI Express™ fabric PICMG 3.4 and on the Aurora™ link-layer protocol.[8–10]

The VS digital controller main building blocks are an ATCA™ shelf (full mesh backplane), an ATCA™ ix86 processor module with PCI Express™ fabric (full mesh capability), and two ATCA™ control modules (scalable to 12). Each control module has the PCI Express™ fabric (one channel) and the Aurora™ fabric (full mesh capability).

Figure 1 presents the architecture of the system, as an example, for four control boards plus one processor module. PCI Express™ links, between the processor board and the control boards, are ×1 full duplex (5 Gbits/s) with a latency below 2 μs. The Aurora™ links, between control boards, are also ×1 full duplex (5 Gbits/s) and have submicrosecond latency. Figure 2 presents the transport delays, between modules, from the analog signals digitalization to the analog signals generation end points of the VS digital controller.

Real-time control algorithms are implemented on the ix86 based processor module (6 Gflops) and on the field programmable gate arrays (FPGA) [80 GMACS (giga-multiply-accumulates per second)] of the control modules. All inputs, all outputs, and processed data of one control board are available, at the same time in real time, to the other control

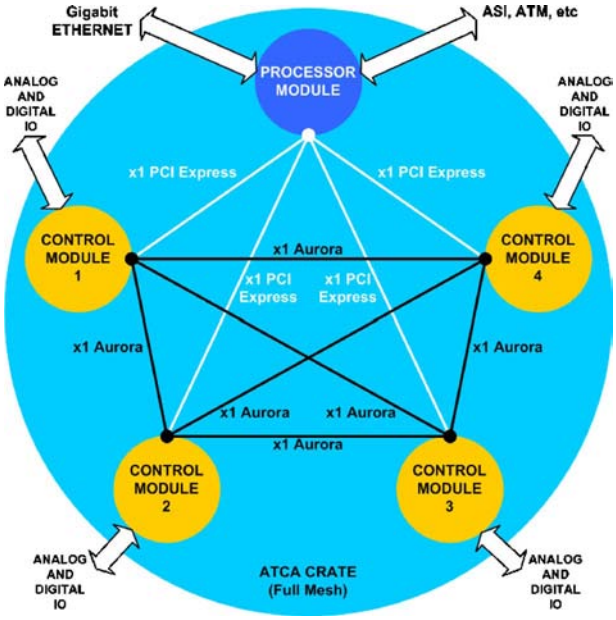

FIG. 1. System architecture.

boards through Aurora™. The processor board can access (at the same time in real time) all inputs, all outputs, and processed data of the control boards through PCI Express™.

The VS digital controller system interfaces to an external network by the Gigabit Ethernet™ (GbE) standard embedded in the processor module. Also Advanced Switching Interconnect™ (ASI) or Asynchronous Transfer Mode™ (ATM) external networks can be implemented using of the shelf personal computer (PC) add-on cards, installed on available slots of the processor module.

Transmission of control signals with better noise immunity and monitoring of power amplifiers are accomplished through fiber optic links of 5 Gbits/s (×1 full duplex), allowing connections up to distances of 300 m.

Synchronism between control modules, for multiple inputs multiple outputs (MIMO) control, is assured by dedicated clock and trigger inputs and through a rear proprietary timing fan-out bus connected to all control boards. A different synchronism approach is going to be tested, based on network time synchronization techniques, to avoid the proprietary timing fan-out bus in future system designs.

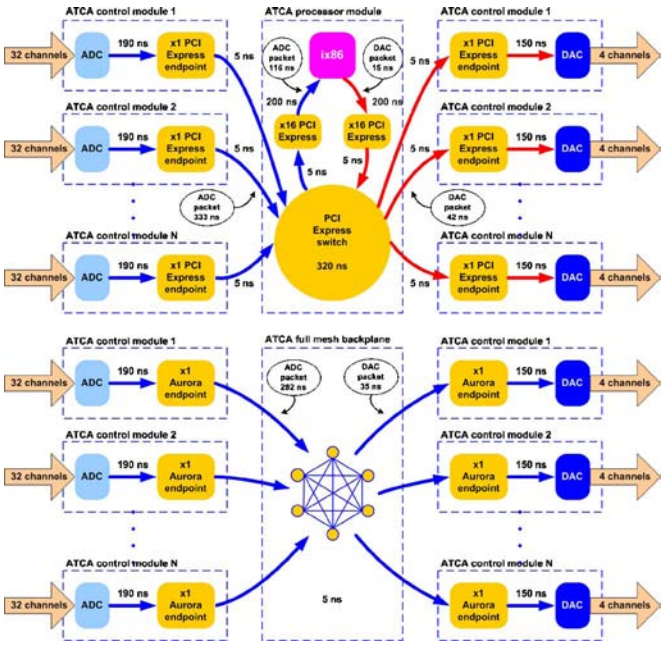

FIG. 2. Transport control loop delays of the VS digital controller.

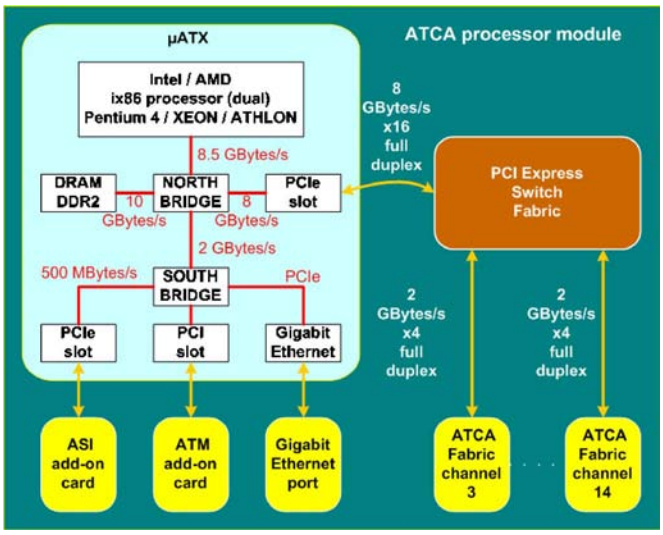

FIG. 3. ATCA™ processor module architecture.

A. ATCA™ processor module

The industry provides various ATCA™ processor modules but, currently, most of them only support the GbE™ fabric. The PCI Express™ has much better time latencies and data throughput than GbE™ and it has, at present, the best development tool support from the industry, especially on the PC platform.

Also PC ATX motherboards are readily available and provide PCI Express™ ×16 interconnections as well as processors in the ix86 family with processing power around 6 Gflops and a set of single instruction multiple data (SIMD) instructions. Highly optimized libraries are available for digital signal processing and scientific applications.

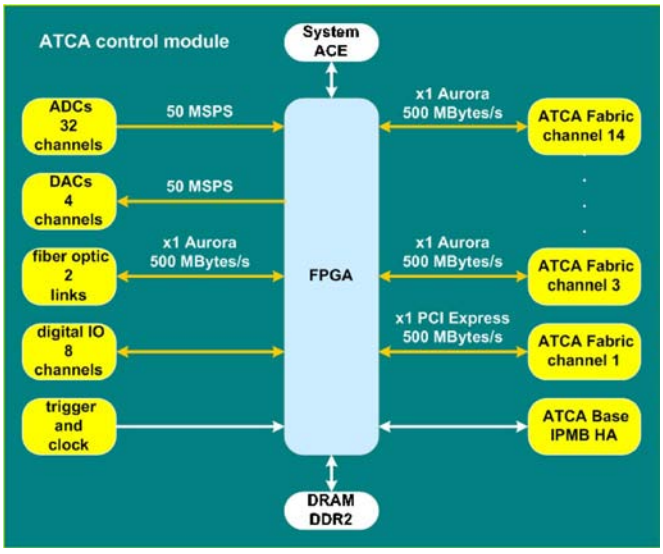

FIG. 4. ATCA™ control module architecture.

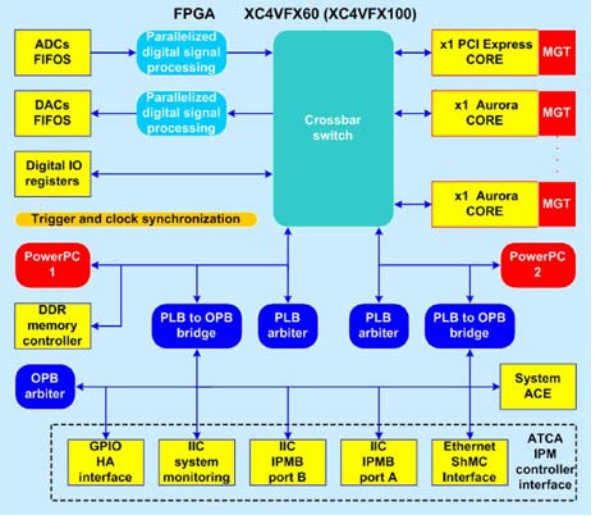

FIG. 5. Control module FPGA architecture.

The above considerations have lead to the development of a processor module implemented as a PC ATX motherboard assembled on an ATCA™ carrier module.

The motherboard is connected to the PCI Express™ switch fabric of the carrier module by a ×16 full duplex link (80 Gbits/s) directly from the NorthBridge (which is directly connected to the processor). The PCI Express™ switch fabric is also connected to 12 ATCA™ channels of ×4 full duplex (20 Gbits/s) links, allowing a scalability of up to 12 control modules in the VS system. Figure 3 shows the processor module architecture.

To comply with the low time latencies of data transfer in this setup a real-time operating system must be used. VxWorks™ and Linux™ are two options available with real-time application interface (RTAI) extensions ported to this specific hardware platform. Interrupt preemption techniques and automatic direct memory access (DMA) transfers can be used to attain better data transport time latency.

As a final remark the processor module can be easily upgraded to higher processing power replacing only the low cost ATX motherboard and/or CPU every time it is needed.

B. ATCA™ control module

The control card has 32 analog differential inputs (±10 V) with 12 bit resolution and antialiasing filters. The channels are simultaneously sampled at 50 MHz (to attain low state machine delays on the digitalization path) with programmable decimation down to 1 kHz on the module FPGA.

Four analog outputs (±10 V) with 12 bit resolution and reconstruction filters are also available as well eight programmable digital inputs/outputs (IOs) and dedicated clock and trigger inputs.

A Xilinx™ FPGA XC4VFX60 (or XC4VFX100) is the processing core of the control module. The processing power is 80 GMACS plus 1400 DHRYSTONE million instructions per second (MIPS) of the two silicon PowerPCs™ (450 MHz) inside the FPGA. A total of 13 RocketIO™ multigigabit transceivers are utilized to connect the FPGA to the ATCA™ channels. One RocketIO™ plus the respective intellectual property (IP) from Xilinx constitute the PCI Express™ end point (×1 full duplex) which connects to one ATCA™ channel. Another one plus the respective IP from Xilinx™ constitutes an Aurora™ end point (×1 full duplex) which connects to one ATCA™ channel (there are 12 Aurora end points connected to 12 ATCA channels in each control board to provide full mesh capability).

The control module block diagram is depicted in Fig. 4 and the FPGA architecture in Fig. 5. Digitized data acquired simultaneously on all analog-to-digital converters (ADCs) are processed on the FPGA and transmitted to the other control cards through Aurora ×1 full duplex links (5 Gbits/s). The FPGA can also send the processed data to the processor module through a PCI Express™ ×1 full duplex link (5 Gbits/s). The digital-to-analog converters (DACs) of each control module can be updated, by the control module itself, by other control modules or through the processor module.

The control module also provides two fiber optic ports (Aurora ×1 full duplex 5 Gbits/s) to the transmission of control signals with better noise immunity and monitoring of power amplifiers.

III. DISCUSSIONS

This scalable, low latency architecture supports MIMO fast plasma control for advanced tokamak operation.

The ATCA™ VS digital controller hardware is under development and is expected to be installed at JET by the end of 2006 in order to replace the old VS controller.

Simultaneously a traditional of the shelf VME-FPDP VS digital controller solution is also going to be installed.

A new VS control algorithm for the tokamak JET is going to run in the two new platforms to attest the performance of each one. The new VS controllers will be tested with analog stimuli generated by a test-bench system which can simulate the JET plasma behavior during critical scenarios.[11–13]

ACKNOWLEDGMENTS

This work, supported by the European Communities under the contract of Association between EURATOM/IST, was carried out within the framework of the European Fusion Development Agreement. The views and opinions expressed herein do not necessarily reflect those of the European Commission. This work has also received financial support from "Fundação para a Ciência e Tecnologia."

[1] John Wesson, *Tokamaks*, 3rd ed. (Clarendon, Oxford, 2004).
[2] K. Lackner and A. B. Macmahon, Nucl. Fusion **14**, 575 (1974).
[3] T. N. Todd, Plasma Phys. Controlled Fusion **35**, B231 (1993).
[4] F. Villone, V. Riccardo, and F. Sartori, Nucl. Fusion **45**, 1328 (2005).
[5] A. J. N. Batista, A. Combo, J. Sousa, and C. A. F. Varandas, Fusion Eng. Des. **60**, 443 (2002).
[6] A. J. N. Batista, A. Combo, J. Sousa, and C. A. F. Varandas, Rev. Sci. Instrum. **74**, 1803 (2003).
[7] J. Sousa, A. J. N. Batista, R. C. Pereira, and C. Varandas, Fusion Eng. Des. 81, (2006).
[8] www.picmg.org
[9] www.pcisig.com
[10] www.xilinx.com/aurora
[11] A. J. N. Batista, H. Fernandes, J. Sousa, C. A. F. Varandas, E. Joffrin, R. Felton, and J. Farthing, Fusion Eng. Des. **71**, 83 (2004).
[12] A. J. N. Batista, D. Alves, N. Cruz, J. Sousa, C. A. F. Varandas, E. Joffrin, R. Felton, and J. Farthing, IEEE Trans. Nucl. Sci. **53**, 756 (2006).
[13] N. Cruz, A. J. N. Batista, D. Alves, J. Sousa, C. A. F. Varandas, E. Joffrin, R. Felton, and J. Farthing, Fusion Eng. Des. **81**, 1933 (2006).