

ATCA Control System Hardware for the Plasma Vertical Stabilization in the JET Tokamak

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Abstract—A multi-input-multi-output controller for the plasma vertical stabilization was implemented and installed on the Joint European Torus tokamak. The system can attain a control-cycle time of approximately $30 \mu\text{s}$ using $\times 86$ multi-core processors but targets $10 \mu\text{s}$ via Field Programmable Gate Array (FPGA) based processing. The hardware, complying with the Advanced Telecommunications Computing Architecture (ATCA) standard, was in-house designed and implemented to achieve the required performance and consists of: A total of 6 synchronized ATCA control boards, each one with 32 analog input channels which provide up to 192 galvanically-isolated channels, used mainly for magnetic measurements. Each board contains an FPGA, which performs digital signal processing and includes a PCI Express communications interface; An ATCA rear transition module, which comprises up to 8 galvanically-isolated analog output channels to control the fast radial field amplifier ($\pm 10 \text{ kV}$, $\pm 2.5 \text{ kA}$). An optical link to digitally control the enhanced radial field amplifier ($\pm 12 \text{ kV}$, $\pm 5 \text{ kA}$). Up to 8 EIA-485 digital inputs for timing and monitoring information; An ATCA processor blade with a quad-core processor, where the control algorithm is presently running, connected to the 6 ATCA control boards through the PCI Express interface. All FPGAs are interconnected by low-latency links via the ATCA full-mesh backplane, allowing all channel data to be available on each FPGA running an upcoming distributed control algorithm.

Index Terms—ATCA, control systems, field programmable gate arrays, real time systems.

I. INTRODUCTION

THE Joint European Torus (JET) is the largest tokamak [1] operating in the world [2]. Strong magnetic fields, which confine the plasma inside the chamber, are generated with several coils. The plasma is forced to be vertically elongated to achieve better characteristics, however such kinds of plasma are

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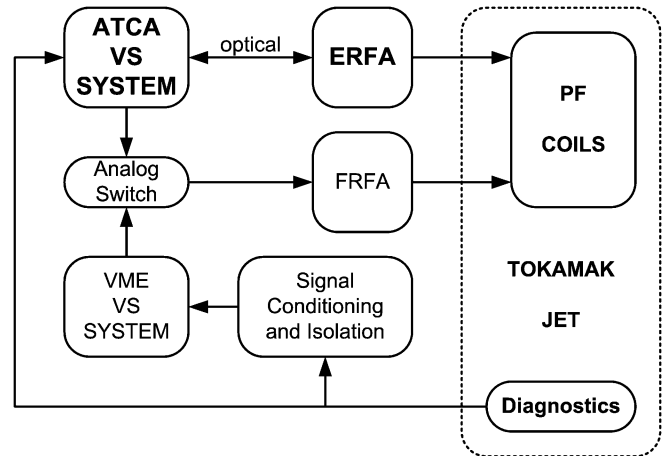


Fig. 1. ATCA VS controller coexisting with former VS system.

vertically unstable and need to be controlled in closed loop [3]. Plasma disruptions may occur due to the lack of control of the instability inducing heavy loads on the machine's vessel.

The Vertical Stabilization (VS) system purpose is to control the instability by actuating on a set of Poloidal Field (PF) coils, which generate a radial magnetic field.

The VS controller described in this paper is the evolution of a previous system architecture concept [4], complying with the specifications of the plasma control upgrade project task 2 of JET [5]. One of the most important project requirements is the execution of the control closed loop-cycle within $50 \mu\text{s}$ with a maximum jitter of $2.5 \mu\text{s}$.

The former VS controller of JET [6], based on the old C40 Digital Signal Processor (DSP) and Versa Module Eurocard (VME) bus standard, is currently working simultaneously with the new VS controller. The outputs of the two systems can be switched during JET operation, allowing the control of the PF coils by one of the VS controllers as illustrated on Fig. 1.

The new VS controller runs continuously, although JET is a pulsed machine, making the system particularly relevant for future fusion devices like ITER [7], where subsystems must run in steady-state operation.

The following sections describe the system's hardware and firmware. The software framework is described in [8].

II. SYSTEM OVERVIEW

The new VS controller hardware is based on the Advanced Telecommunications Computing Architecture (ATCA) standard [9]. Two communications fabrics are used simultaneously on the ATCA backplane, the PCI Express [10] and the Aurora [11] in star and full-mesh topologies respectively.

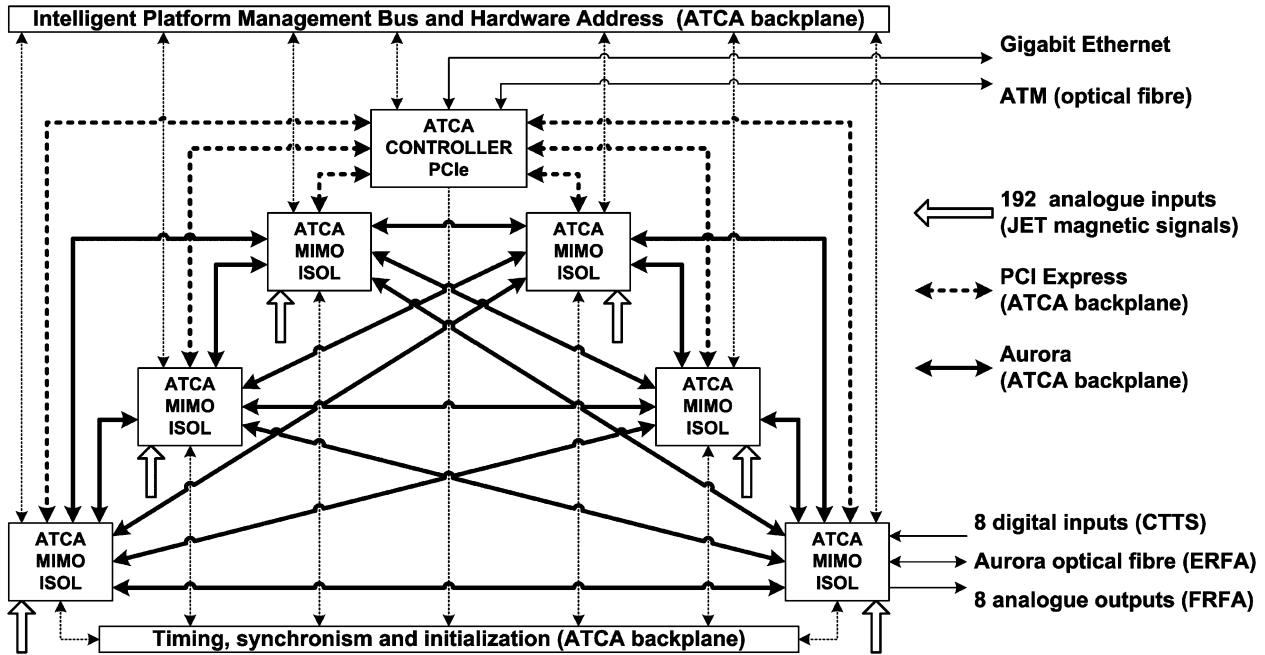


Fig. 2. ATCA VS system hardware architecture.

A. Architecture

The system's architecture is presented on Fig. 2. The analog signals from some of JET's diagnostics (mainly magnetic measurements) are connected directly to the galvanically-isolated (1 kV) inputs of the ATCA-MIMO-ISOL boards. The signals are sampled at 2 Mega Samples Per Second (MSPS) and 18-bit resolution, digitally filtered and decimated to 20 kHz (oversampling allows an increase on the dynamic range and eases the anti-aliasing filter implementation) before they are sent, in real-time, to the ATCA-CONTROLLER-PCIe board, via PCI Express full-duplex communication links, making use of the ATCA backplane.

One of the four processors of the ATCA-CONTROLLER-PCIe searches, by means of polling, a buffer memory for the decimated data arrival of the next control cycle [8]. Upon arrival the decimated data are processed by the control algorithm and the result is sent back to one of the ATCA-MIMO-ISOL boards. The resulting data from the control algorithm is used to feed the Digital to Analogue Converters (DAC) and the digital optical link of the ATCA-MIMO-ISOL.

Presently the PF coils of JET tokamak are driven by the Fast Radial-Field Amplifier (FRFA) [12] which is connected to the DACs of the VS controller. An Enhanced Radial-Field Amplifier (ERFA) [13] was installed recently to replace the FRFA and is controlled digitally through the optical link of the ATCA VS system, see Fig. 1.

To be able to decrease the control-cycle time of the centralized algorithm processing, mentioned above, an alternative or complementary distributed algorithm processing is possible using the Field Programmable Gate Arrays (FPGA), of the ATCA-MIMO-ISOL boards, and the full-mesh Aurora fabric (ATCA backplane interconnections between Aurora endpoints of the ATCA-MIMO-ISOL boards, Fig. 2). Due to the full-mesh

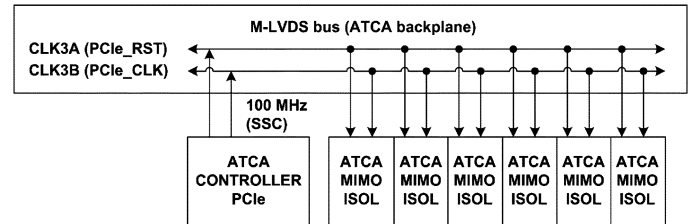


Fig. 3. PCI Express synchronization using the user defined M-LVDS lines of the ATCA backplane to propagate the sideband signals.

Aurora fabric, a Multi-Input-Multi-Output (MIMO) architecture was achieved, where the data of any input of the ATCA VS system can be present on any FPGA, in real-time.

An upcoming distributed control algorithm will be implemented on the FPGAs, allowing parallel data processing, to further reduce the control-cycle time in order to detect as soon as possible giant Edge Localized Modes (ELM) and try to counteract the associated vertical instability.

B. Synchronization

The PCI Express endpoint, implemented on the ATCA-MIMO-ISOL's FPGA, must be synchronized with the ATCA-CONTROLLER-PCIe's PCI Express switch. For that purpose, it's necessary to pass a 100 MHz Spread Spectrum Clock (SSC) and a reset signal through the ATCA backplane. The ATCA standard [10] has no specification for such sideband signals. To solve this problem, two user-defined backplane lines were used, as seen on Fig. 3.

It was also necessary to synchronize the ATCA VS system with JET's Composite Timing and Trigger System (CTTS) [14]. For that purpose, a 2 MHz clock and a trigger need to be propagated through the ATCA backplane.

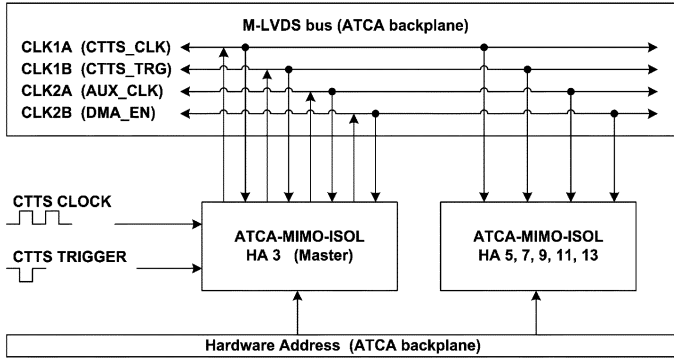


Fig. 4. Signals overriding the M-LVDS lines of the ATCA specification. The CLK1A, CLK1B, CLK2A, and CLK2B on the ATCA standard are telecomm network clocks which were replaced on the VS system by the CTTS clock, CTTS trigger, DMA enable, and an auxiliary clock.

To fully synchronize the Direct Memory Access (DMA) engines of the ATCA-MIMO-ISOL boards, two additional signals are also transmitted on the backplane.

Since the two available user-defined lines of the ATCA backplane were already taken by the PCI Express sideband signals, the only option was to violate the ATCA standard and make use of four lines specified for telecomm clocks, which are not needed on the VS control system hardware, remaining compatible with third party products that do not use these lines. Fig. 4 shows the four signals that override the ATCA specification.

The CTTS trigger signal is used to reset and synchronize the absolute-time counter of each ATCA-MIMO-ISOL board.

The DMA enable signal is used to synchronize the decimated data sent to the ATCA-CONTROLLER-PCIe memory buffer and is activated by the software.

The decimated data is time-stamped with the control-cycle absolute time, since the last trigger, and is sent simultaneously by all ATCA-MIMO-ISOL cards to the host's (ATCA-CONTROLLER-PCIe) memory buffer, with the exception of one card designated as master (defined as ATCA slot hardware address 3). The master is the last one of the six boards to send data to the host (250 ns delay).

The host, at the end of the control cycle, starts polling the memory buffer to detect an increment on the cycle time-stamp (50 μ s steps) of the master board. Upon increment detection the host gets the decimated data of all boards from the memory buffer, for algorithm processing.

The control-cycle jitter is minimized (to less than 1 μ s) with the polling scheme relying only on one ATCA-MIMO-ISOL board compared to the use of an interrupt (jitter around 3 μ s).

C. Performance

The system delays associated with the PCI Express fabric, without the digital signal processing and the control algorithm processing times, can be consulted on Fig. 5. The links between the endpoints and the switch are $\times 1$ and the packets have a constant payload of 172 bytes resulting on an effective bandwidth of $1.76 \text{ Gbit/s} = 2.5 \text{ Gbit/s}(\text{physical link}) \times 0.8(8\text{B}/10\text{B}) \times 0.88(172 \text{ bytes packet efficiency})$.

Fig. 6 shows the Aurora full-mesh fabric associated delays, also without processing times. Links between Aurora endpoints

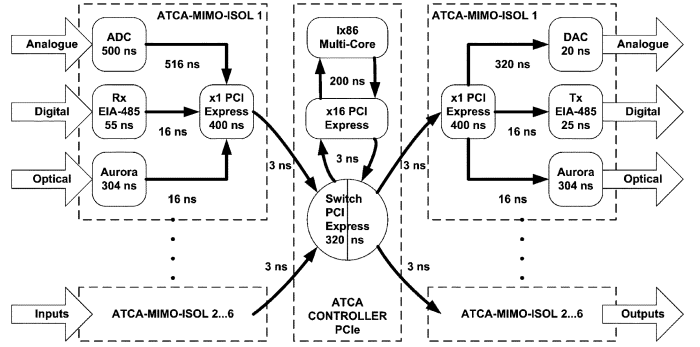


Fig. 5. Delays using the PCI Express fabric.

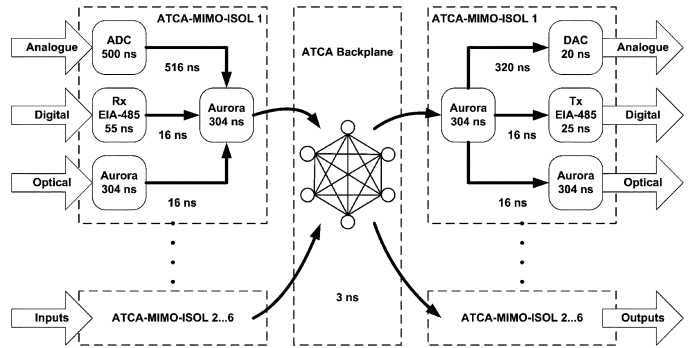


Fig. 6. Delays using the Aurora fabric.

are $\times 1$ and the effective bandwidth will depend on the upcoming distributed control algorithm.

The optical link is equally implemented using Aurora and the delays are similar to the ones of Fig. 6 with the additional propagation time through the optical fiber, which is about 500 ns.

The 100-tap Finite Impulse Response (FIR) filter of the digital signal processing on the FPGA adds a delay of 20 μ s. Actuators and sensors delays are in [13] and [5] respectively.

The control algorithm processing time, measured on host, is approximately 30 μ s and the control-cycle jitter is less than 800 ns. The upcoming control algorithm targets a control-cycle time of 10 μ s by distributing the matrixes into the six FPGAs.

III. SYSTEM BUILDING BLOCKS

An ATCA shelf, six ATCA-MIMO-ISOL boards, one ATCA-CONTROLLER-PCIe board, and an ERFA interface board, implement the VS control system hardware of JET.

The next sub-sections describe the hardware within each type of board.

A. ATCA-MIMO-ISOL Board

It is an in-house developed board complying with the ATCA specification, highly modularized, and with an optional Rear Transition Module (RTM), Fig. 7. The design is based on an FPGA connected to FLASH and Dual Data Rate (DDR) memories, Analogue to Digital Converters (ADC), DACs, EIA-485 IOs, optical Small Form-factor Pluggable (SFP) port and to the ATCA full-mesh backplane. Fig. 8 summarizes the board's architecture, including the RTM.

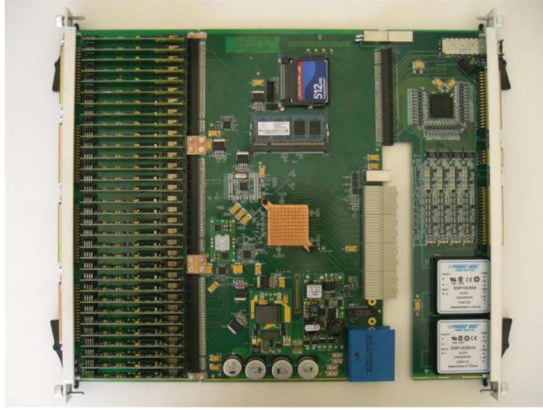


Fig. 7. ATCA-MIMO-ISOL board top view (including the RTM).

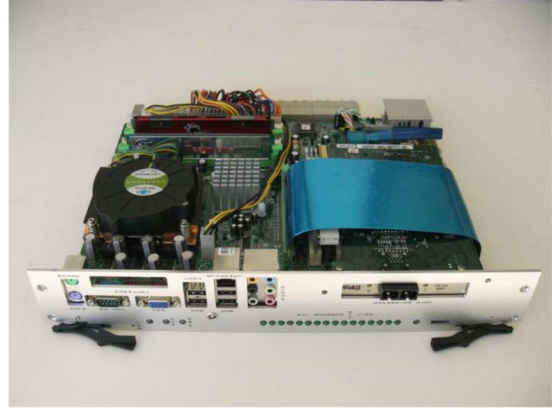


Fig. 9. ATCA-CONTROLLER-PCIe board (RTM power supply not shown).

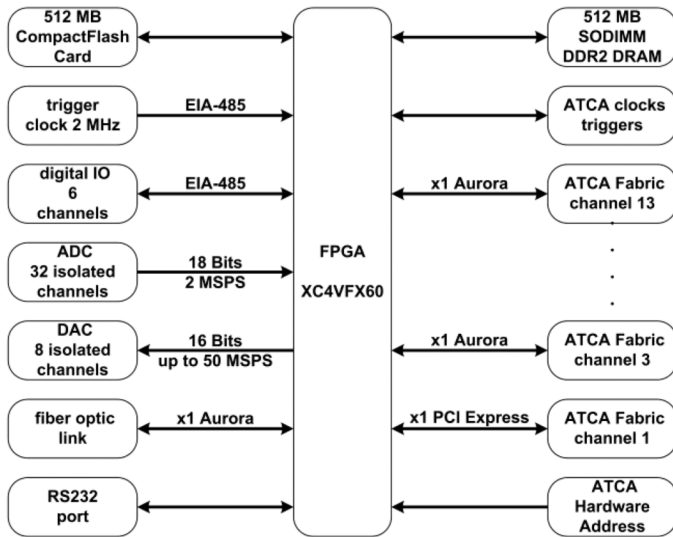


Fig. 8. ATCA-MIMO-ISOL board architecture.

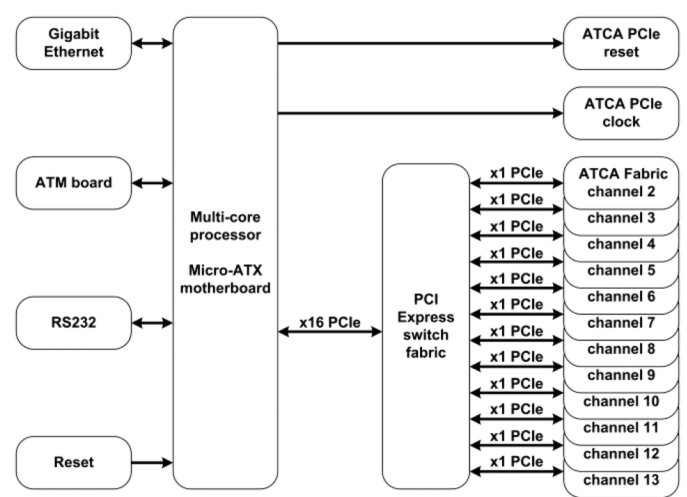


Fig. 10. ATCA-CONTROLLER-PCIe board architecture.

The board's main characteristics are:

1) Analogue inputs.

- Number of channels: 32 (differential).
- Dynamic range: -32 V to $+32\text{ V}$.
- Resolution: 18 bits.
- Sampling rate: 2 MSPS.
- Impedance: $> 100\text{ k}\Omega$.
- Voltage isolation: 1 kV.
- Anti-aliasing filter: 500 kHz passive low-pass 3rd order Butterworth.
- Connector: Male D 37-way.

2) Analogue outputs.

- Number of channels: 8 (differential).
- Dynamic range: -10 V to $+10\text{ V}$.
- Resolution: 16 bits.
- Output current: 45 mA.
- Voltage isolation: 1 kV.
- Connector: Female D 37-way.

3) Digital IO signals.

- Number of channels: 8 (EIA-485).
- Trigger (input), Clock (input), 6 user defined (inputs).
- Connector: Female D 37-way.

4) Optical interface.

- SFP full-duplex port.
- Aurora.

5) Trigger specifications.

- Master trigger: external or internal (software).
- Negative edge, minimum pulse width of 500 ns.

6) Clock specifications.

- Master clock: 2 MHz (external or internal).

7) Time stamping specifications.

- Time resolution: $1\text{ }\mu\text{s}$.
- Maximum time count: over 30 minutes.
- Time counter reset: trigger (external or internal).
- Steady state operation: triggers from central timing system with 30 minutes period.

8) Storage capabilities.

- 512 MB of SODIMM DDR2 DRAM memory.
- 512 MB of CompactFlash card memory.

9) Processing capabilities.

- FPGA: Xilinx Virtex 4 (XC4VFX60/XC4FX100).

10) ATCA specifications.

- Single front ATCA slot with RTM slot.
- ATCA Fabric channel 1 ($\times 1$ PCI Express).
- ATCA Fabric channels 3 to 13 ($\times 1$ Aurora).

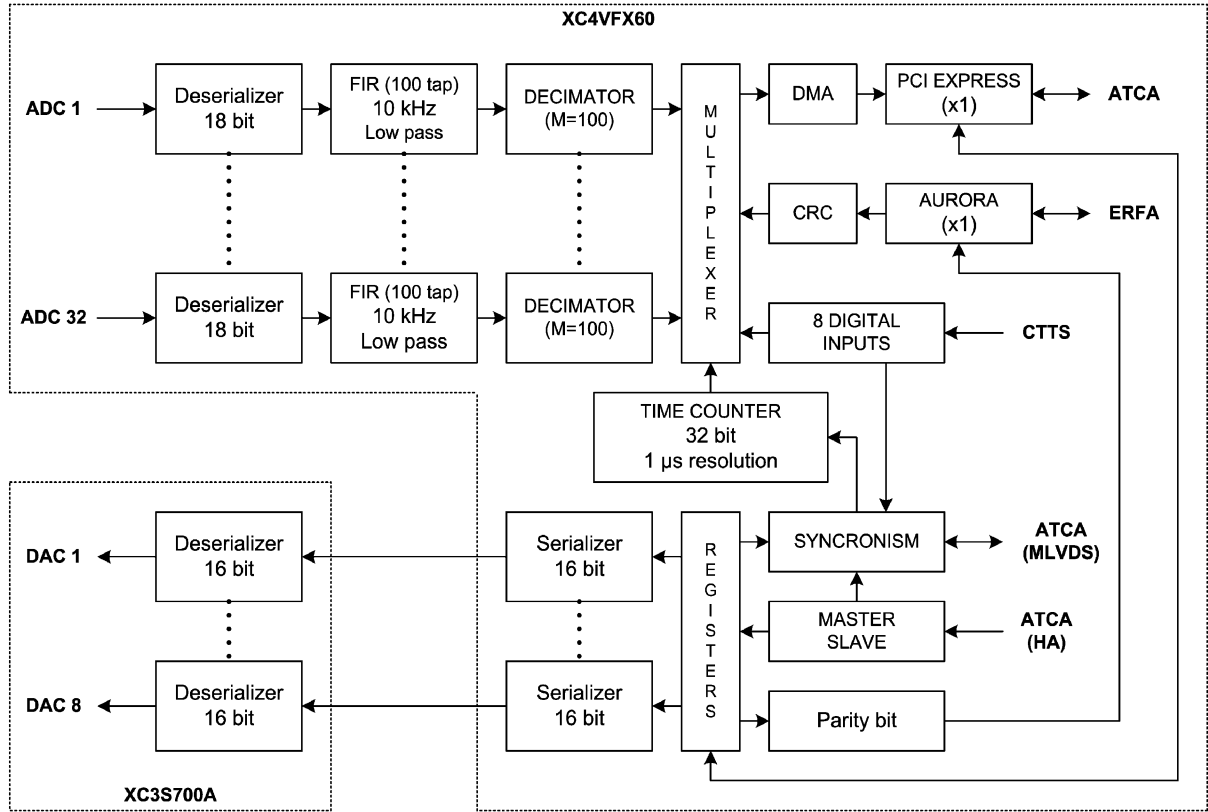


Fig. 11. Firmware architecture (simplified).

B. ATCA-CONTROLLER-PCIe Board

This in-house developed board, depicted on Fig. 9, complies with the ATCA specification and includes an auxiliary RTM power supply. The design is based on a PCI Express switch connected to the ATCA full-mesh backplane and to a micro Advanced Technology Extended (ATX) motherboard with a quad-core processor. The board architecture is shown on Fig. 10.

The board's main characteristics are:

- 1) Processing.
 - Intel quad-core.
- 2) Memory.
 - 2 GB of DIMM DDR2 DRAM.
 - Hard Disk Drive (HDD) 80 GB.
- 3) ATCA specifications.
 - Double front ATCA slot with RTM slot.
 - ATCA Fabric channels 2 to 13 ($\times 1$ PCI Express).
- 4) Interfaces.
 - Gigabit Ethernet.
 - Asynchronous Transfer Mode (ATM).
 - RS232.

C. ERFA Interface Board

This board, also in-house developed, is proprietary and complies only with the 3U Eurocard form factor. Designed exclusively to add an optical interface and an Aurora endpoint to the ERFA amplifier, allows the interconnection to the ATCA VS system for the control and monitoring of ERFA.

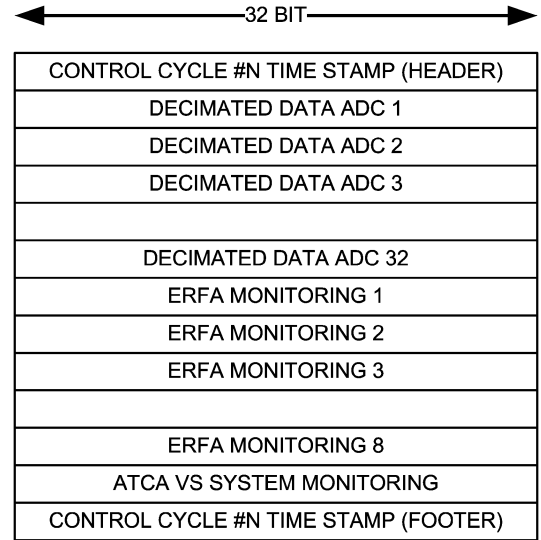


Fig. 12. PCI Express packet payload on each control cycle.

IV. SYSTEM FIRMWARE

As vital as the ATCA-MIMO-ISOL hardware is the board's FPGA firmware. The firmware was developed in Verilog language and includes serializers, deserializers, FIRs, decimators, Cyclic Redundancy Check (CRC) engines, packet engines, DMAs, PCI Express endpoint, Aurora endpoints, timing and synchronization logic, etc. Fig. 11 illustrates the firmware architecture.

Fig. 12 shows the PCI Express packet payload built by the firmware packet engine on each control cycle. The header and

footer are equal and are used by the host for packet arrival validation.

V. CONCLUSION

The new vertical stabilization architecture has been running in parallel with the previous version of the system since the summer of 2008 and it was already used several times to control the machine in closed loop. Several consecutive weeks of operation with no faults were already achieved, with the system running in real-time continuously.

The developed ATCA system can attain a control-cycle time around 30 μ s using a quad-core processor, Linux Operating System (OS) with Real-Time Application Interface (RTAI), C++ language and the PCI Express fabric. Presently the control cycle is programmed for a conservative time of 50 μ s with a measured jitter below 800 ns.

The FPGAs, currently, are only performing digital signal processing, communications, timing and synchronization tasks.

An upcoming distributed control algorithm will be implemented on the FPGAs, making use of the Aurora full-mesh fabric and the authors hope to achieve the targeted control-cycle time of 10 μ s.

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