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Citation: [Review of Scientific Instruments](#) **63**, 4799 (1992); doi: 10.1063/1.1143567

View online: <http://dx.doi.org/10.1063/1.1143567>

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Real time analysis of tokamak discharge parameters

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(Presented on 17 March 1992)

The techniques used in implementing two applications of real time digital analysis of data from the DIII-D tokamak are described. These tasks, which are demanding in both the speed of data acquisition and the speed of computation, execute on hardware capable of acquiring 40 million data samples per second and executing 80 million floating point operations per second. In the first case, a feedback control algorithm executing at a 10 kHz cycle frequency is used to specify the current in the poloidal field coils in order to control the discharge shape. In the second, fast Fourier transforms of Mirnov probe data are used to find the amplitude and frequency of each of eight toroidal mode numbers as a function of time during the discharge. Data sampled continuously at 500 kHz are used to produce results at 2 ms intervals.

I. INTRODUCTION

Real time digital analysis of tokamak data is becoming necessary for the more complex tasks in present-day facilities and will be indispensable for the the next generation of long pulse or steady state tokamaks. Here, real time analysis refers to data processing performed on the time scale of acquisition of the data while the tokamak discharge is operating. In long pulse or steady state discharges, the quantity of continuously sampled diagnostic data could easily become unmanageable. Real time analysis can be used for reduction of data to fewer values for storage, generation of trigger signals to indicate time periods for which unprocessed diagnostic data should be saved, or to generate real time data displays for experimenters. The detailed control of tokamak discharges envisioned for the next generation devices will require real time analysis in order to evaluate the complex quantities to be controlled such as the current and pressure profiles. Real time diagnostic analysis would be required to provide processed results to the discharge control systems. Real time processing of data using analog systems is common. Two examples of applications are given in Refs. 1 and 2. With digital systems, though, complex analysis algorithms that would be impractical in an analog system can be implemented relatively easily. A digital system with a general purpose design allows easy experimentation with a variety of applications for real time processing.

To make real time analysis possible both a high speed digital processor and a high rate of transfer of data between the diagnostic detector and the digital processor are necessary. A high speed data acquisition and processing system which satisfies these requirements has been developed for use in plasma control and diagnostic data analysis applications for the DIII-D tokamak.^{3,4} In this paper we describe the implementation of two applications with this system: control of the shape of the tokamak discharge and spectral analysis of fluctuations in the magnetic field detected by Mirnov probes. The type of real time calculation described here has not been practical previously but can now be implemented because of recent improvements in the processing speed of readily available microprocessors.

In the remainder of this paper, we give a brief description of the hardware in use for real time data analysis (Sec. II), followed by a description of the two real time calculations in Secs. III and IV.

II. THE DATA ACQUISITION AND PROCESSING HARDWARE

The hardware for the general purpose data acquisition and processing system used in this work has been described in detail in Ref. 4 so only a brief description is given here. The digital processor is an Intel i860 microprocessor with a clock speed of 40 MHz and peak processing speeds of 40×10^6 integer instructions per second simultaneously with 80×10^6 floating point operations per second. There are 16 Mbytes of high speed random access memory which can be used for data and software storage. Data from the tokamak diagnostic is transferred into a first in, first out (FIFO) memory where it is buffered until the i860 processor requests data. The data is then transferred directly from the FIFO memory into the random access memory without further intervention by the i860 processor. These data flow paths are illustrated in Fig. 1. Buffering of the data in a FIFO memory allows data to be delivered to multiple i860 processor systems simultaneously for parallel processing applications without requiring any synchronization between the processors. Data can be transferred from the diagnostic to the FIFO memory and from there to the random access memory at a peak speed of 40×10^6 , 14 bit samples per second. There is also an interface to the industry standard VME⁵ bus which allows access to a wide variety of input and output devices which might be necessary in a specific application and to a Sun Microsystems computer which acts as the host computer and provides the user interface.

The data acquisition hardware is designed to accommodate two primary applications: feedback control and data reduction. In feedback control a single set of diagnostic data samples is collected and the commands for the tokamak systems are calculated and output to the tokamak in each feedback cycle. The calculation cycle period and the time delay between the sampling of the diagnostic signals and the output of the command must be kept to a

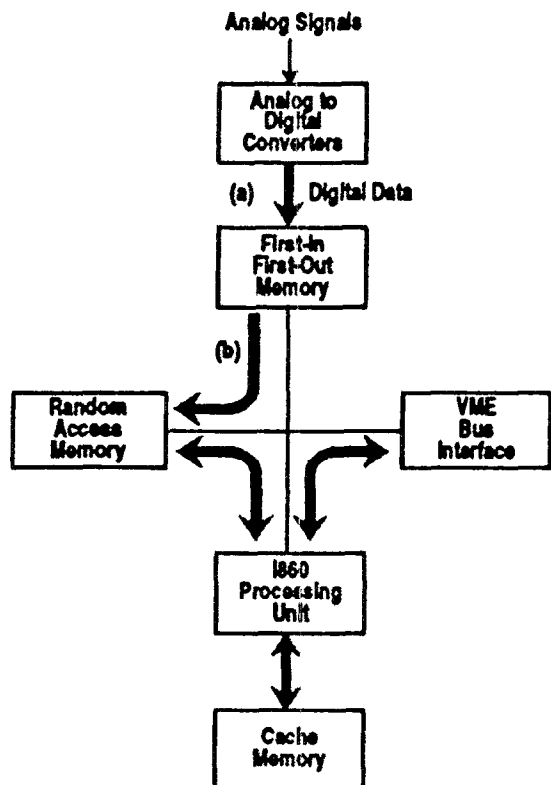


FIG. 1. A simplified diagram of the data flow paths (double width lines) in the data acquisition and processing hardware, and the common connection between the FIFO memory, the random access memory, the i860 processor, and the VME bus interface. There is a separate data path between the i860 processor and the cache memory; data transfer is possible on this path at any time. The data rate on path (a) depends on the application; data is transferred in bursts at the maximum rate of 40 Msamples/s in the control application but at a continuous, average rate of 1 Msample/s in the Mirnov probe analysis application. Data is always transferred at the maximum rate on path (b) in order to minimize the use of the common connection.

minimum. Therefore the data is transferred from the diagnostic to the FIFO memory simultaneously with the transfer from the FIFO memory to the random access memory. In data reduction applications the processor is only required to have an average processing rate which is as fast as the average rate at which data is acquired. The data is typically buffered in the FIFO memory until a sufficient number of samples has accumulated and then it is written to the random access memory in a relatively long burst. The data are accumulated in one buffer in the random access memory while the i860 processor reduces the data stored in a second memory buffer.

The i860 processor cannot access the random access memory while the data transfer from the FIFO memory is in progress because, as shown in Fig. 1, there is a common data path between the FIFO memory, the random access memory and the i860 processor. Therefore, the amount of time available for memory access during data processing depends on how close the average rate of data transfer is to the maximum transfer rate and the extent to which the i860 processor's cache memory can be used during the analysis. If there is not sufficient time available for analysis,

an alternate mode of operation allows the entire random access memory to be used to store the data acquired from the diagnostic during the tokamak discharge. The i860 processor can then provide reduced data in "near real time," that is, on a short time scale after the discharge ends.

III. A FEEDBACK CONTROL APPLICATION

In this section, we discuss the techniques used to achieve a 10 kHz feedback control cycle frequency with the computation intensive algorithm used for control of the DIII-D tokamak discharge shape. The DIII-D tokamak discharge shape is regulated by controlling the current in the 18 poloidal field coils. The current in each coil is controlled by a separate power supply so 18 power supply commands must be generated in each feedback system computation cycle. 96 tokamak magnetic diagnostic signals are digitized to provide the input data. The control algorithm uses a predetermined linear mapping, implemented with a matrix multiplication, between the input data and the discharge shape to determine the difference between the actual shape and the desired shape.³ On each cycle of the control system the 96 input values are used to compute the errors in the 18 aspects of the discharge shape that are to be controlled and the values of beta poloidal and the internal inductance which are used to choose the appropriate linear mapping. The errors are then used to compute the commands for the poloidal field power supplies.

During a discharge, the control system loops continuously through its processing cycle. First, at the appropriate time in the previous cycle, the i860 processor sends a signal to the digitizers to trigger conversion of the 96 analog input signals to digital values. The analog to digital conversion requires a total of 7 μ s and an additional 3.2 μ s are required to transfer the data from the digitizers to the random access memory. This is accomplished while the i860 processor completes a control cycle using the previous set of data. The data are then converted by the i860 processor from integer to floating point format⁴ in a total of 2.4 μ s. The digitizers are then inactive until the next conversion trigger.

Next, the linear mapping is used to compute the 18 discharge shape parameters to be controlled plus beta poloidal and internal inductance. This requires multiplication of the 96 element data vector by a 96×20 control matrix. The operation involves 3840 floating point multiplications or additions and requires only 49.7 μ s. The computed shape parameter values are subtracted from the desired values to obtain the error in the shape.

Finally, the 18 element error vector is translated to commands to increase or decrease the current in the poloidal field coils through multiplication by an 18×18 matrix that specifies which coil currents should be changed in order to adjust each of the shape parameters. This calculation requires 12.7 μ s. The coil current commands are delivered to the poloidal field power supplies by writing the command levels to digital to analog converters using the VME bus (Fig. 1).

The total cycle time is less than 100 μ s although a large amount of floating point computation is required. This is

achieved by taking advantage of several features of the hardware system.

(1) The data is collected from the digitizers in a short burst at the peak speed of 40 Msamples/s so there is a very short delay between sampling the analog signal and the beginning of the computation.

(2) The i860 processor is specifically designed for vector operations so calculation rates within a few percent of the theoretical maximum of 80 MFLOPS can actually be sustained during matrix operations. Matrix operations take most of the time in the algorithm.

(3) Access to the on-chip cache memory of the i860 processor can be sustained at 640 Mbyte/s. Therefore, the software is arranged so that most of the smaller vectors that hold intermediate results are stored in the cache memory.

(4) The data cache of 8 kbyte is too small to hold the rather large control matrix along with everything else so the i860 "pipelined floating load" instruction is used to read the matrix without disturbing the cache content.

During a matrix multiplication, the control matrix can be read from memory at the rate required to maintain the high floating point operation rate because data transfer rates within a few percent of the peak value of 160 Mbyte/s can be sustained.

(5) The entire program is composed of fewer than the 1000 machine language instructions which can be stored in the instruction cache. Because the program repeatedly executes the same instructions, access to the random access memory is not required to fetch instructions so the entire bandwidth of the processor-memory interface is available for the transfer of data for the calculations.

(6) During the matrix multiplication which produces the control command values, as the multiplication of the error vector by each matrix row is completed, the value is written immediately to the digital to analog convertor. The i860 processor can perform the required memory bus operations simultaneously with the continuation of the matrix multiplication because all components of this multiplication are located in the data cache.

IV. MODE NUMBER ANALYSIS OF MIRNOV FLUCTUATIONS

One of the more useful tokamak diagnostics is an array of Mirnov probes which measure fluctuations in the magnetic field just outside the plasma. Spectral analysis⁶ of these fluctuations is a powerful tool for the detection of plasma instabilities which may be present in the discharge. Continuous acquisition of Mirnov probe data at a sufficiently high sampling rate is typically not possible because of constraints on available digitizer memory. In this section, we describe how real time analysis of the fluctuation data from a pair of Mirnov probes has been implemented to allow observation of spectra throughout a discharge.

Frequency, amplitude, and mode number are obtained from the smoothed cross power spectrum of the Mirnov probe pair. With $X_1(\omega)$ and $X_2(\omega)$ the complex Fourier transforms of the digitized magnetic fluctuation signals from the probes, the complex cross spectrum of the probe

pair is $C_{12}(\omega) = \langle X_1(\omega)X_2^*(\omega) \rangle$, where $\langle \rangle$ denotes averaging in the frequency domain over an interval $\delta\omega$, centered about ω . From $C_{12}(\omega)$ we derive the cross power, phase, and coherence. The cross-power spectrum

$$P_{12}(\omega) = [C_{12}(\omega)C_{12}^*(\omega)]^{1/2}$$

represents the fluctuation power density as a function of frequency. The phase spectrum

$$\Theta_{12}(\omega) = \tan^{-1}\{\text{Im}[C_{12}(\omega)]/\text{Re}[C_{12}(\omega)]\}$$

gives the phase difference between the probes as a function of frequency. The toroidal mode number versus frequency can be estimated by $n(\omega) = \Theta_{12}(\omega)/\Delta\Phi$ rounded to the nearest integer, where $\Delta\Phi$ is the toroidal angle separating the probes. The coherence spectrum for the probe pair is defined as

$$\gamma_{12}(\omega) = P_{12}(\omega)/[P_{11}(\omega)P_{22}(\omega)]^{1/2},$$

where P_{11} and P_{22} are the analogous autopower spectra of the individual probes. A high value of $\gamma_{12}(\omega)$ indicates that the two probe signals are well correlated at the frequency ω , while a low value suggests that the probes are measuring uncorrelated noise. The 95% confidence level for correlation is approximately given by

$$\gamma_{95\%} = \tanh(1.96/\sqrt{2M-2}),$$

where M is the number of frequency elements included in the averaging interval $\delta\omega$. This provides a convenient criterion for deciding whether a peak in the cross-power spectrum is meaningful, and whether the associated mode number estimate is reliable.

The input data for the calculation is a set of 1024 samples from each of two probes separated by 45° toroidally from which eight toroidal mode numbers can be distinguished. The real time algorithm calculates the mode number versus frequency from each set of data and records, for each of the eight detectable mode numbers, the peak amplitude and the frequency at the peak, ignoring frequencies at which $\gamma_{12} < \gamma_{95\%}$. Typically the lower and higher frequency ranges represent different instabilities, so the amplitude peaks for the eight mode numbers are recorded in two frequency ranges. Thus the data quantity is reduced by a factor of 32 from the 1024 12 bit integer samples from each of the two probes, requiring a total of 4096 bytes of storage, to 16 floating point values (eight amplitudes, eight frequencies) in each of two frequency ranges, requiring 128 bytes of storage.

Each set of data is acquired by using the FIFO memory as a buffer. The i860 processor programs the "data transfer counter," part of the data acquisition hardware, with the number of samples required from each diagnostic channel. The sample trigger for the digitizers is generated by the tokamak timing system at 2 μ s intervals beginning at some specified time during the discharge. After each sample trigger is received, digitizer data is transferred into the FIFO memory. When the FIFO memory becomes half full, a transfer of data into the random access memory is triggered. This transfer lasts until the FIFO memory is empty. Each time the FIFO memory becomes half full

there is a new data transfer triggered until the specified total number of samples has been acquired. Because there are only two digitizer channels written into the FIFO every 2 μs , the input rate is 1 Msample/s, whereas the data is written to the random access memory at 40 Msamples/s (Fig. 1). Thus, during only 55 μs of the 2048 μs required to acquire the data, the random access memory is busy with the data transfer and during the remaining 1993 μs the i860 processor can access the memory during the data analysis.

As the first step in the analysis, the input data is converted to floating point format and $X_1(\omega)$ and $X_2(\omega)$ are computed using two 1024 point, real input to complex output, Fourier transform operations, requiring a total of approximately 1245 μs .

Second, the vectors $X_1(\omega)$ and $X_2(\omega)$ are passed through a pipelined calculation which is optimized for use with the floating point multiply and add pipeline in the i860 processor. The first part of the pipeline calculates the real and imaginary parts of $X_1(\omega)X_2^*(\omega)$, and the real values $X_1(\omega)X_1^*(\omega)$ and $X_2(\omega)X_2^*(\omega)$. In the second part of the pipeline these four values are separately averaged over three points in the frequency domain to obtain $C_{12}(\omega)$, $P_{11}(\omega)$, and $P_{22}(\omega)$. To compute one averaged vector element requires two multiplies and three additions that are performed in four processor clock cycles. The final part of the pipeline computes $P_{11}(\omega)P_{22}(\omega)\gamma_{95\%}^2$, and P_{12}^2 in five clock cycles. Thus 21 clock cycles per vector element are required for a total of 270 μs for 512 vector elements.

The complex vector C_{12} and the two real vectors P_{12}^2 and $P_{11}(\omega)P_{22}(\omega)\gamma_{95\%}^2$ contain all of the information necessary to find the frequency peaks and associated mode numbers. The actual calculation of the phase is not necessary. Instead, the mode number at each frequency is found by comparing $\text{Im}[C_{12}(\omega)]$ to each value of $\tan(\theta_i)\text{Re}[C_{12}(\omega)]$ where $\tan(\theta_i)$ is an entry from a table of values of the tangents of the angles which separate the complex plane into eight regions, one for each mode number. Each vector element is tested for sufficient coherence

by comparing P_{12}^2 to $P_{11}(\omega)P_{22}(\omega)\gamma_{95\%}^2$. Finally, the maximum amplitude and its frequency are recorded for each mode number using only frequency points with sufficient coherence. The calculation of the mode number and the peak amplitudes requires multiplications by the $\tan(\theta_i)$ values and several comparison operations, using a maximum of 31 processor clock cycles per point or 400 μs .

The complete calculation, then, requires approximately 1915 μs , less than the time required to acquire the data. This very fast spectral analysis is possible because of the vector processing features in the i860 processor, because assembly language code was written to optimize the implementation of the algorithm and because unnecessary calculation intensive operations such as divisions, inverse tangent, and square roots were eliminated from the algorithm.

V. SUMMARY

We have described how two data acquisition and computation intensive applications can be implemented in real time using digital analysis hardware which can both acquire data and perform floating point computation at high speed. These are only two examples of the type of real time data analysis application which can be useful in present tokamak facilities and which will be essential in future long pulse tokamaks.

ACKNOWLEDGMENT

This work was supported by the U.S. Department of Energy under Contract No. DE-AC03-89ER51114.

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