Evolution of Intel x86 Generations

1. **Intel 8080**
    - First general-purpose microprocessor (8-bit).
    - Used in the **Altair**, the first personal computer.
    - Featured an **8-bit data path to memory**.
2. **Intel 8086 / 8088**
    - Introduced the **x86 architecture**.
    - 16-bit processor with **wider data paths** and larger registers.
    - Added an **instruction prefetch queue** to speed up execution.The **8088 variant** powered IBM's first PC, securing Intel's dominance.
3. **Intel 80286**
    - Extended memory addressing from **1 MB to 16 MB**, enabling more powerful applications.
4. **Intel 80386**
    - First **32-bit processor** by Intel.Introduced **multitasking**, allowing multiple programs to run simultaneously.
5. **Intel 80486**
    - Added **advanced cache technology** and **instruction pipelining** for better performance.
    - Included a **built-in math coprocessor**, improving complex calculations.
6. **Pentium**
    - Introduced **superscalar architecture**, enabling **parallel execution** of multiple instructions.
7. **Pentium Pro**
    - Enhanced superscalar design with:
        - **Register renaming**
        - **Branch prediction**
        - **Data flow analysis**
        - **Speculative execution**
8. **Pentium II**
    - Introduced **Intel MMX technology** for efficient **video, audio, and graphics processing**.
9. **Pentium III**
    - Added **floating-point instructions** to support **3D graphics applications**.
10. **Pentium 4**
    - Further enhancements for **floating-point operations** and **multimedia performance**.
11. **Intel Core**
    - First Intel x86 processor with **dual-core technology**, integrating **two processors on a single chip**.
12. **Intel Core 2**
    - Extended and improved the Core architecture for **higher performance** and **energy efficiency**.

Summary of Key Trends

- **8080 → Pentium Era**: Focus on expanding data width, performance, and memory addressing.
- **Pentium → Core**: Shift towards **parallelism** and **advanced processing techniques**.
- **Core → Core 2 and beyond**: Move to **multi-core processors** and energy-efficient designs.

This evolution shows how Intel gradually enhanced performance, efficiency, and capabilities, leading to modern CPUs used today in everything from laptops to servers.

prototype of all subsequent general-purpose computers.

Figure 2.1 shows the general structure of the IAS computer (compare to middle portion of Figure 1.4). It consists of

- A main memory, which stores both data and instructions[1]
- An arithmetic and logic unit (ALU) capable of operating on binary data
- A control unit, which interprets the instructions in memory and causes them to be executed
- Input and output (I/O) equipment operated by the control unit

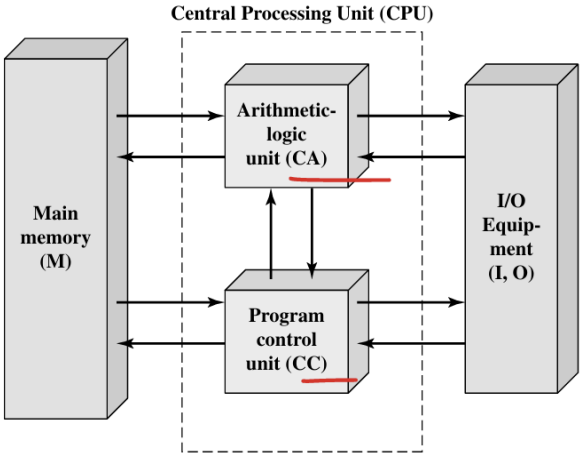

Figure 2.1 Structure of the IAS Computer

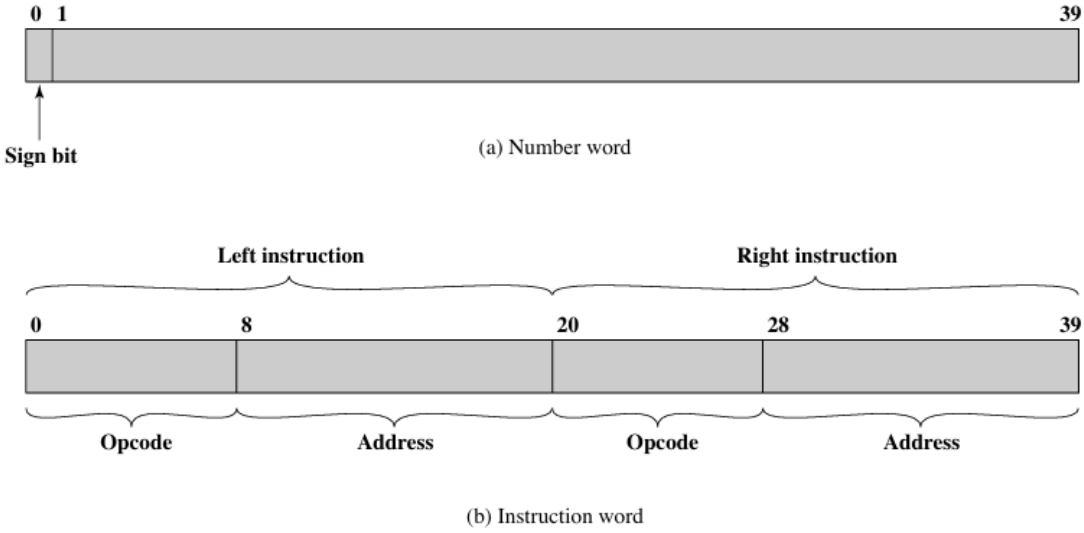

Figure 2.2 IAS Memory Formats

The memory of the IAS consists of 1000 storage locations, called *words,* of 40 binary digits (bits) each.[2] Both data and instructions are stored there. Numbers are represented in binary form, and each instruction is a binary code. Figure 2.2 illustrates these formats. Each number is represented by a sign bit and a 39-bit value. A word may also contain two 20-bit instructions, with each instruction consisting of an 8-bit operation code (opcode) specifying the operation to be performed and a 12-bit address designating one of the words in memory (numbered from 0 to 999).

The control unit operates the IAS by fetching instructions from memory and executing them one at a time. To explain this, a more detailed structure diagram is

- **Memory buffer register (MBR):** Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit.
- **Memory address register (MAR):** Specifies the address in memory of the word to be written from or read into the MBR.
- **Instruction register (IR):** Contains the 8-bit opcode instruction being executed.
- **Instruction buffer register (IBR):** Employed to hold temporarily the right-hand instruction from a word in memory.
- **Program counter (PC):** Contains the address of the next instruction-pair to be fetched from memory.
- **Accumulator (AC) and multiplier quotient (MQ):** Employed to hold temporarily operands and results of ALU operations. For example, the result of multiplying two 40-bit numbers is an 80-bit number; the most significant 40 bits are stored in the AC and the least significant in the MQ.

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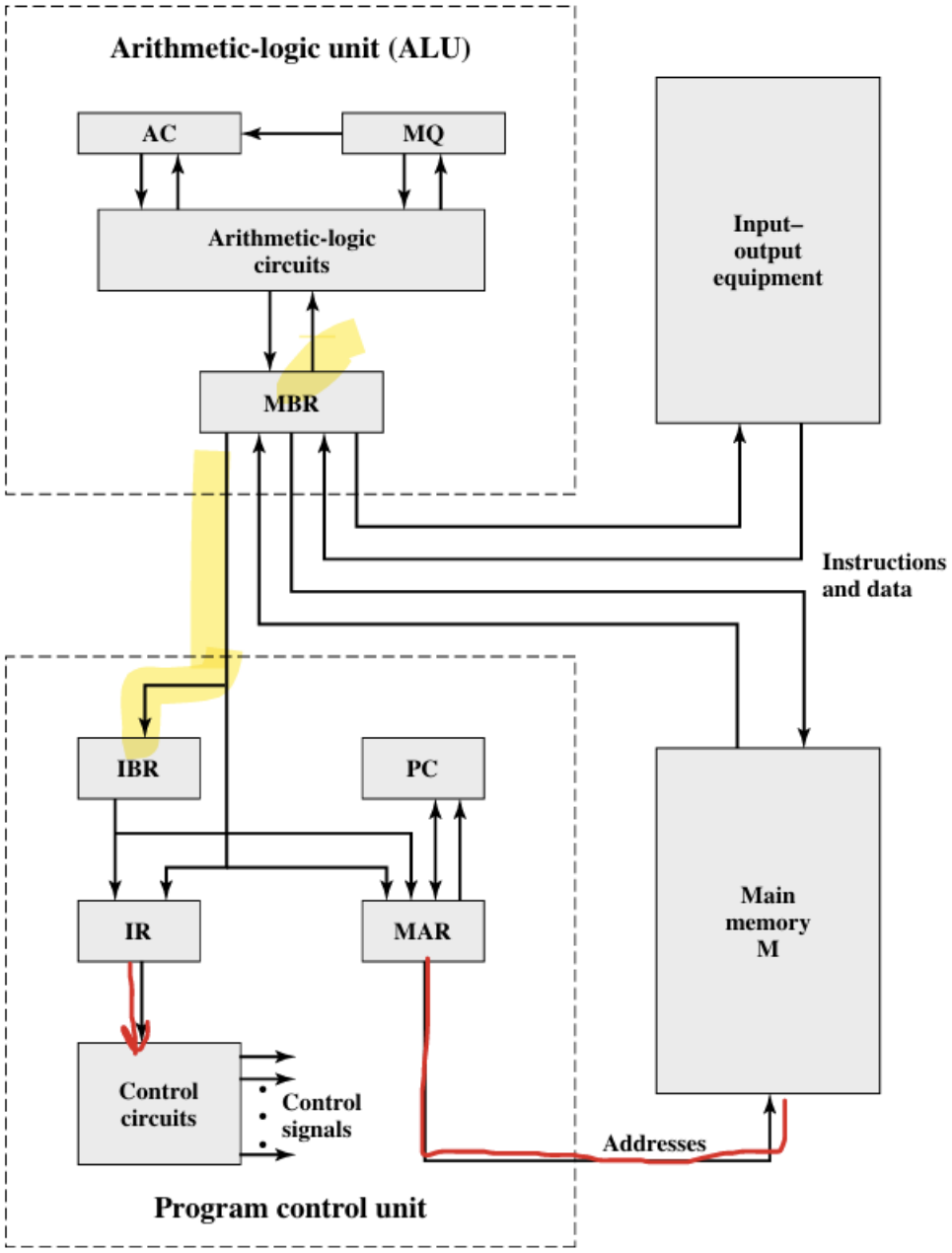

Figure 2.3 Expanded Structure of IAS Computer

1. Two

Subcycles of the Instruction Cycle

The IAS computer performs its operations in **two subcycles**:

- **Fetch Cycle**:
  - The **opcode** (operation code) of the next instruction is loaded into the **IR** (Instruction Register).
  - The **address portion** of the instruction is loaded into the **MAR** (Memory Address Register).

    - The instruction may come directly from the **IBR** (Instruction Buffer Register) or be fetched from **main memory** by first loading into the **MBR** (Memory Buffer Register) and then distributed to the IBR, IR, and MAR.
- **Execute Cycle**:
    - Once the opcode is in the IR, the **control circuitry** interprets it.
    - The control circuitry then sends appropriate **control signals** to move data or perform arithmetic/logic operations in the **ALU (Arithmetic Logic Unit)**.

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2. Purpose of Indirection

- Only **one register (MAR)** is used to specify the address for memory **read or write** operations.
- Only **one register (MBR)** is used for transferring data between the CPU and memory.
- This **simplifies the electronics** by reducing the number of data paths and circuits needed, making the design less complex and more reliable.
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sacrificing the investment in already-developed software. The characteristics of a family are as follows:

- **Similar or identical instruction set:** In many cases, the exact same set of machine instructions is supported on all members of the family. Thus, a program that executes on one machine will also execute on any other. In some cases, the lower end of the family has an instruction set that is a subset of that of the top end of the family. This means that programs can move up but not down.
- **Similar or identical operating system:** The same basic operating system is available for all family members. In some cases, additional features are added to the higher-end members.
- **Increasing speed:** The rate of instruction execution increases in going from lower to higher family members.
- **Increasing number of I/O ports:** The number of I/O ports increases in going from lower to higher family members.
- **Increasing memory size:** The size of main memory increases in going from lower to higher family members.
- **Increasing cost:** At a given point in time, the cost of a system increases in going from lower to higher family members.

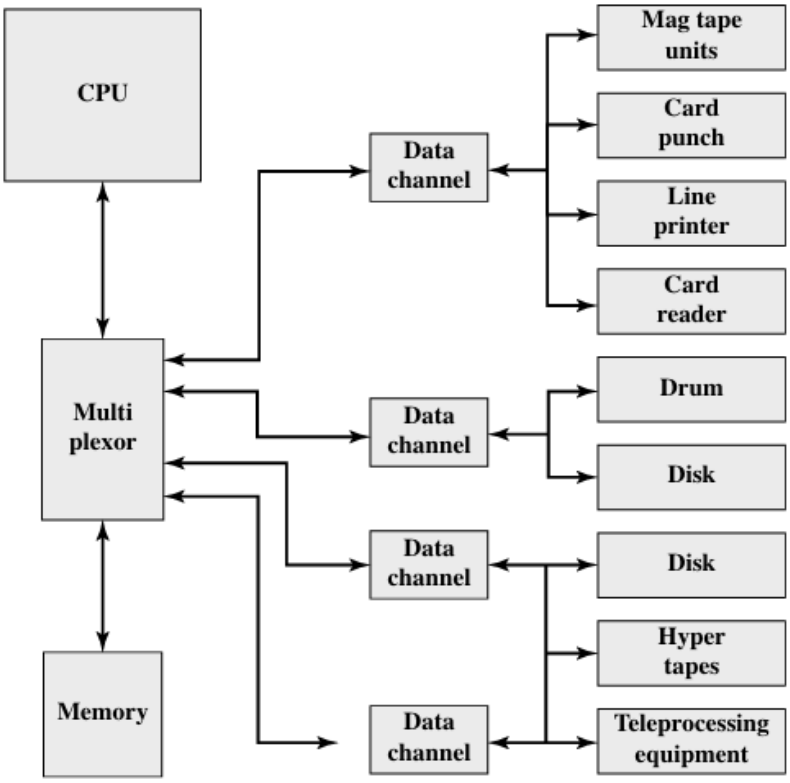

Figure 2.5 An IBM 7094 Configuration

The IAS computer had a total of 21 instructions, which are listed in Table 2.1. These can be grouped as follows:

- **Data transfer:** Move data between memory and ALU registers or between two ALU registers.
- **Unconditional branch:** Normally, the control unit executes instructions in sequence from memory. This sequence can be changed by a branch instruction, which facilitates repetitive operations.
- **Conditional branch:** The branch can be made dependent on a condition, thus allowing decision points.
- **Arithmetic:** Operations performed by the ALU.
- **Address modify:** Permits addresses to be computed in the ALU and then inserted into instructions stored in memory. This allows a program considerable addressing flexibility.

Here's a **comparison table** between **DEC PDP-8** and **IBM System/360**, with brief definitions and only the most important points:

Feature	DEC PDP-8 *(Minicomputer)*	IBM System/360 *(Mainframe)*
Definition	A **small, low-cost computer** designed for labs, small businesses, and embedded systems.	A **large, powerful computer** built for enterprises, scientific, and government use.
Size	Compact, fits on a **desk or inside equipment**.	Very large, needed **air-conditioned rooms**.
Cost	**~$16,000** – affordable for individuals and small labs.	**Hundreds of thousands of dollars** – very expensive.
Architecture	**Bus structure (Omnibus)** – shared pathways for data, control, and addresses.	**Central-switched architecture** – components connected through a central controller.
Target Market	Labs, small businesses, and **OEMs** (resellers).	Large enterprises and government organizations.
Impact	Started the **minicomputer revolution** and made computing accessible.	Set the **standard for mainframe computing** worldwide.

Explain the key techniques used in modern processors to maximize performance.

Answer: Key Techniques Used

a) Branch Prediction

- **Purpose:** Predicts which instructions will be needed next.
- **How:** Looks ahead and preloads likely instructions.
- **Benefit:** Reduces waiting time and keeps the processor busy.

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b) Data Flow Analysis

- **Purpose:** Finds dependencies between instructions.
- **How:** Reorders instructions to run as soon as data is ready.
- **Benefit:** Avoids delays and allows parallel execution.

c) Speculative Execution

- **Purpose:** Runs future instructions in advance.
- **How:** Uses branch prediction and data flow analysis.
- **Benefit:** Keeps the processor fully active and boosts performance.

Embedded system. A combination of computer hardware and software, and perhaps additional mechanical or other parts, designed to perform a dedicated function.

ARM processors are designed to meet the needs of three system categories:

• Embedded real-time systems: Systems for storage, automotive body and power-train, industrial, and networking applications

• Application platforms: Devices running open operating systems including Linux, Palm OS, Symbian OS, and Windows CE in wireless, consumer enter tainment and digital imaging applications

• Secure applications: Smart cards, SIM cards, and payment terminals

Question answer:

2.1 In a stored program computer, programs are represented in a form suitable for storing in memory alongside the data. The computer gets its instructions by reading them from memory, and a program can be set or altered by setting the values of a portion of memory.

2.2 A main memory, which stores both data and instructions; an arithmetic and logic unit (ALU) capable of operating on binary data; a control unit, which interprets the instructions in memory and causes them to be executed; and input and output (I/O) equipment operated by the control unit.

2.3 Gates, memory cells, and interconnections among gates and memory cells.

2.4 Moore observed that the number of transistors that could be put on a single chip was doubling every year and correctly predicted that this pace would continue into the near future.

2.5 Similar or identical instruction set: In many cases, the same set of machine instructions is supported on all members of the family. Thus, a program that executes on one machine will also execute on any other.

- Similar or identical operating system: The same basic operating system is available for all family members.
- Increasing speed: The rate of instruction execution increases in going from lower to higher family members.
- Increasing number of I/O ports: In going from lower to higher family members.
- Increasing memory size: In going from lower to higher family members.
- Increasing cost: In going from lower to higher family members.

2.6 In a microprocessor, all of the components of the CPU are on a single chip.