

Microprocessor (Chinmoy Sir):

1 Give the features of 8031 microcontroller. - 02

Ans:

Feature	8031	8051	8052
ROM (on-chip program space in bytes)	0K	4K	8K
RAM (bytes)	128	128	256
Timers	2	2	3
IO pins	32	32	32
Serial port	1	1	1
Interrupt sources	6	6	8

2 Enlist the brands of microcontroller. - 01

Ans:

- o Intel
- o Atmel
- o Philips
- o Infineon
- o Dallas Semi/Maxim

3 Write Short notes with key features of

i) Pentium iv - 02

Ans:

- o Pentium 4 was developed base on NetBurst micro-architecture.
- o Clock speed of Pentium 4 varies from 1.3 GHz to 3.8 GHz.
- o It operates in hyper-pipelined technology
- o Another features of Pentium 4 Processor is that it supports faster system bus at 400 MHz to 1066 MHz with 3.2 GB/s of bandwidth.
- o It has advanced dynamic execution
- o It has a rapid execution engine.
- o It has enhanced multimedia applications.

ii) Core i5 - 02

Ans:

- o Available in multiple speeds ranging from 1.90 GHz up to 3.80 GHz.
- o Typically found as quad-core processors.
- o Features 3 MB, 4 MB, or 6 MB of cache.
- o Built for modern gaming, multitasking, and content creation.
- o Supports DDR4/DDR5 RAM (DDR - Double Data Rate)
- o Provides a flexible architecture for customization.

4. Explain "how does onionskin operating system provide resource protection". - 03

Ans:

"Onion skin" security model could provide resource protection in an operating system by following way:

Layered Security: Operating like the layers of an onion, the system implements multiple security layers, each offering different levels of protection.

Access Controls: Different layers have varying levels of access permissions and restrictions for resources like data, files, and system functions.

Isolation and Segmentation: Each layer is isolated from the others, limiting the impact of breaches. This segmentation prevents unauthorized access to critical components if one layer is compromised.

Defense in Depth: Multiple layers ensure a comprehensive defense strategy. Even if one layer is breached, other layers act as additional barriers against unauthorized access.

Resource Management: Critical resources are safeguarded by tighter security controls at deeper layers, allowing only authorized access.

Reduced Attack Surface: By segmenting resources into layers, it reduces the potential areas vulnerable to attacks, making it harder for hacker to access sensitive components.

An "onion skin" security model in an operating system establishes layered protection, varying access rights, and isolation to enhance overall resource protection and system security.

5. Why is PPI used in computer system? -2

Ans:

PPI

The Programmable Peripheral Interface 8255 (PPI 8255) is an integrated circuit (IC) that serves as an essential component in digital systems, enabling the communication between a microprocessor and external devices such as input/output ports, sensors, and actuators.

The other uses are:

- o Peripheral Communication
- o Data Transfer Management
- o Handling Multiple Peripheral Device
- o Reducing CPU Load
- o Interfacing with external components

6. Explain the basic operation of TSR program. -2

Ans:

Terminate and Stay Resident

TSR (Terminate and Stay Resident) programs were special software in DOS that could stay in the computer's memory after running.

Here's how they worked:

Loading: They loaded like regular programs.

Task Execution: Did their job, like monitoring or providing utilities.

Stay in Memory: Instead of closing, they used tricks to stay active in the background.

Stay active background

Interrupts Handling: Used signals to remain in memory and respond quickly.

Background Mode: When other programs ran, TSRs stayed dormant but ready.

TSR sleeping, but ready

Sleeping

WINTAB PROGRAM
RUNNING OUR TSR
SLEEPING BUT READY

Quick Activation: Could be quickly reactivated when needed, without reloading.

TSR programs were handy for utilities and tasks that needed to run continuously or be readily available without reloading.

Need to run continuously

7. Compare among mode 0, mode 1, mode 2 of 82C55 PPI.

03

Ans:

strobed mode

PPT

10/1

Feature	Mode 0	Mode 1	Mode 2
Operating Mode	Simple Input/Output Mode	Strobed Input/Output Mode	Bidirectional Bus Mode
Ports Configuration	Three separate 8-bit ports (A, B, C)	Three 8-bit ports (A, B, C) together	Two 8-bit ports (A, B) bidirectional Group A only
Control Signals	Read (RD) and Write (WR) for each port	RD and WR for grouped ports (A, B, C)	Bidirectional control signal (Control line)
Handshake Signals	No special handshake signals	Uses a special Strobe (STB) signal	Uses a Control line for handshake
I/O Operations	Each port can work separately	Ports A, B, C work together	Ports A and B can exchange data both ways
Application	Simple tasks with individual port control	Tasks needing grouped data transfers	Tasks involving two-way data transfer

8. Define embedded processor. - 01

Ans:

An embedded system is a computer system that is designed to perform a specific task within a larger system.

It is a self-contained system that is embedded within a larger device or system and is used to control the operation of the device.

9. Mention the address lines of 80286. - 01

Ans:

80286 Microprocessor had a 24-bit address bus which could address up to 16 MB (megabytes) of physical memory.

The address lines for the 80286 processor are A0 to A23, indicating a total of 24 address lines. These address lines allowed the CPU to access different memory locations within the 16 MB addressable memory space.

10. Explain the way to achieve multitasking in DOS. - 02

Ans:

In the early versions of **DOS** (Disk Operating System), multitasking (running many programs at the same time) wasn't built-in like it is in today's system.

However, there were some methods and third-party utilities that allowed a form of multitasking in DOS environments:

✓ **TSR Programs:** These were like special programs that could stay running in the background while other programs run. They could switch between tasks, allowing a bit of multitasking. Programs like **SideKick** and **DESQview** could do this.

✓ **Multitasking Tools:** Some software like **DESQview** and **DoubleDOS** made it possible to run several DOS programs at once by creating separate little 'windows' for each program. People could switch between these windows to use different programs.

✓ **Task Switching:** There were tools that let users switch between programs manually. This meant you could pause one program and start another, pretending to do multitasking, but really, only one program worked at a time.

✓ **Memory Tricks:** People used memory management tools to better handle memory. This allowed for loading different programs into different parts of the memory. Though not real multitasking, it helped manage memory better for smoother program running.

These methods helped do a little bit of multitasking in DOS, but it wasn't as smooth or powerful as what we have now in modern operating systems.

TSR program
Multitasking tools
Task switching
Memory tricks

11. Distinguish between RAM and cache memory. - 02

Ans:

RAM	CACHE
RAM is a <u>volatile memory</u> that could store the data as long as the <u>power is supplied</u> .	Cache is a <u>smaller</u> and <u>fast memory component</u> in the computer.
The size of <u>RAM</u> is <u>greater</u> .	The size of <u>cache memory</u> is <u>less</u> .
It is <u>expensive</u> but <u>not as expensive as Cache</u> .	It is <u>expensive than RAM</u> .
It <u>holds programs</u> and <u>data</u> that are currently <u>executed by the CPU</u> .	It <u>holds frequently used data</u> by the CPU.
It is <u>not fastest</u> as compared to cache.	It is <u>faster</u> .
RAM is faster than a hard disk, floppy disk, compact disk, or just any form of secondary storage media.	Cache memory increase the <u>accessing speed</u> of CPU.
CPU reads Cache Memory data before reading RAM.	CPU reads RAM data after reading Cache Memory.
Types of RAM-	Types of Cache-
<ul style="list-style-type: none">o Static RAM (SRAM)o Dynamic RAM (DRAM)	<ul style="list-style-type: none">o L1 (Level 1) cacheo L2 (Level 2) cacheo L3 (Level 3) cache

12. Generally number of address pins of a memory device does not matched with CPU address pins. How does the mismatch problems overcome in computer system? - 03

Ans:

To overcome mismatch problem between address pin of memory and CPU address pin we use following system:

Memory Banking: Splitting memory into smaller sections called banks allows the CPU to work with parts of memory that match its address pins. It's like having multiple smaller puzzles instead of one big one.

memory को कई छोटे जाते होते हैं तो CPU को match address pin

Memory Controllers: These are connectors between the CPU and memory. They help translate the CPU's signals so the memory can understand them, even if they don't have the same number of pins.

Memory Mapping: Computer systems arrange memory in a way that aligns with the CPU's needs. They allocate specific ranges of memory to correspond with certain ranges of CPU addresses, making them match up better.

Chip Selection and Address Conversion: Using chip selection signals and address conversion techniques, the CPU can pick and talk to specific memory chips within a larger memory setup, even if they don't match perfectly in pin count.

These methods enhance the CPU and memory communication effective.

13. What do you mean by INS by OUTS? – 2

Ans:

The **INS** (input string) instruction (not available on the 8086/8088 microprocessors) transfers a byte, word, or doubleword of data from an I/O device into the extra segment memory location addressed by the DI register.

The **OUTS** (output string) instruction transfers a byte, word, or doubleword of data from the data segment memory location address by SI to an I/O device.

14. Explain basic input interface. - I

Ans:

A basic input interface is a fundamental component that allows users to input data or commands into a computer system.

It facilitates communication between users and the computer. Some basic input interfaces are:

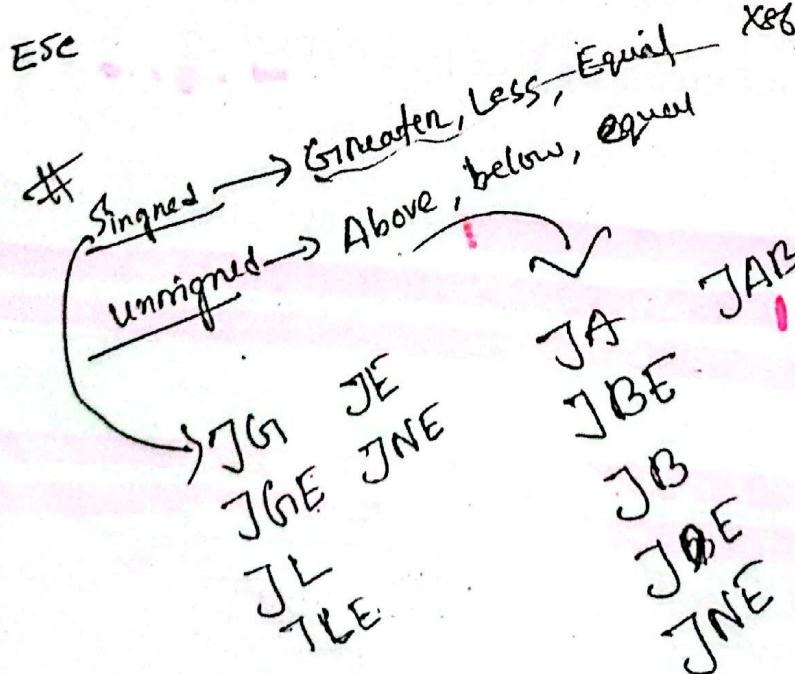
- ↪ Keyboard
- ↪ Mouse
- ↪ Touchpad etc.

15. Describe 8087 Coprocessor. - 02

Ans:

The 8087 is an early numeric coprocessor by Intel introduced in 1980. It was designed to assist the 8086 and 8088 processors in handling floating-point arithmetic operations such as addition, subtraction, multiplication, division etc.

It significantly sped up calculations involving decimal numbers with fractions or very large/small values. Featuring its own set of instructions and registers for floating-point operations, it utilized a stack-based architecture with eight 80-bit registers. The 8087 improved the computational capabilities of early x86-based computers, particularly in scientific, engineering, and mathematical applications. Later, Intel integrated similar capabilities directly into the processor chip itself.



16. Differentiate among core i3, core i5 and core i7

Ans:

Specifications	Core-i3	Core-i5	Core-i7
Application	Entry level processor	Mid level processor	High level processor
Number of cores	Dual-core or Quad-core processors	Dual-core, Quad-core, or Hexa-core	Quad-core, Hexa-core, or Octa-core processors,
Frequency range	2.93 to 3.06 GHz	3.2 to 3.46 GHz	2.8 to 4 GHz
Turbo boost	Not Supported	Supported	Supported
Cache	Smaller size	Moderately size	Larger size
Performance	Entry Level	Balanced Level	High
Graphics	Low	Mid-range	Best
Price	Low	Mid-range	Expensive

Dynamic
CPU
clock
Speed

Dual core
quad
hexa

2.9 - 3.0
3.2 - 3.4
2.8 - 3.0

17. Mention the data transfer types of a DMA controller. -01.

DMA

Ans:

Type of Transfer	Clock Cycles per Single Word Transfer ¹
Internal Memory → Internal Memory	2
External Memory ↔ Internal Memory	2 + wait states
External Memory → External Memory ²	2 + wait states
Internal Memory ↔ Internal I/O	2
External Memory ↔ Internal I/O	2 + wait states
Internal I/O → Internal I/O	2

NOTES:

1. Data transfer for one channel takes a minimum of two clock cycles per single word.
2. External memory includes external I/O.

18. How does DMA controller handle unmatched source and destination? - 02

Ans:

Ex: $(2D \rightarrow 1D)$ or $(3D \rightarrow 2D)$

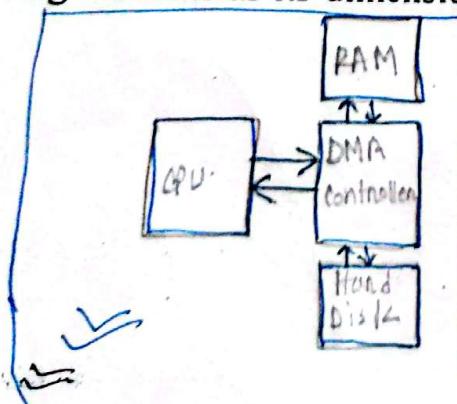
DMA

The source and destination data structures can have different dimensions.

The data structure with the largest dimension is read or written once during the block transfer; the data structure with the smaller dimension can be written or read repeatedly.

For this situation, a single counter register handles both sides of the transfer. The high-dimension (three-dimensional or two-dimensional) side of the transfer determines the counter mode. Each "tick" of the counter counts one word transfer; that is, one source read and one destination write.

The data structure on the low-dimension side of the transfer is fully described by a right-justified subset of the counter—the number of counter fields being the same as its dimension (two-dimensional or one-dimensional).



When the source and destination operate at different speeds, the DMA controller manages the mismatch using buffering and hand-shaking signals. This ensures proper synchronization and reliable data transfer without loss or corruption.

19. Give explanation of 8051 with its specification. -02

Ans:

In 1981, Intel Corporation introduced an 8-bit microcontroller called the 8051. 8-bit processor, meaning that the CPU can work on only 8 bits of data at a time. Data larger than 8 bits has to be broken into 8-bit pieces to be processed by the CPU.

Feature	8051
ROM (on-chip program space in bytes)	4K
RAM (bytes)	128
Timers	2
I/O pins	32
Serial port	1
Interrupt sources	6

20. Why is environment preservation necessary in multitasking operating system? -02

Ans:

Environment preservation in a multitasking operating system is essential to maintain:

Data Protection: Environments keep processes' data safe from unauthorized access or changes.

System Stability: It prevents problems in one process from affecting the entire system.

Smooth User Experience: Preserving environments allows multiple apps to run smoothly together.

Clean Resource Handling: It manages resources efficiently by releasing them properly when not needed.

Optimized Performance: Preserving environments helps the system use resources effectively, boosting performance.

Resource Fairness: Preserving environments ensures fair sharing of resources among processes, preventing one from dominating.

Isolation for Stability: Each process stays independent, avoiding disruptions from one to another.

✓ 24. what is a von neumann machine ? write down the major difference between intel 8085 and 8086 microprocessor . - 2

Ans :

A von Neumann machine is based on the concept of a stored-program computer, where both (instructions) and (data) are stored in the same memory space and are accessed using the same bus system.

Difference between 8085 and 8086 :

8085 microprocessor	8086 microprocessor
It is 8 bit microprocessor	It is 16 bit microprocessor
It has 16 bit address line	It has 20 bit address line
It has 8 bit data bus	It has 16 bit data bus
clock speed of 8085 microprocessor is 3 MHz	clock speed of 8086 microprocessor vary between 5.8 and 10 MHz for different versions
It has 5 flags	It has 9 flags
It does not support pipelining	It supports pipelining
It operates on clock cycle with 50% duty cycle	It operates on clock cycle with 33% duty cycle
8085 microprocessor does not support memory segmentation	8086 microprocessor supports memory segmentation
It has less number of transistors compare to 8086 microprocessor. It is about 6500 in size	It has more number of transistors compare to 8085 microprocessor. It is about 29000 in size
It is accumulator based processor	It is general purpose register based processor
It has no minimum or maximum mode	It has minimum and maximum modes
In 8085, only one processor is used	In 8086, more than one processor is used. Additional external processor can also be employed
In this microprocessor type, only 64 KB memory is used	In this microprocessor type, 1 MB memory is used

22. How can you determine the microprocessor as 8-bit or 16-bit or 32-bit or 64-bit? - 02

Ans :

The bit size of a microprocessor is determined by the width of the data bus, which is the number of bits that can be transferred at one time between the processor and memory. For example, an 8-bit microprocessor has a data bus that is 8 bits wide, while a 16-bit microprocessor has a data bus that is 16 bits wide. Similarly, a 32-bit microprocessor has a data bus that is 32 bits wide, and a 64-bit microprocessor has a data bus that is 64 bits wide. The bit size of a microprocessor determines the maximum amount of memory that can be addressed by the processor, as well as the maximum size of the data that can be processed by the processor at one time.

23. Distinguish microcontroller and microprocessor . - 02

Ans :

Micropocessor	Microcontroller
a. Microprocessors are widely used in computer systems.	a. Microcontroller is widely used in embedded systems.
b. It has only a CPU embedded into it.	b. It has a CPU, a fixed amount of RAM, ROM and other peripherals all embedded on it.
c. In case of microprocessors we have to connect all the components externally so the circuit becomes large and complex.	c. As all the components are internally connected in microcontroller so the circuit size is small.
d. It consumes more power.	d. It consumes less power than a microprocessor.
e. It has very less internal register storage so it has to rely on external storage. So all memory operations are carried out using memory based external commands which results in high processing time.	e. It has many registers so processing time is less.

24. Shortly describe 82C55 PPI with its operational modes.

2.5

PPT

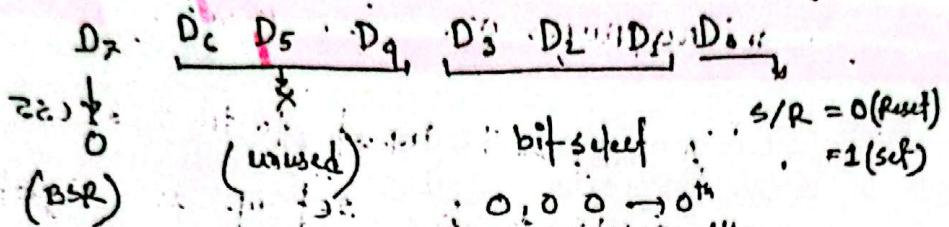
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Ans:

The 82C55 Programmable Peripheral Interface (PPI) is a classic chip from the early days of computing that provided versatile I/O capabilities for microprocessor.

MODES in 8255

→ BSR [bit select mode]



only port C is used for setting or resetting individuals bits based on control word.

→ FO

mode 0 → simple I/O for A, B, C

mode 1 → I/O port for A and B

→ port C used as handshake

mode 2 → Bidirectional data bytes for port A.

→ Port B in/out

→ Port C used as handshake

25. Why in memory decoding necessary in computer system .
----- (1.5 marks)

Ans :

Memory decoding is required in computer system to ensure that each memory location can be uniquely identified and accessed . When a computer processor needs to read from or write to a specific memory location , it sends out a memory address that corresponds to that location . Without this address decoder, only one memory device can be attached to a microprocessor that would make this virtually useless.

26. Criticize the statement " More registers integration produce faster CPU ".----- (2 marks).

NO

Ans :

The statement "More registers integration produce faster CPU" is not entirely accurate. While it is true that registers are faster to access than memory, adding more registers to a CPU does not necessarily result in a faster CPU. This is because the number of registers in a CPU is limited by the size of the CPU's instruction set and the number of bits used to represent memory addresses. Adding more registers to a CPU can also increase the complexity of the CPU's design, which can lead to longer clock cycles and slower performance. In addition, the benefits of adding more registers to a CPU are often offset by the increased complexity of the CPU's instruction set and the additional overhead required to manage the additional registers. Therefore, while registers are an important component of a CPU, adding more registers to a CPU is not a guaranteed way to improve its performance.

27. Compare PROM, EPROM, and EEPROM. ---(1.5 marks)

Ans:

Types of ROM

PROM:

- Programmable ROM
- User can store programs only once.
- User can make micro code program can be made that are needed mostly.
- The process of making program in PROM is called 'Burning'.

Example: CD-R

EPROM:

- Erasable PROM
- Information can be removed by ultra violet rays.
- Information can be re-write after removing previous information.
- It is cheaper than PROM because it is re-useable.

Example: CD(RW)

EEPROM:

- Electrically Erasable PROM
- Information can be removed by electric signals.

It is the simplest way to store info in ROM.
Now it is used to store BIOS in Memory.

Example : Pen Drive

28. Give the evolution of microprocessor from mechanical era to present (with important advancement). -(2.5 marks)

Ans :

The evolution of microprocessors can be traced back to the mechanical era, where mechanical calculators were used for arithmetic operations. The first electronic computer, the ENIAC, was introduced in 1946 and used vacuum tubes for processing data. The invention of the transistor in 1947 paved the way for the development of the first microprocessor, the Intel 4004, in 1971. The Intel 4004 was a 4-bit microprocessor that could perform up to 60,000 instructions per second. Since then, microprocessors have evolved rapidly, with the introduction of 8-bit, 16-bit, 32-bit, and 64-bit processors. Today's microprocessors are capable of executing billions of instructions per second and are used in a wide range of applications, from smartphones to supercomputers. Some of the important advancements in microprocessors include the development of cache memory, virtual memory, and parallel processing, which have all contributed to the performance and efficiency of modern microprocessors.

1946
1947

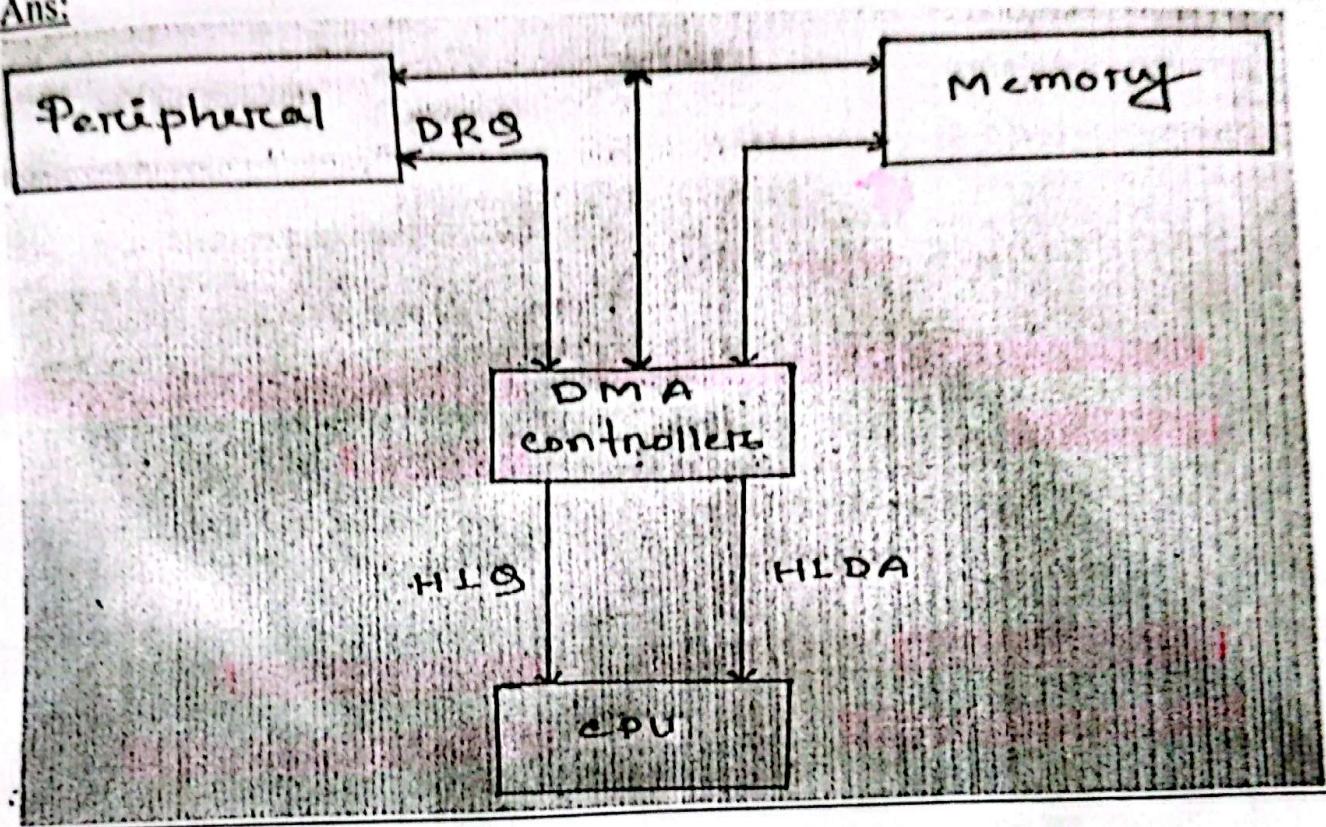
1971 → 4004 → 4 bit
1972 → 8008 → 8 bit
1978 → 8086 → 16 bit
1982 → 80286 → 16 bit

1986 → 80386 → 32 bit
1993 → Pentium → 4
2006 → Core 2 → 64 bit
2007 → Core i3 → 11
2009 → Core i5 → 4
2010 → Core i7 → 4

29. How does DMA speed up CPU performance ?----- (2 , marks)

Ques DMA

Ans:



There are many process that can be speed up CPU performance by using DMA controller , these are :----

- 1. Without CPU involvement.
- 2. Parallel processing.
- 3. Faster data transfer.
- 4. Reduce interrupt overhead.
- 5. Improve system responsiveness.

30. Distinguish between SRAM and DRAM .----(2 marks)

Ans:

Difference between SRAM and DRAM

Static RAM	Dynamic RAM
1. SRAM stores the data as long as the power supply of the computer is in the 'ON' state.	1. DRAM stores the data for a very short amount of time(few milliseconds) before losing the data even though the power supply might be in 'ON " state.
2. It has higher speed compared to DRAM	2. It has lower speed compared to SRAM
3. It is expensive	3. It is cheaper
4. It doesn't require a refreshing circuit	4. It needs to be refreshed periodically so as to retain the data, So it requires a refreshing circuit
5. It stores bit as voltage	5. It stores bit as charge
6. It has less storage capacity	6. It has more storage capacity
7. It stores data in a flip-flop circuit containing transistors in a memory cell	7. It requires less number of transistors per memory cell because capacitors and one transistor are needed to form a memory cell

31. Why is stepper motor so called ?-----(1.5 marks) PPL

Ans:

Stepper motors are so called for a very straightforward reason, that one -

- (i) This movement occurs in discrete steps, unlike regular motors that rotate continuously.
 - (ii) Each pulse of electricity sent to the motor triggers a specific, predetermined angular movement.
 - (iii) The number of steps per revolution is 200, ^{or} means step-by-step movement of the motor. Each step is precise and controlled.

Motors means the device converts electrical energy into mechanical movement.

so the Name Stepper motors effectively capture its unique characteristics of movement in distinct, controlled steps.

32. "All coprocessors are peripherals , but all peripherals are not coprocessors " -Explain this statement .-----(2.5 marks)

Ans :

Peripherals are additional devices to a computer to expand its functionality. They are external or internal and can include ----

- 1. Input devices like keyboard, mouse, camera.
- 2. Output devices like monitor, printer, speaker.
- 3. Storage devices like hard drive and USB drives.

Coprocessors are specialized processors that work alongside the main CPU to handle specific tasks more efficiently. They are typically used for ----

- 1. scientific calculations, 3D graphics rendering
- 2. Encryption and decryption operations

Peripheral has no processing power but coprocessor has little amount of processing power that can work with CPU but CPU's need no help of coprocessor for its own activity. SO it is clear that all coprocessors are peripherals but all peripherals are not coprocessors.

33. " CPU actually works on binary digits " – Explain this statement .----(2 marks)

Ans :

The statement "CPU actually works on binary digits" means that the central processing unit (CPU) of a computer processes data in the form of binary digits or bits. Binary digits are the basic building blocks of digital electronics and are represented by the numbers 0 and 1. The CPU is responsible for executing instructions stored in the computer's memory, which are represented in the form of binary code. The CPU uses transistor to perform calculations in binary. Modern computers use billions of transistors to perform calculations, but at the lowest levels, you only need a handful to form the most basic components, known as gates. Logic gates take two binary inputs, perform an operation on them, and return an output. The OR gate, for example, returns true if either of the inputs is true. The AND gate checks if both inputs are true, XOR checks if only one of the inputs are true, and the N-variants (NOR, NAND, and

XNOR) are inverted versions of their base gates. With just two gates, you can do basic binary addition.

34. Suppose you would like to transfer data from your disk drive to a flash drive by using DMA controller. Explain whole procedure in details to complete the activities.  DMA

Configure the DMA controller. This involves setting up the DMA controller registers with the appropriate values for the source and destination addresses, the number of bytes to transfer, and the transfer mode.

Prepare the disk drive. Before starting the transfer, you need to prepare the disk drive by reading the data from the disk into a buffer in memory. This can be done using standard disk I/O operations.

Start the DMA transfer. Once the DMA controller is configured and the data is loaded into memory, you can start the DMA transfer. The DMA controller will then transfer the data from memory to the flash drive without any further intervention from the CPU.

35. Describe the responsibility of memory management unit in computer system

The MMU translates virtual memory addresses used by programs into physical memory addresses in main memory. The MMU tracks memory use in fixed-size blocks known as pages, and if a program refers to a location in a page that is not in physical memory, the MMU will cause an interrupt to the microprocessor. The MMU also performs additional memory-related tasks such as memory protection, which blocks attempts by a program to access memory it has not previously requested, and managing a processor cache, which stores recently accessed data in a very fast memory and thus reduces the need to talk to the slower main memory

36. Define handshaking PPT

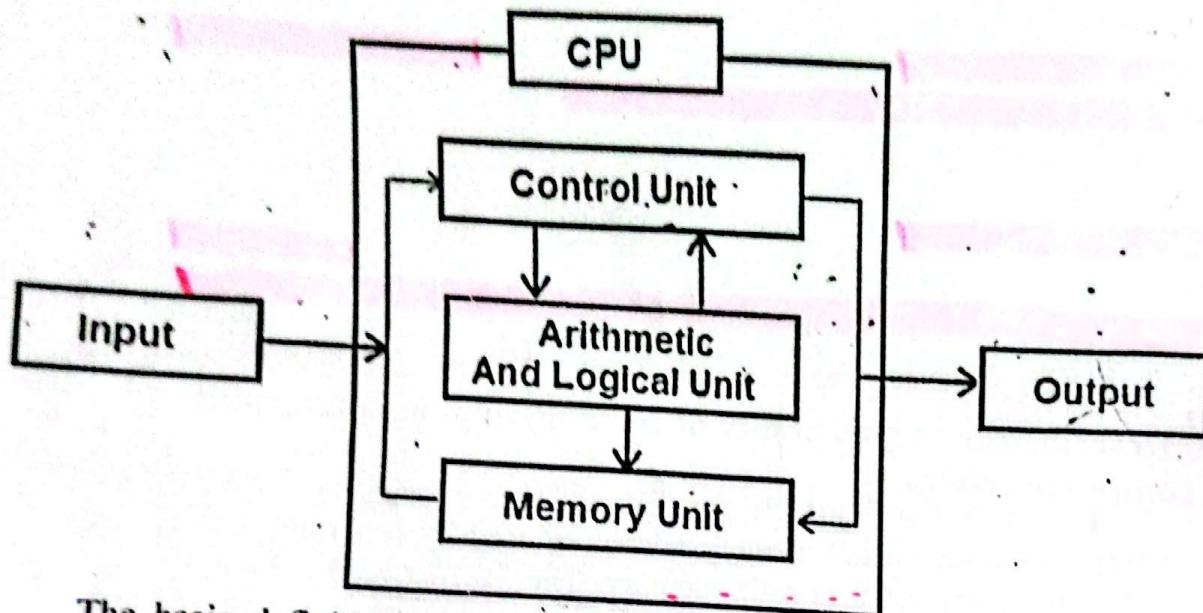
Handshaking is a technique used in microprocessors to synchronize I/O devices with the microprocessor. It is an I/O control method that allows the microprocessor to work with an I/O device at the I/O device's data transfer rate.

37. What is n-bit processor

An n-bit processor is a microprocessor that has a data bus width of n bits.

An n-bit processor is a type of computer processor that has a word length of n bits. The word length refers to the number of bits that can be processed by the processor in a single operation.

38. Block diagram of a computer system



The basic definition of the computer system is a system that receives data, processes it., and then produces the final outcome. The primary components of a computer system include the Input Unit, Central Processing Unit (CPU), Arithmetic Logical Unit (ALU), Control Unit, Storage Unit - Primary and the Secondary Unit, and the Output Unit.

39. Why is DMA used in computer system? DMA

Direct Memory Access (DMA) is used in computer systems to improve the efficiency of data transfer between devices. DMA allows I/O devices to directly access memory without the intervention of the CPU, which can significantly reduce the load on the CPU and improve system performance.

For example, when transferring large amounts of data between a hard drive and memory, using DMA can free up the CPU to perform other tasks while the data transfer is taking place.

40. Continuous motor is familiar to us, but stepper is a digital motor. Why it is digital? How it can be operated through 82C55 PPI? PPI

A stepper motor is a digital motor because it moves in discrete steps, unlike a continuous motor which rotates continuously. Stepper motors are controlled by sending digital pulses to the motor's stator, which controls the degree of rotation and position of the motor with great precision.

To operate a stepper motor through 82C55 PPI you would need to connect the stepper motor to the output ports of the 82C55 PPI and send digital pulses to the motor's stator using the PPI's control signals. The PPI can be programmed to generate the required digital pulses to control the stepper motor's rotation and position with great precision.

41. Describe channel priority of DMA DMA

DMA channel priority determines if and when a DMA channel can be interrupted during a block transfer. An interruption occurs between word transfers. The current DMA word transfer is allowed to complete before the core or another DMA channel can take control of the resource that is under contention. The DMA channel priority arbitration occurs for each DMA word transfer; only enabled and already triggered channels can take part in this arbitration.



42. Why is coprocessor used in computer systems?

A coprocessor is an additional processor used in some computer systems to perform specialized tasks such as extensive arithmetic calculations or processing of graphical displays.

A graphics processing unit (GPU) is a type of coprocessor that is specifically designed to handle the complex calculations required for rendering graphics and video.

43. What is the difference between coprocessors and peripheral devices?

Feature	Coprocessors	Peripheral Devices
Function	Supplement the functions of the primary processor (CPU)	Provide additional functionality to the computer system
Operations	Floating-point arithmetic, graphics, signal processing, string processing, cryptography or I/O interfacing with peripheral devices	Input/output tasks, data storage, and communication

44. Describe the relationship among hardware, software and firmware.

Hardware, software, and firmware are three essential components of a computer system. They work together to enable the computer to perform various tasks. Here are some key relationships between them:

Hardware provides the foundation for any software or firmware that runs on it. It includes physical components such as the motherboard, processor, memory, hard drive, etc.

Hardware	Software	Firmware
Hardware foundation (CPU, RAM, GPU, motherboard, memory, hard drive, etc.)	It is the code. It is stored in the RAM.	Type of software, stored in ROM.

Software is the code that runs on a device. It is stored in random access memory (RAM) and can be executed by the processor.

Firmware is software that is embedded in hardware. It is stored in read-only memory (ROM) and is responsible for booting the system and low-level tasks. Firmware works directly with hardware, but software doesn't. The operating system is in direct communication with the firmware, which has direct communication with the hardware.

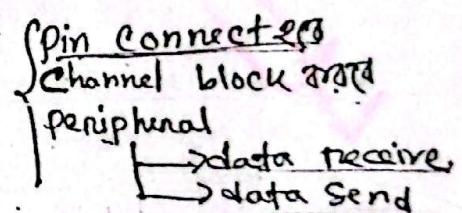
45. 8086 is a 16 bit microprocessor, but its memory mapping is 20 bits. How it is possible?

The 8086 uses a technique called memory segmentation to access memory beyond the 64 KB limit of a 16-bit address space. The 20-bit address bus is divided into two parts: the segment address and the offset address. The segment address is shifted left by 4 bits and added to the offset address to form the physical address. This allows the 8086 to address up to 1 MB of memory.

46. Explain trigger of DMA

DMA

Data movement in by a particular DMA channel is initiated by either a hardware or a software trigger. Following is an example list of some of the hardware and software DMA triggers, also known as DMA request sources. Peripheral triggers are device-dependent. A DMA channel can be configured for triggering by only one source at a time.



■ Hardware triggers:

External interrupt pins (IRQA - IRQD)

DMA channel block transfer completion (by this or a different DMA channel)

— Peripheral status bits

— Receiver has new datum to be read by DMA

— Transmitter needs new datum from DMA to send

— Timer compare event

■ Software triggers

DMA Enable bit for this DMA channel

A peripheral status bit that triggers an enabled DMA transfer also typically can trigger an enabled peripheral interrupt. The DMA transfer is triggered by the status bit change, not by the peripheral interrupt event, and the DMA transfer occurs whether or not the peripheral interrupt is enabled.

47. Mention 6 processors with its corresponding coprocessors

Processor	Coprocessor
Intel Core Processors	Intel Graphics (Integrated GPU)
AMD Ryzen Processors	AMD Radeon Graphics (Integrated GPU)
Intel Xeon Processors	Intel Xeon Phi (Many-core coprocessor)
NVIDIA Tegra Processors	NVIDIA GPU (Graphics Processing Unit)
Qualcomm Processors	Snapdragon Adreno GPU (Graphics Processing Unit)
Apple M1 Processors	Apple-designed GPU (Integrated GPU)

Processor	COPROCESSOR
1. 8086 & 8088	1. 8087
2. 80286	2. 80287, 80287 XL
3. 80286 DX	3. 80287, 80387 DX
4. 80386 SX	4. 80387 SX
5. 80486 DX	5. It is Inbuilt
6. 80486 SX	6. 80487 SX.

48. Explain the priority between a DMA channel and the core.

DMA

If the core and a DMA channel are both contending for the same partition of internal memory, but neither has begun the word transfer, the core always takes precedence. The DMA channel must wait until the core is not accessing this memory partition for at least one core clock cycle before it can begin to access the partition.

If the DMA channel and the core are each attempting to access a different internal memory partition in RAM or ROM, no contention exists. In this case, the accesses can be made simultaneously (data movement can occur in both of these data paths in a given core clock cycle).

Note: Even though DMA and the core have separate address and data buses, there is only one external address and data bus.

If the core and a DMA channel are both contending to make an external memory access, the prioritizing between that channel and the core is performed according to one of two selectable modes:

■ Static DMA — The core priority is set to be either lower, equal, or greater than that of the DMA. The individual DMA channels have equal priority when compared to the core, although they may still have unequal priorities when compared to each other. This mode is set using bits CDP[1 - 0] of the Operating Mode Register.

■ Dynamic DMA — The DMA channel priority setting used for comparison with other DMA channels is also used for comparison with the core. This mode is set using bits CP[1 - 0] of the Status Register.

If the DMA channel is already performing an access to the resource, the core must wait until the current DMA word transfer finishes accessing the resource before the core can access that resource. The core may have to wait for the entire DMA word transfer to complete, or it may have to wait only for the DMA source read to complete. This depends on the destination address of the DMA channel. If the destination of the DMA word transfer is not in the contended resource, then the core can proceed with its access to the resource while the DMA performs its destination write somewhere else.

DMA

precedence until
Allow peripheral
Allow transfer independently

core

can't
don't
don't

Static DMA

~~49. Give the application of microcontroller.~~

Here are some common applications of microcontrollers:

1. Consumer electronics
2. Medical devices
3. Automotive industry
4. Aviation
5. Marine
6. Industrial instrumentation devices
7. Process control devices
8. Metering and measurement devices
9. Toys
10. Cameras
11. Robots
12. Washing machines
13. Microwave ovens
14. Military equipment
15. RADAR
16. Missiles

Channel description

50. Describe addressing modes of DSP56300

DMA Sheet

The DSP56300 contains six DMA channels that share buses and offset registers but are otherwise independent. Each DMA channel can be triggered by interrupt pins, peripheral actions, or other DMA events, and assigned priority relative to other channels and relative to the core. Each of the six DMA channel contains its own set of four operational registers, all of which are memory-mapped in the internal I/O memory space and all of which are 24-bit registers:

- **DMA Source Address Register (DSR):** A read/write register that contains the source address for the next DMA transfer for its channel. Each DMA channel has one DSR: DSR0, DSR1, DSR2, DSR3, DSR4 and DSR5.
- **DMA Destination Address Register (DDR):** A read/write register that contains the destination address for the next DMA transfer for its channel. Each DMA channel has one DDR: DDR0, DDR1, DDR2, DDR3, DDR4 and DDR5.
- **DMA Counter (DCO):** A read/write register that contains the number of DMA data transfers to be performed by its channel. The DCO has five modes of operation determined by the DMA channel Address Generation mode defined in the DMA channel's Control Register. Each DMA channel has one DCO: DCO0, DCO1, DCO2, DCO3, DCO4 and DCO5.
- **DMA Control Register (DCR):** A read/write register that controls the operation of a DMA channel. Each DMA channel has one DCR: DCR0, DCR1, DCR2, DCR3, DCR4 and DCR5.

The DMA Controller also has supporting 24-bit registers available to all the DMA channels:

- **DMA Offset Register (DOR):** Each DOR is a read/write register that contains the offset value to be used in some of the DMA addressing modes. The DMA controller has four common offset registers (DOR0, DOR1, DOR2 and DOR3) that can be used by all the channels according to their Address Generation mode.

- **DMA Status Register (DSTR):** This read-only register reflects the overall operating status of all channels in the DMA Controller.

5). Describe overlapping data movement mechanism of DMA.

DMA

The overlapping data movement mechanism involves the simultaneous operation of the DMA controller and the CPU during data transfers. While the DMA controller is transferring data between the source and destination, the CPU is free to perform other computations or execute instructions. This simultaneous operation of the DMA controller and the CPU is the essence of overlapping data movement. It maximizes the system's overall throughput and efficiency by allowing parallel processing.