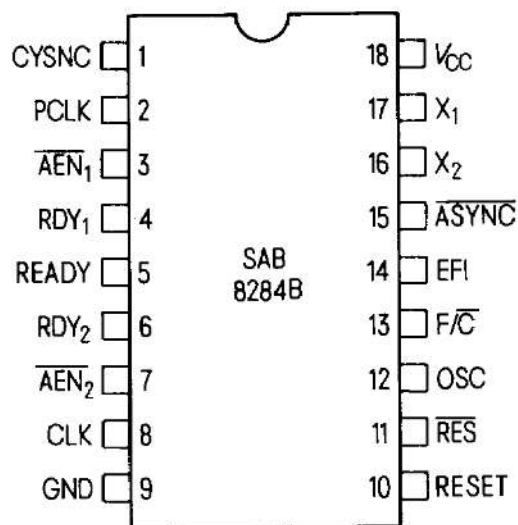


SAB 8284B, SAB 8284B-1 Clock Generator and Driver for SAB 8086 Family Processors

- Fully compatible with SAB 8284A, SAB 8284A-1
- 30% Less Power Supply Current than Standard SAB 8284A, SAB 8284A-1
- Generates the System clock for SAB 8086 and SAB 8088 Processors:
upto 8 MHz with SAB 8284B
upto 10 MHz with SAB 8284B-1
- Uses a Crystal or a TTL Signal for Frequency Source upto 30 MHz
- Provides Synchronization for Synchronous and Asynchronous READY Signals
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other SAB 8284Bs

Figure 1
Pin Configuration



Pin Names

| | |
|--------------------------------------|---|
| X ₁ X ₂ | Connections for crystal |
| F/C | Clock source select |
| EFI | External clock input |
| CSYNC | Clock synchronization input |
| ASYNC | Ready synchronization select |
| RDY ₁ RDY ₂ | Ready signal |
| AEN ₁ AEN ₂ | Address enabled qualifiers for RDY _{1,2} |
| RES | Reset input |
| RESET | Synchronized reset output |
| OSC | Oscillator output |
| CLK | MOS Clock for the processor |
| PCLK | TTL Clock for peripherals |
| READY | Synchronized ready output |
| V _{CC} | Power Supply (+5V) |
| GND | Ground (0V) |

SAB 8284B is a bipolar clock generator/driver designed to provide clock signals for SAB 8086 and SAB 8088 processors and peripherals. It also contains READY logic for operation with two bus systems and provides the processors required

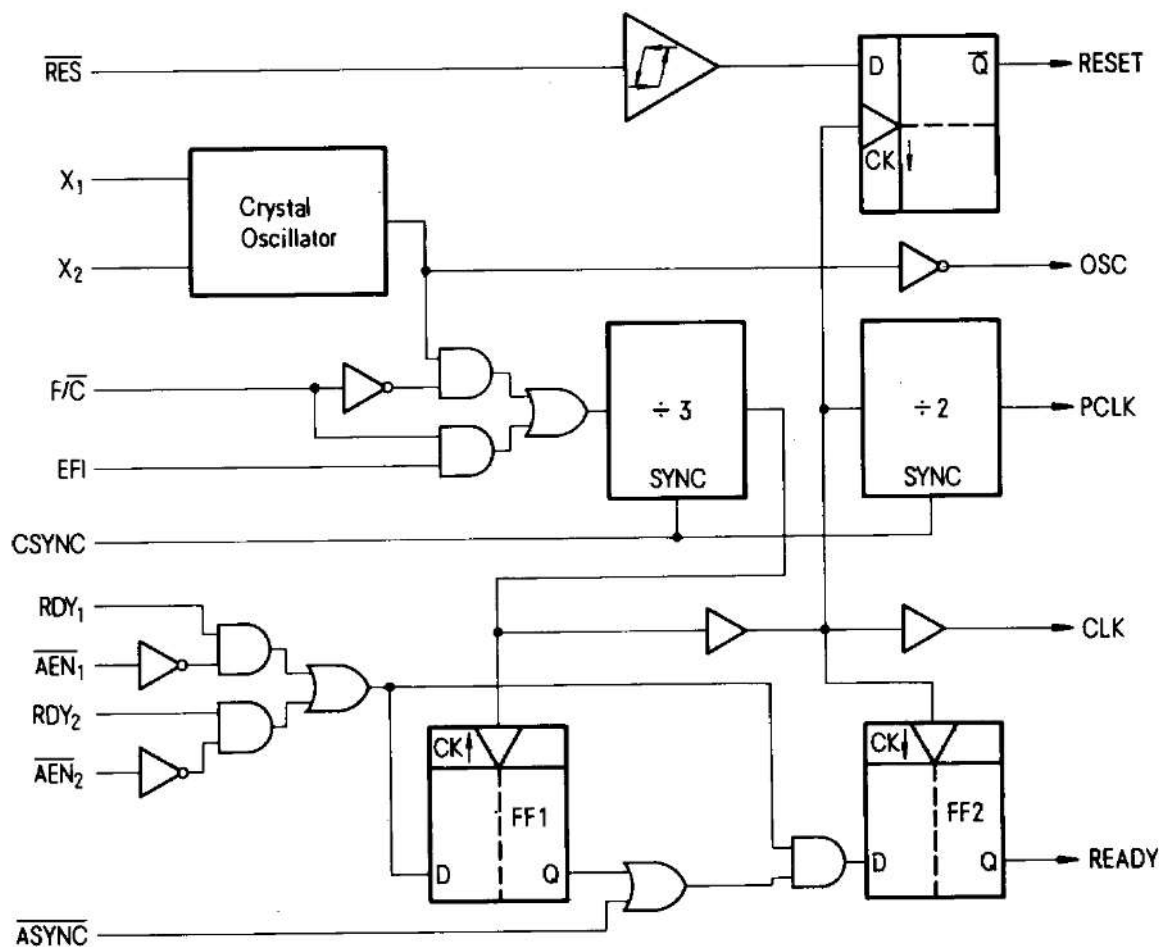
READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Pin Definitions and Functions

| Symbol | Number | Input (I) Output (O) | Function |
|--|--------|-------------------------|---|
| $\overline{\text{AEN}}_1$ $\overline{\text{AEN}}_2$ | 3, 7 | I | ADDRESS ENABLE. $\overline{\text{AEN}}$ is an active LOW signal. $\overline{\text{AEN}}$ serves to qualify its respective Bus Ready Signal (RDY_1 or RDY_2). $\overline{\text{AEN}}_1$ validates RDY_1 while $\overline{\text{AEN}}_2$ validates RDY_2 . Two $\overline{\text{AEN}}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{\text{AEN}}$ signal inputs are tied true (LOW). |
| RDY_1 , RDY_2 | 4, 6 | I | BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY_1 is qualified by $\overline{\text{AEN}}_1$ while RDY_2 is qualified by $\overline{\text{AEN}}_2$. |
| $\overline{\text{ASYNC}}$ | 15 | I | READY SYNCHRONIZATION SELECT. $\overline{\text{ASYNC}}$ is an input which defines the synchronization mode of the READY logic. When $\overline{\text{ASYNC}}$ is low, two stages of READY synchronization are provided. When $\overline{\text{ASYNC}}$ is left open or HIGH a single stage of READY synchronization is provided. |
| READY | 5 | O | READY. READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met. |
| X_1 , X_2 | 16, 17 | I | CRYSTAL IN. X_1 and X_2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency. |
| $\text{F}/\overline{\text{C}}$ | 13 | I | FREQUENCY/CRYSTAL SELECT. $\text{F}/\overline{\text{C}}$ is a strapping option. When strapped LOW, $\text{F}/\overline{\text{C}}$ permits the processors clock to be generated by the crystal. When $\text{F}/\overline{\text{C}}$ is strapped HIGH, CLK is generated from the EFI input. |
| EFI | 14 | I | EXTERNAL FREQUENCY IN. When $\text{F}/\overline{\text{C}}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output. |
| CLK | 8 | O | PROCESSOR CLOCK. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts ($V_{\text{CC}} = 5\text{V}$) is provided on this pin to drive MOS devices. |
| PCLK | 2 | O | PERIPHERAL CLOCK. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has 50% duty cycle. |
| OSC | 12 | O | OSCILLATOR OUTPUT. OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal. |
| $\overline{\text{RES}}$ | 11 | I | RESET IN. $\overline{\text{RES}}$ is an active LOW signal which is used to generate RESET. The SAB 8284B provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. |

| Symbol | Number | Input (I) Output (O) | Function |
|-----------------|--------|-------------------------|--|
| RESET | 10 | O | RESET. RESET is an active HIGH signal which is used to reset the SAB 8086 family processors. Its timing characteristics are determined by RES. |
| CSYNC | 1 | I | CLOCK SYNCHRONIZATION. CSYNC is an active HIGH signal which allows multiple SAB 8284B to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hard-wired to ground. |
| V _{CC} | 18 | — | Power Supply (+5V) |
| GND | 9 | — | Ground (0V) |

Figure 2
Block Diagram



Functional Description

General

The SAB 8284B is a single chip clock generator/driver for SAB 8086 and SAB 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, "Ready" synchronization and reset logic. Refer to Figure 2 for "Block Diagram" and Figure 1 for "Pin Configuration".

Oscillator

The oscillator circuit of the SAB 8284B is designed primarily for use with an external series resonant fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors ($R_1 = R_2 = 510 \Omega$) as shown in figure 7 are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

It is advisable to limit stray capacitances to less than 10pF on X1 and X2 to minimize deviation from operating at the fundamental frequency.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another SAB 8284B clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the SAB 8284B. This is accomplished with two Schottky flip-flops (see figure 3). The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/\overline{C} input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the $\div 3$ counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle MOS clock driver designed to drive the SAB 8086 and SAB 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input (\overline{RES}) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the SAB 8284B. Waveforms for clocks and reset signals are illustrated in Figure 4.

READY Synchronization

Two READY inputs (RDY_1 , RDY_2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier (\overline{AEN}_1 and \overline{AEN}_2 , respectively).

The $\overline{\text{AEN}}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{\text{AEN}}$ pin should be tied LOW.

Synchronization is required for all asynchronous active going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{\text{ASYNC}}$ input defines two modes of READY synchronization operation.

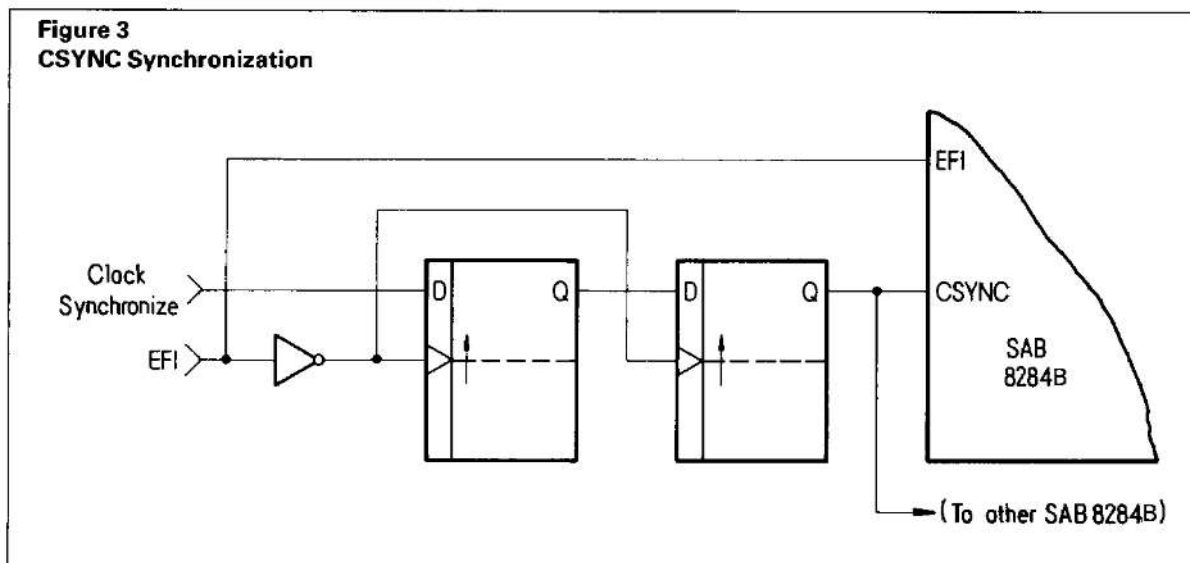
When $\overline{\text{ASYNC}}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time t_{R1VCH}) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY

output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL} , on each bus cycle (Refer to Figure 5).

When $\overline{\text{ASYNC}}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices **that can be guaranteed to meet the required RDY time** (Refer to Figure 6).

$\overline{\text{ASYNC}}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Figure 3
CSYNC Synchronization



Absolute maximum ratings ¹⁾

| | |
|--------------------------------|---------------|
| Temperature Under Bias | 0 to 70°C |
| Storage Temperature | – 65 to 150°C |
| All Output and Supply Voltages | –0.5 to 7 V |
| All Input Voltages | –1.0 to 5.5 V |
| Power Dissipation | 1W |

D.C. Characteristics
 $T_A = 0 \text{ to } 70^\circ\text{C}; V_{CC} = +5 \text{ V} \pm 10\%$

| Symbol | Parameter | Limit Values | | Unit | Test Condition |
|---------------------|---|--------------|--------------|---------------|--|
| | | Min. | Max. | | |
| I_F | Forward Input Current (ASYNC) Other Inputs | – | –1.3 –0.5 | mA | $V_F = 0.45 \text{ V}$ $V_F = 0.45 \text{ V}$ |
| I_R | Reverse Input Current (ASYNC) Other Inputs | | 50 50 | μA | $V_R = V_{CC}$ $V_R = 5.25 \text{ V}$ |
| V_C | Input Forward Clamp Voltage | | –1.0 | V | $I_C = -5 \text{ mA}$ |
| I_{CC} | Power Supply Current | | 110 | mA | All outputs open |
| V_{IL} | Input LOW Voltage | | 0.8 | V | – 5 mA –1 mA –1 mA – |
| V_{IH} | Input HIGH Voltage | 2.0 | – | | |
| V_{IHR} | Reset Input HIGH Voltage | 2.6 | – | | |
| V_{OL} | Output LOW Voltage | – | 0.45 | | |
| V_{OH} | Output HIGH Voltage CLK Other Outputs | 4 2.4 | – | | |
| $V_{IHR} - V_{ILR}$ | $\overline{\text{RES}}$ Input Hysteresis | 0.25 | – | | |

¹⁾ Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5\text{V} \pm 10\%$

Timing Requirements

| Symbol | Parameter | Limit Values | | Unit | Test Condition |
|---------------------|--|--|------------------|------|---------------------------|
| | | Min. | Max. | | |
| t_{EHEL} | External Frequency HIGH Time | 13 | — | ns | 90% – 90% V_{IN} |
| t_{ELEH} | External Frequency LOW Time | | | | 10% – 10% V_{IN} |
| t_{EEL} | EFI Period | $t_{\text{EHEL}} + t_{\text{ELEH}} + \delta$ | | | ³⁾ |
| | XTAL Frequency | 12 | 25 ⁷⁾ | MHz | — |
| t_{R1VCL} | RDY ₁ , RDY ₂ Active Setup to CLK | 35 | — | ns | ASYNC = HIGH |
| t_{R1VCH} | RDY ₁ , RDY ₂ Active Setup to CLK | | | | ASYNC = LOW |
| t_{R1VCL} | RDY ₁ , RDY ₂ Inactive Setup to CLK | | | | |
| t_{CLR1X} | RDY ₁ , RDY ₂ Hold to CLK | 0 | | | |
| t_{AYVCL} | ASYNC Setup to CLK | 50 | | | |
| t_{CLAYX} | ASYNC Hold to CLK | 0 | | | |
| t_{A1VR1V} | $\overline{\text{AEN}}_1$, $\overline{\text{AEN}}_2$ Setup to RDY ₁ , RDY ₂ | 15 | | | — |
| t_{CLA1X} | $\overline{\text{AEN}}_1$, $\overline{\text{AEN}}_2$ Hold to CLK | 0 | | | |
| t_{YHEH} | CSYNC Setup to EFI | 20 | | | |
| t_{EHYL} | CSYNC Hold to EFI | 10 | | | |
| t_{YHYL} | CSYNC Width | $2 \cdot t_{\text{EEL}}$ | | | |
| t_{1HCL} | $\overline{\text{RES}}$ Setup to CLK | 65 | | | ⁴⁾ |
| t_{CL1H} | $\overline{\text{RES}}$ Hold to CLK | 20 | | | |
| t_{LIH} | Input Rise Time | — | 20 | | From 0.8V to 2.0V |
| t_{IHL} | Input Fall Time | — | 12 | | From 2.0V to 0.8V |

Notes see next page.

Timing Responses

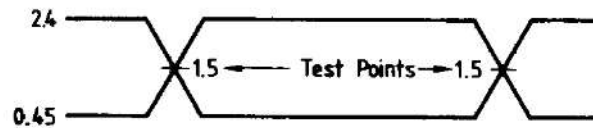
| Symbol | Parameter | Limit Values | | Unit | Test Condition |
|------------------------------|-------------------------------------|---------------|------|------|---------------------|
| | | Min. | Max. | | |
| t_{CLCL} | CLK Cycle Period | 100 | | ns | — |
| t_{CHCL} | CLK HIGH Time | ¹⁾ | — | | Fig. 7 & Fig. 8 |
| t_{CLCH} | CLK LOW Time | ²⁾ | | | Fig. 7 & Fig. 8 |
| t_{CH1CH2} t_{CL2CL1} | CLK Rise or Fall Time | — | 10 | | 1.0 V to 3.5 V |
| t_{PHPL} | PCLK HIGH Time | $t_{CLCL}-20$ | | | — |
| t_{PLPH} | PCLK LOW Time | $t_{CLCL}-20$ | | | |
| t_{RYLCL} | Ready Inactive to CLK ⁶⁾ | —8 | | | Fig. 9 & Fig. 10 |
| t_{RYHCH} | Ready Active to CLK ⁵⁾ | ²⁾ | | | Fig. 9 & Fig. 10 |
| t_{CLIL} | CLK to Reset Delay | | 40 | | |
| t_{CLPH} | CLK to PCLK HIGH Delay | — | | | |
| t_{CLPL} | CLK to PCLK LOW Delay | | 22 | | — |
| t_{OLCH} | OSC to CLK HIGH Delay | —5 | | | |
| t_{OLCL} | OSC to CLK LOW Delay | 2 | 35 | | |
| t_{OLOH} | Output Rise Time (except CLK) | — | 20 | | From 0.8 V to 2.0 V |
| t_{OHOL} | Output Fall Time (except CLK) | | 12 | | From 2.0 V to 0.8 V |

- ¹⁾ $(\frac{1}{3} t_{CLCL}) + 2$ for CLK Freq. ≤ 8 MHz
 $(\frac{1}{3} t_{CLCL}) + 6$ for CLK Freq. = 10 MHz
²⁾ $(\frac{2}{3} t_{CLCL}) - 15$ for CLK Freq. ≤ 8 MHz
 $(\frac{2}{3} t_{CLCL}) - 14$ for CLK Freq. = 10 MHz
³⁾ δ = EFI rise (5 ns max) + EFI fall (5 ns max).

- ⁴⁾ Setup and hold necessary only to guarantee recognition at next clock.
⁵⁾ Applies only to T_3 and T_W states.
⁶⁾ Applies only to T_2 states.
⁷⁾ 30 MHz for SAB 8284B-1

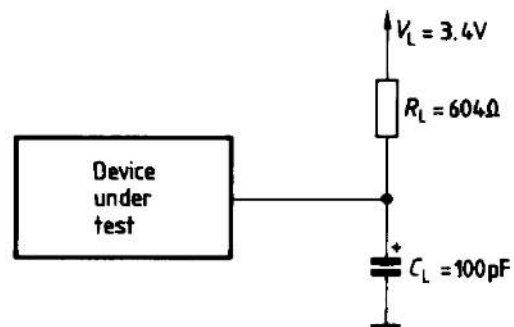
A.C. Testing

Input/Output Waveform

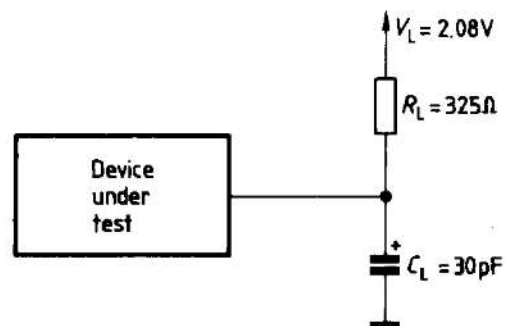


A.C. Testing: Input are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0".
Timing Measurements are made at 1.5 V for Both a Logic "1" and "0".

Load Circuit for CLK output

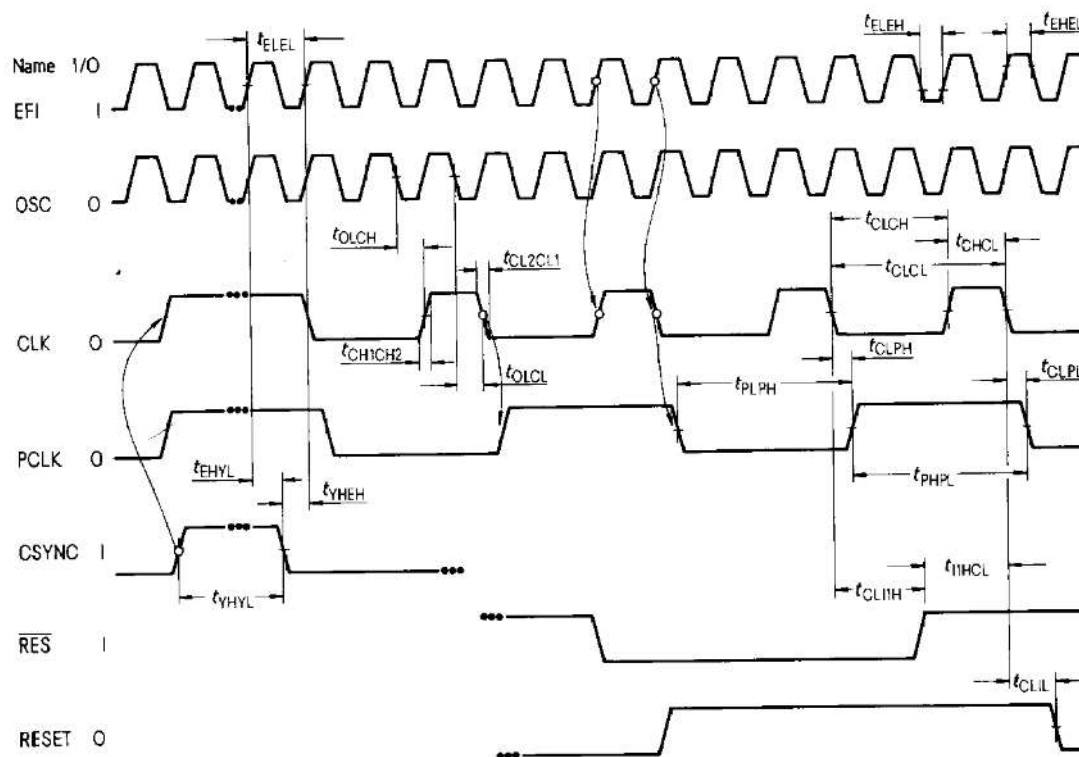


Load Circuit for all other output



Waveforms

Figure 4 Clocks and Reset Signals



Note: All timing measurements are made at 1.5V, unless otherwise noted.

Figure 5
Ready Signals – Asynchronous Devices

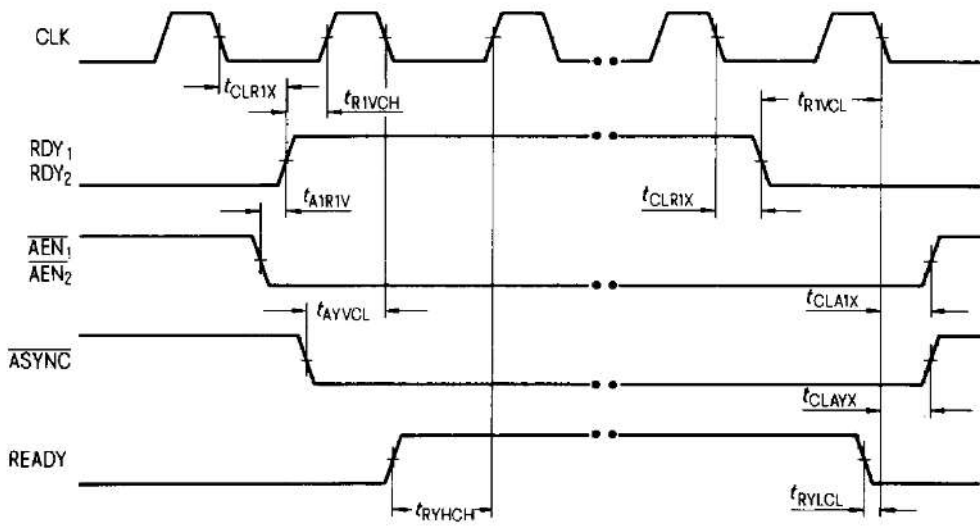
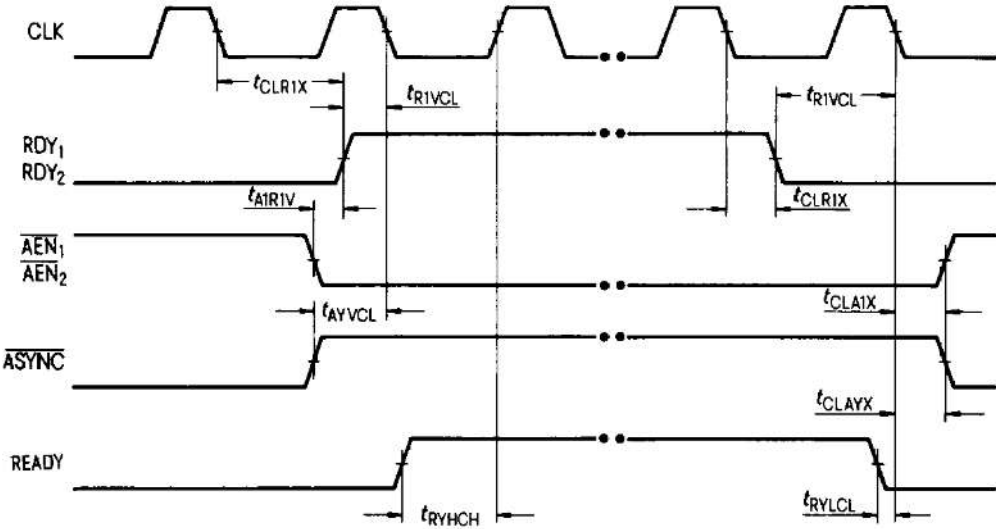


Figure 6
Ready Signals – Synchronous Devices



Testconditions

Figure 7
Clock High- and Low Time; Using X1, X2

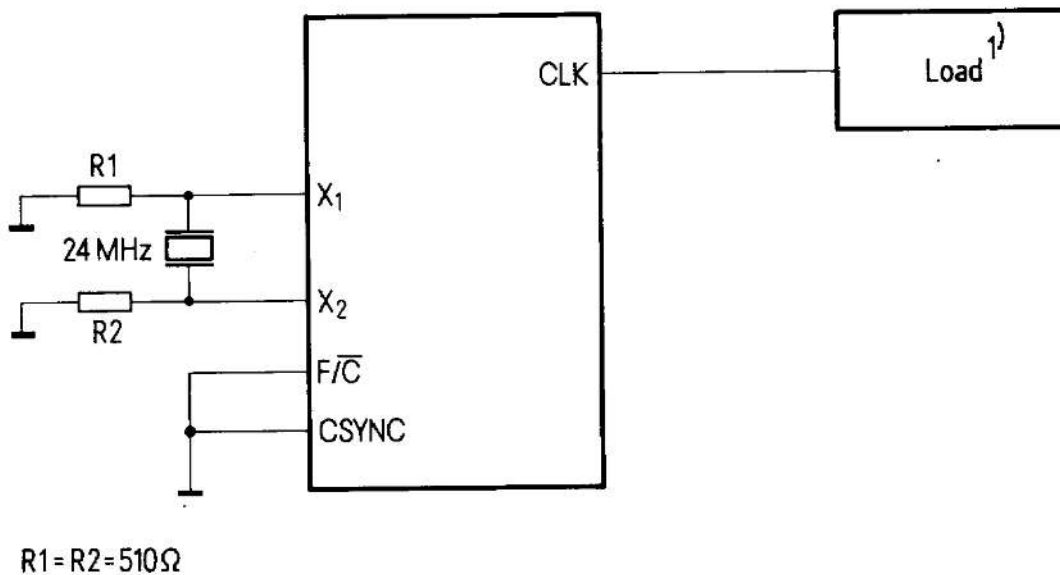
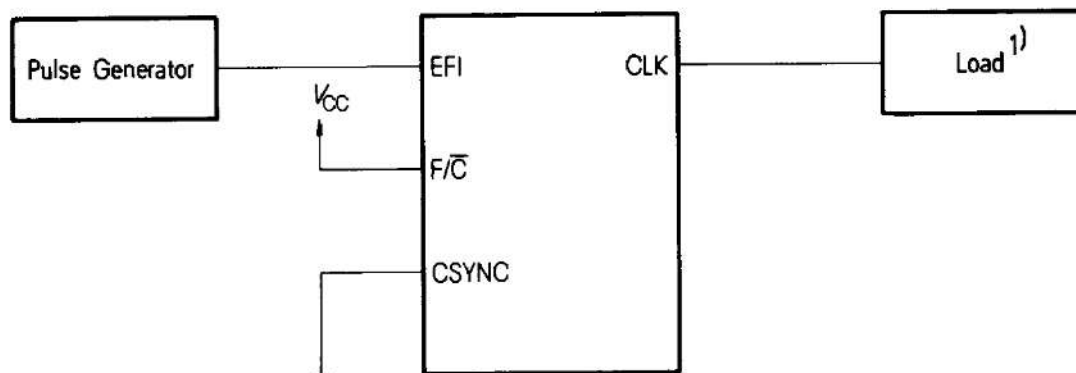


Figure 8
Clock High- and Low Time; Using EFI



1) $C_L = 100\text{ pF}$

Figure 9
Ready to Clock – Using X1, X2

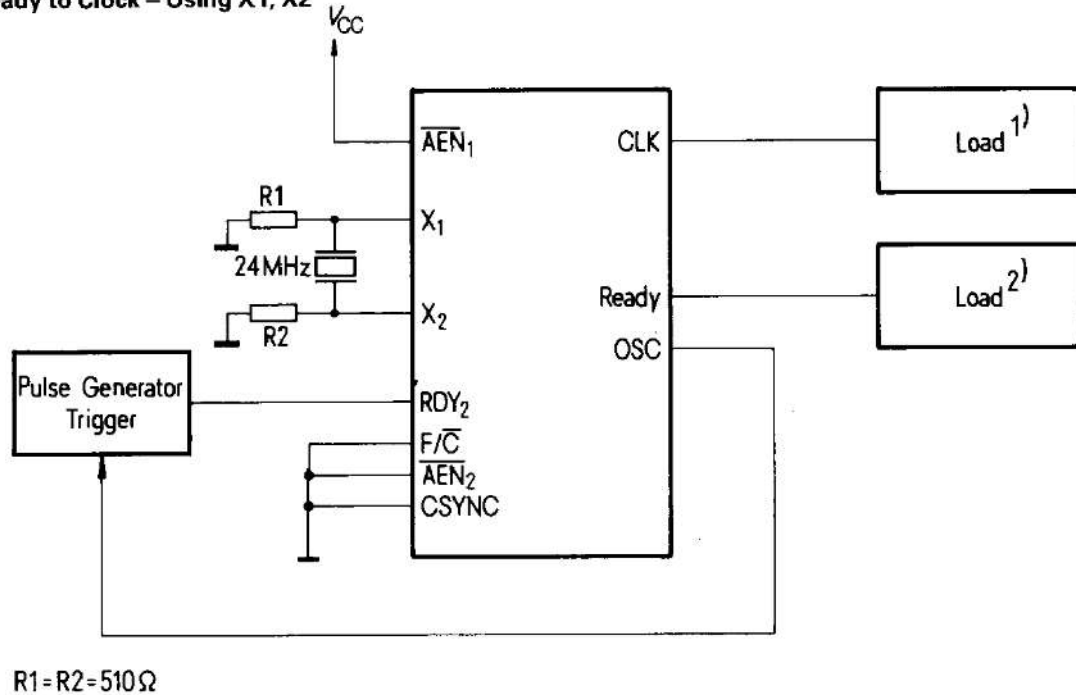
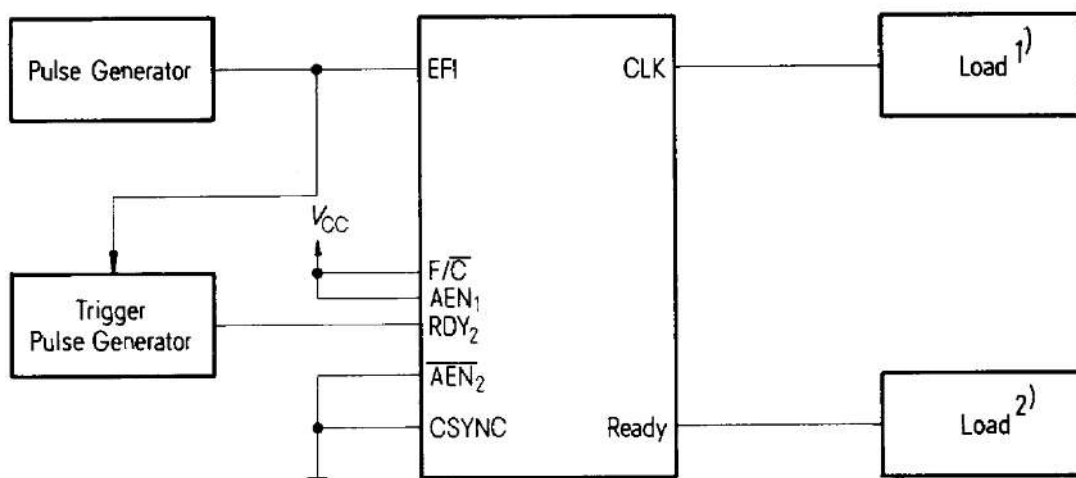


Figure 10
Ready to Clock – Using EFI



¹⁾ $C_L = 100 \text{ pF}$

²⁾ $C_L = 30 \text{ pF}$

SAB 8284B

Ordering Information

| Component | Description | Ordering Code |
|-----------------|------------------------------------|---------------|
| | Clock Generator- (Plastic Package) | |
| SAB 8284B – P | upto 8 MHz | Q67020–Y151 |
| SAB 8284B-1 – P | upto 10 MHz | Q67020–Y152 |