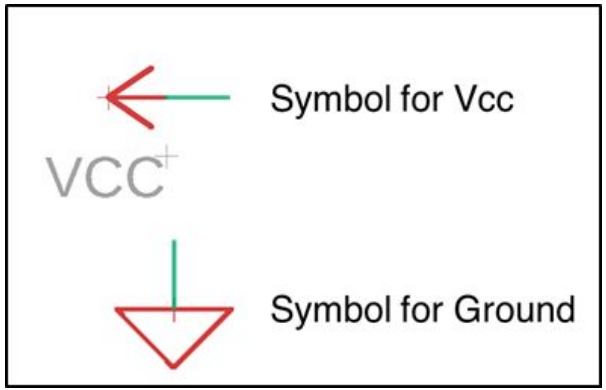
ON-PAPER DESIGN

Group-7

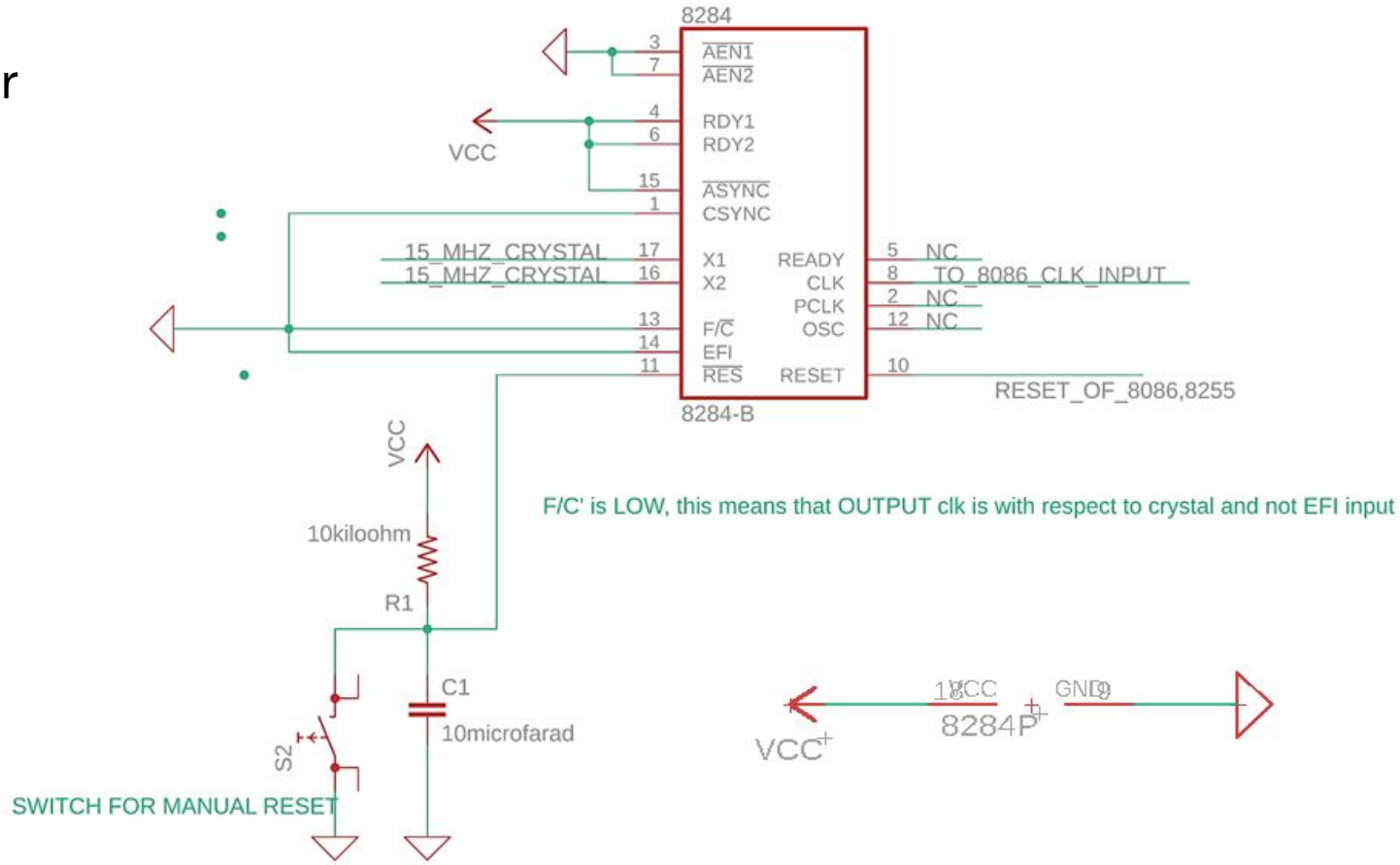
Batch Weighing Machine

MuP - 2020-21

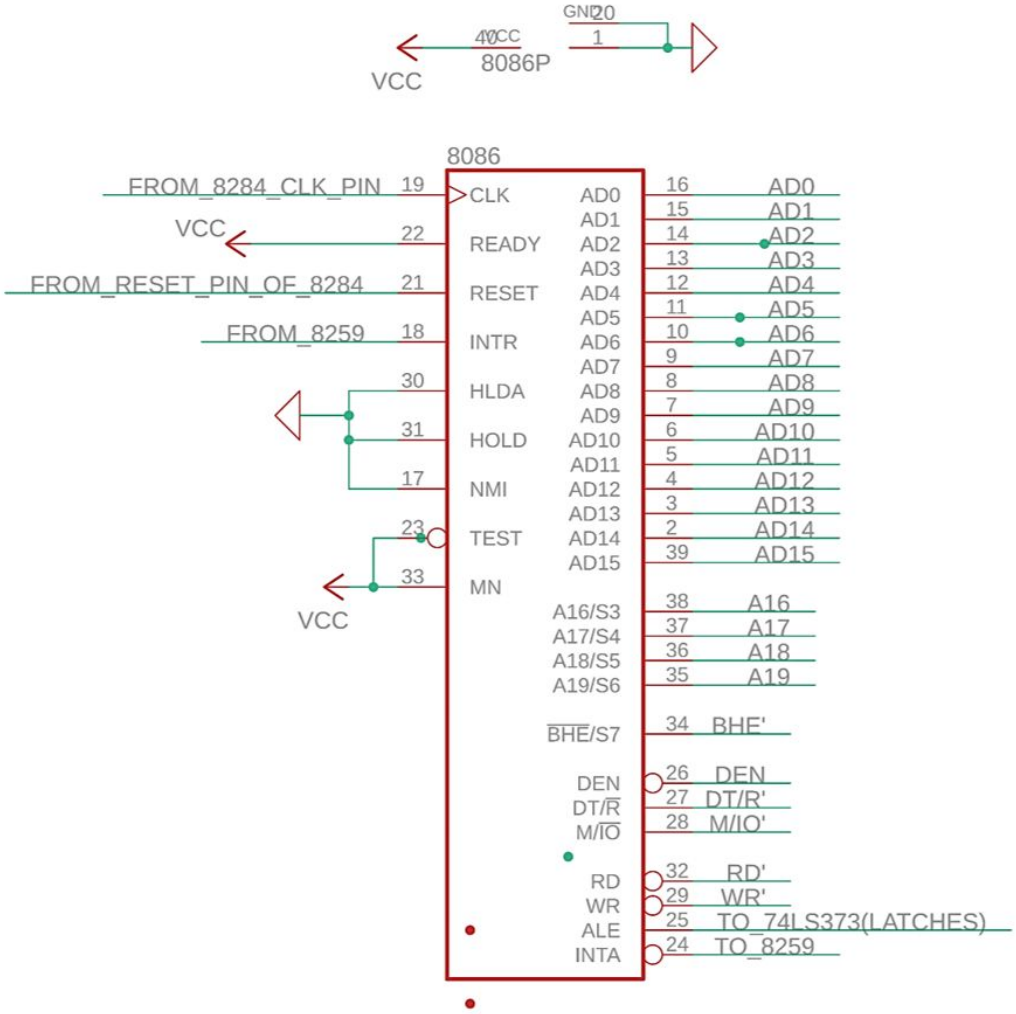
- In some places, Vcc and GND are not available on the chip. They have been shown separately near the chip
- All the Vcc's mentioned in the on paper design are 5V unless labelled explicitly giving a different voltage



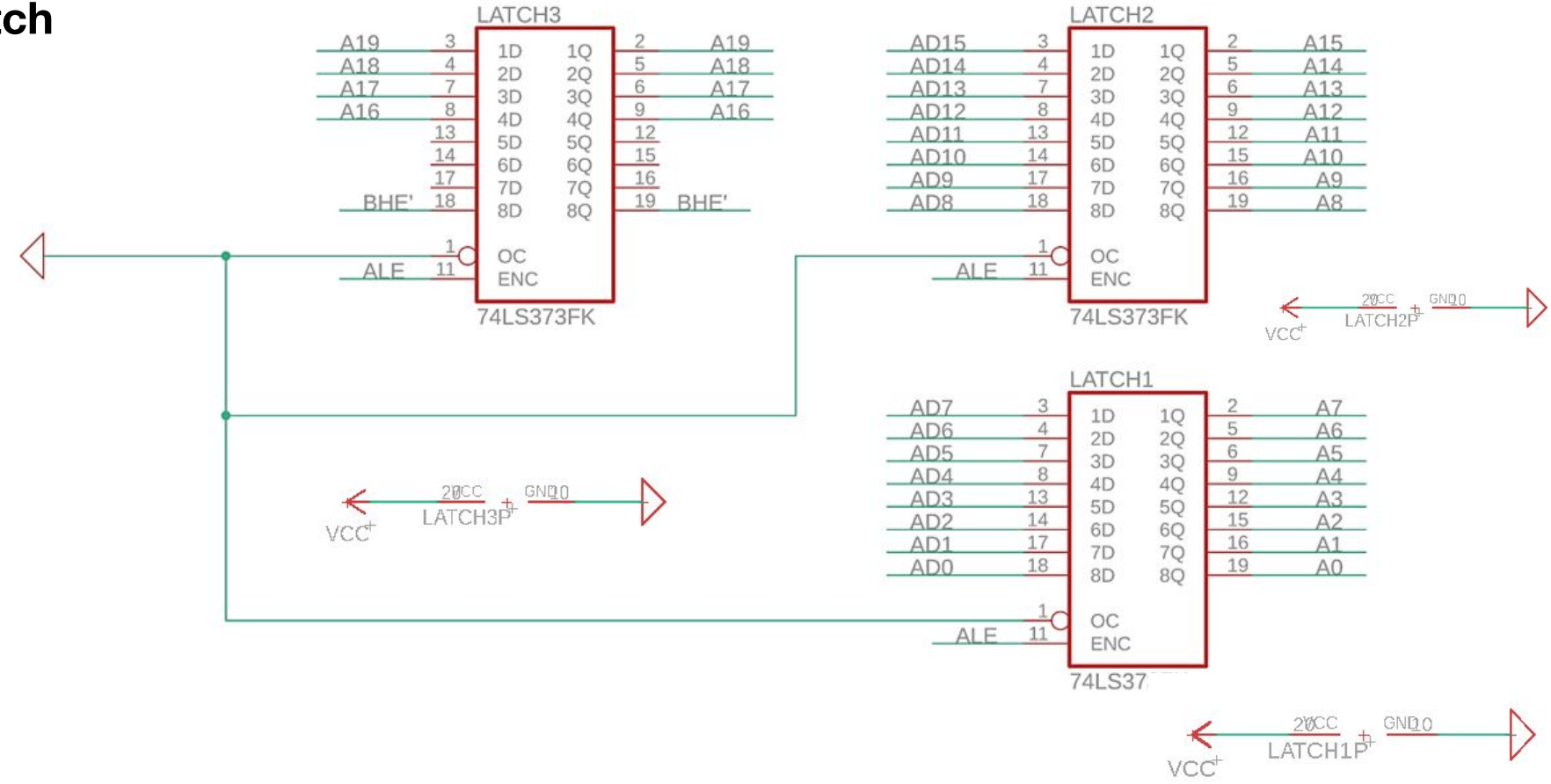
8284 -
Clock
Generator



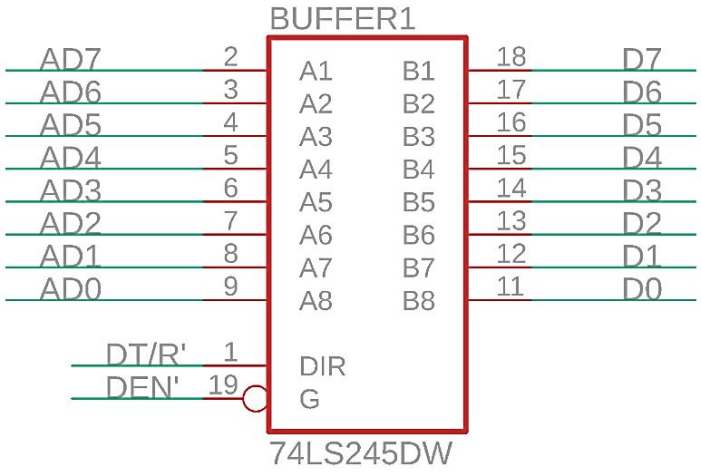
8086

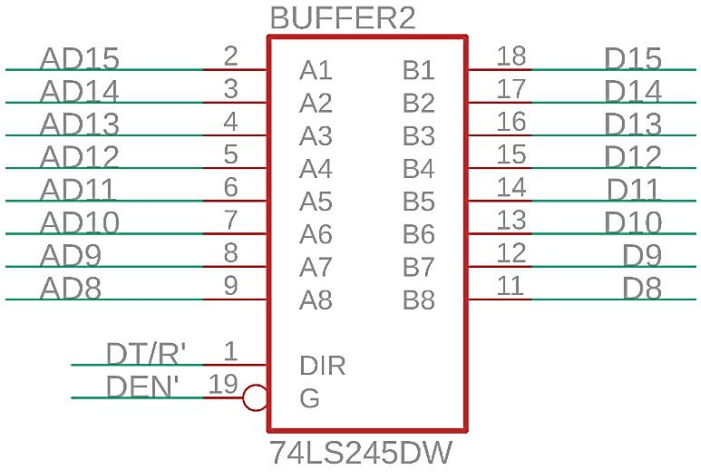

VCC
40
8086P
GND
20
1
8086
FROM_8284_CLK_PIN
19
CLK
VCC
22
READY
FROM_RESET_PIN_OF_8284
21
RESET
FROM_8259
18
INTR
30
HLDA
31
HOLD
17
NMI
23
TEST
33
MN
VCC
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
16 AD0
15 AD1
14 AD2
13 AD3
12 AD4
11 AD5
10 AD6
9 AD7
8 AD8
7 AD9
6 AD10
5 AD11
4 AD12
3 AD13
2 AD14
39 AD15
A16/S3
A17/S4
A18/S5
A19/S6
38 A16
37 A17
36 A18
35 A19
BHE/S7
34 BHE'
DEN
DT/R
M/IO
26 DEN
27 DT/R'
28 M/IO'
RD
WR
ALE
INTA
32 RD'
29 WR'
25 TO_74LS373(LATCHES)
24 TO_8259

74LS373
Latch

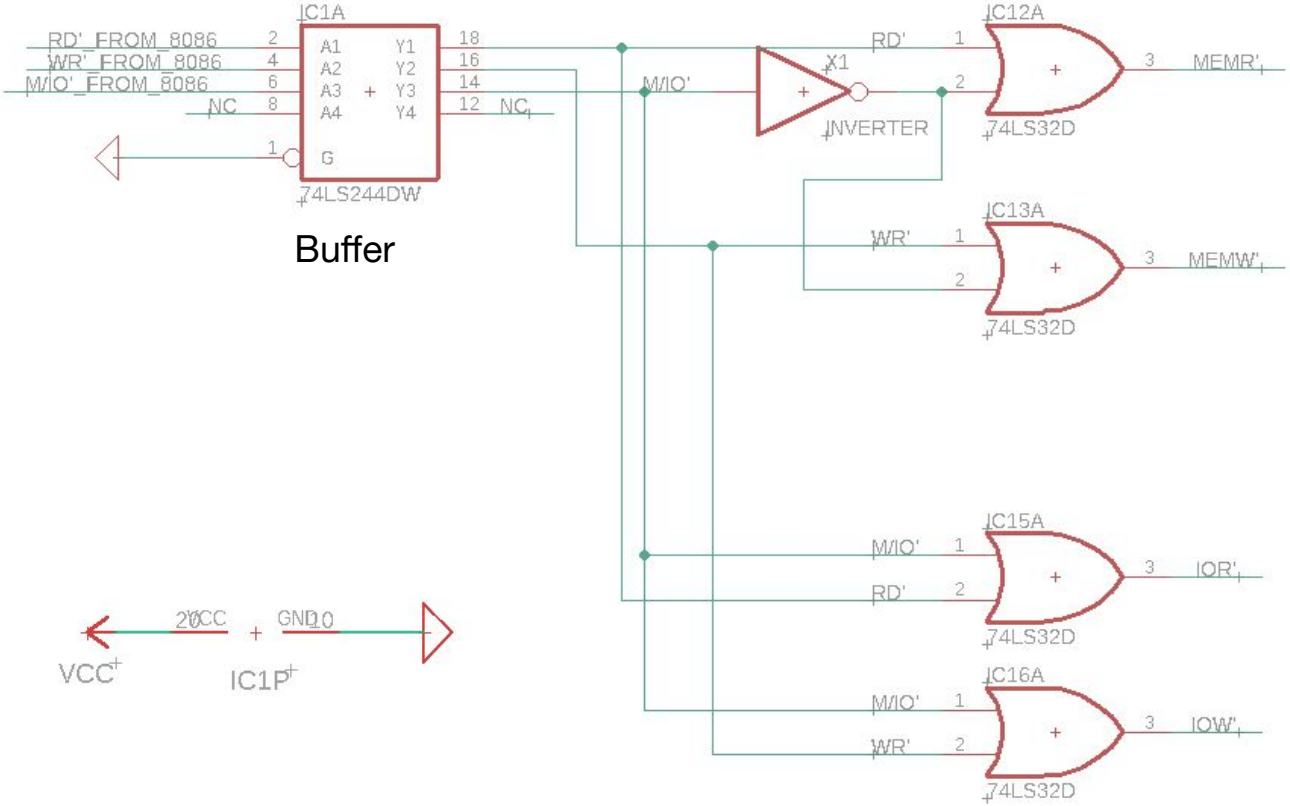


Data Bus Buffers





Control Signals



Logic for the formation of control signals

M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

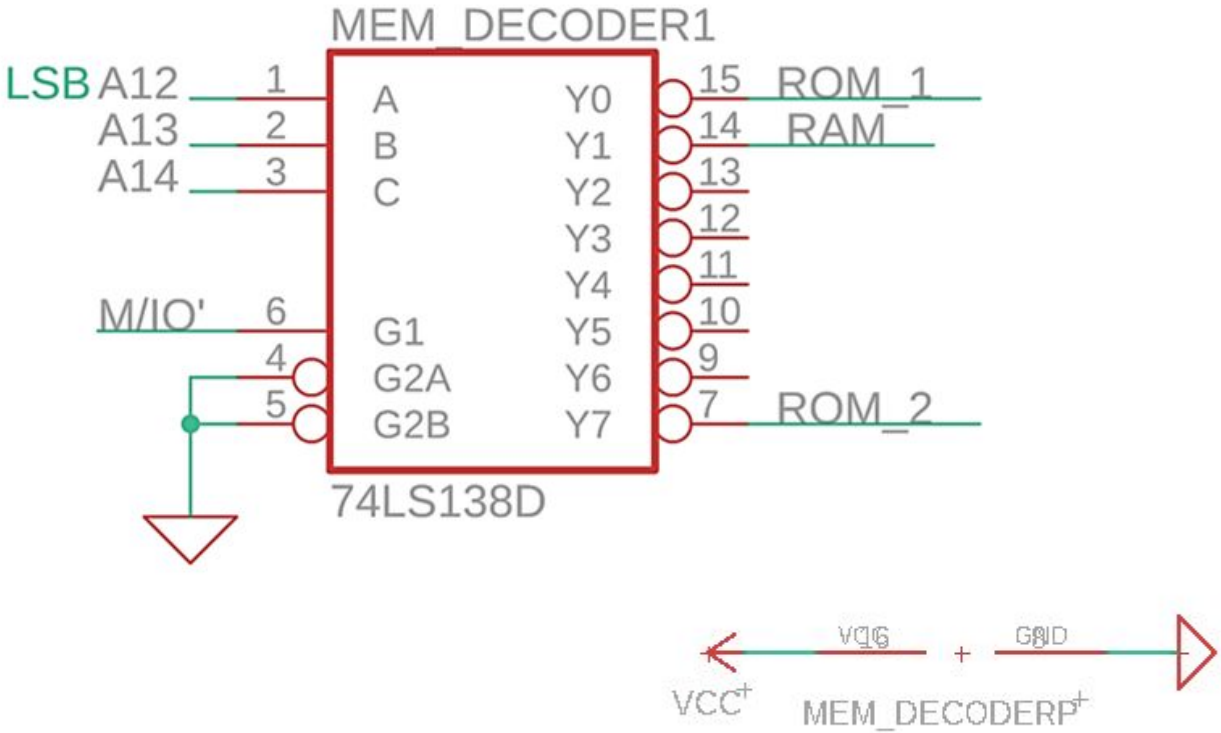
Chip Select for even, odd banks

RAM_FROM
MEMORY DECODER

ROM_1_FROM
MEMORY DECODER

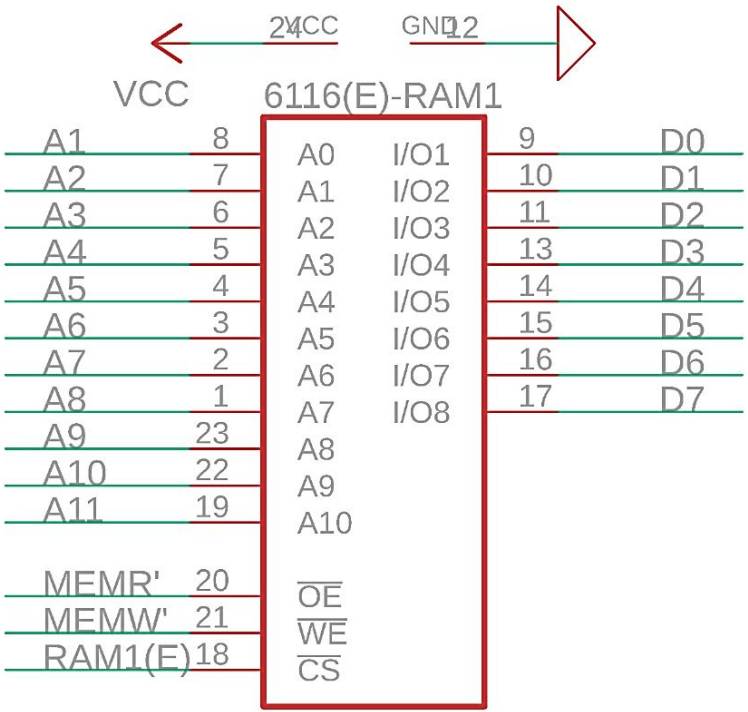
ROM_2_FROM
MEMORY DECODER

74LS138 -
Memory Decoder

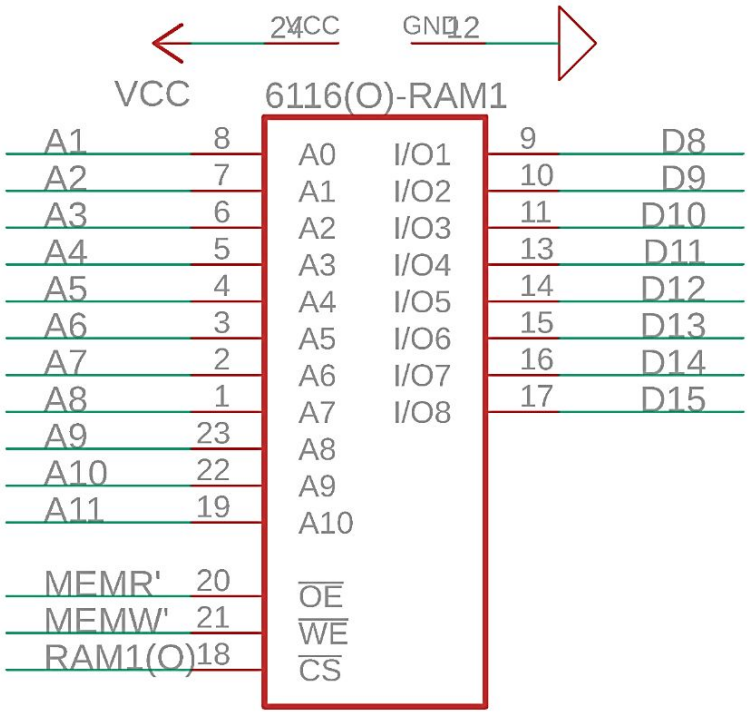


6116-
2K RAM

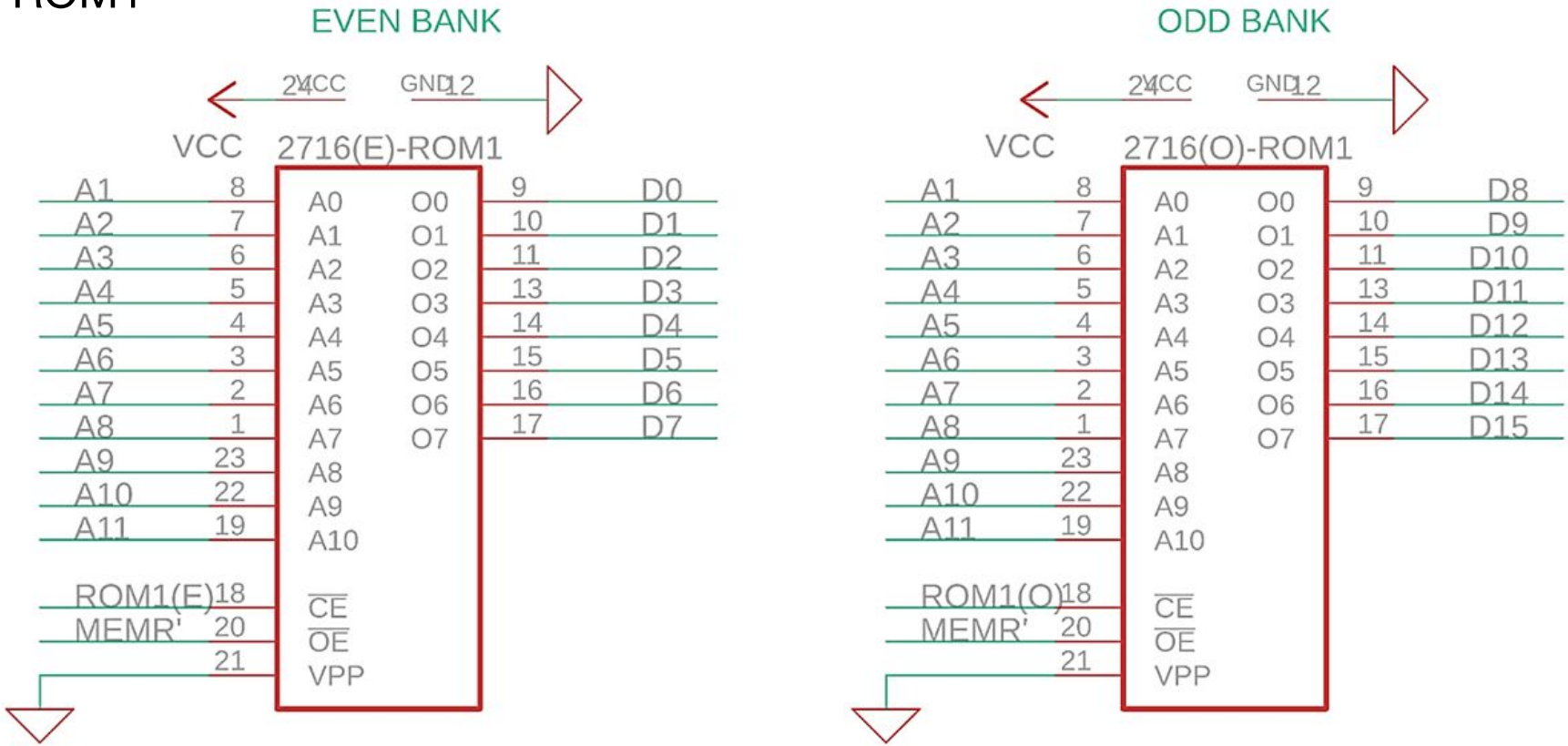
EVEN BANK



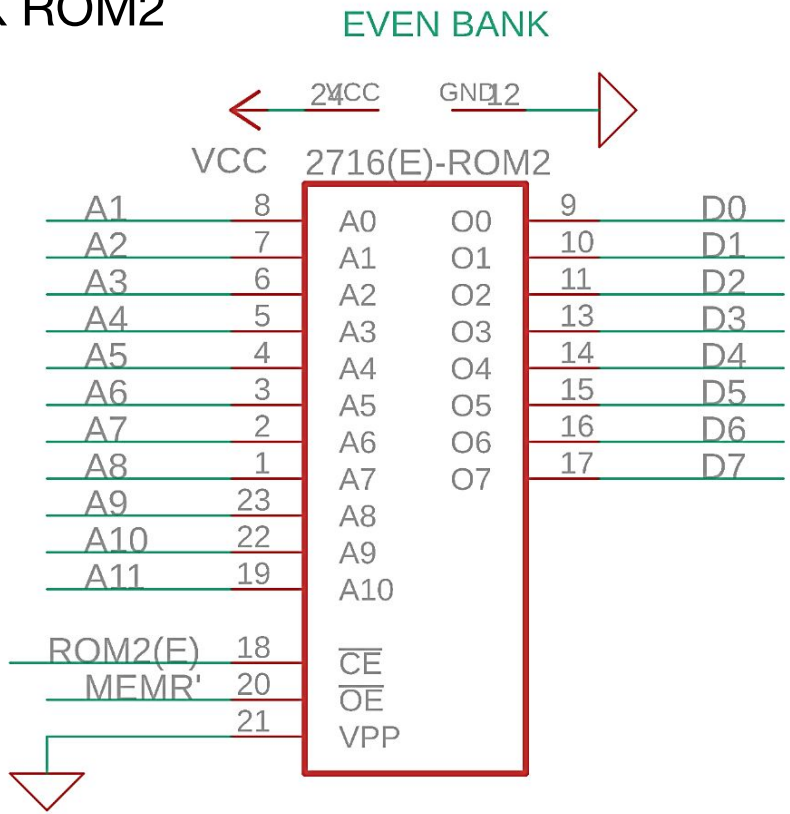
ODD BANK

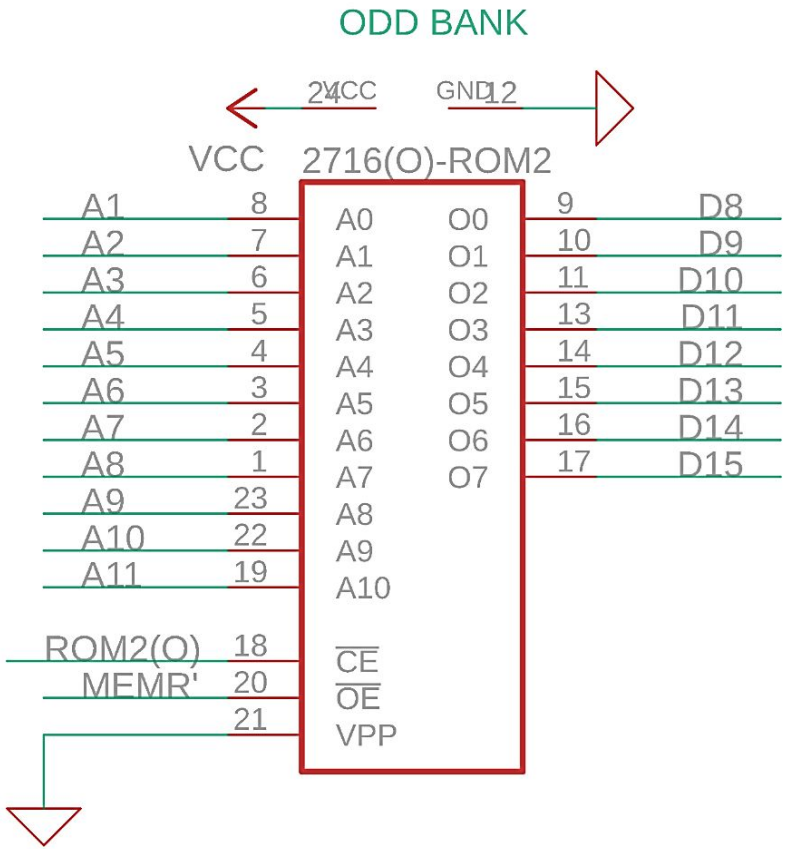


2716-
2K ROM1

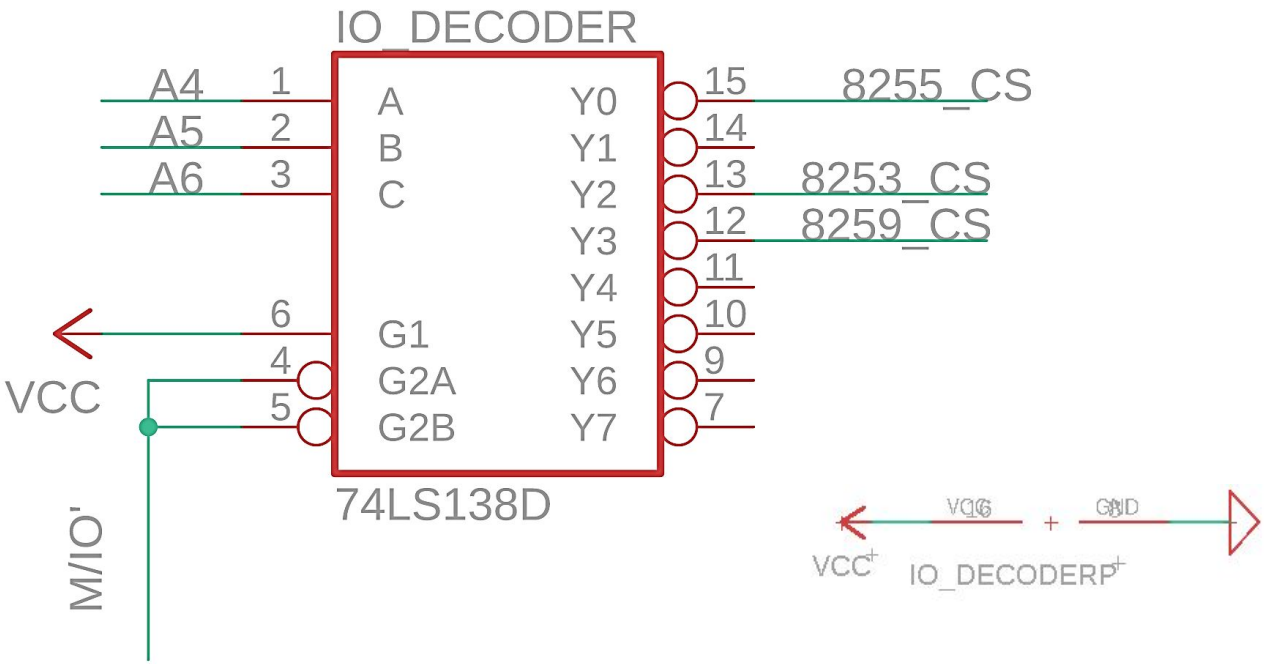

EVEN BANK
24 VCC
GND 12
VCC
2716(E)-ROM1
A1 8
A2 7
A3 6
A4 5
A5 4
A6 3
A7 2
A8 1
A9 23
A10 22
A11 19
ROM1(E) 18
MEMR' 20
21
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE
OE
VPP
O0 9 D0
O1 10 D1
O2 11 D2
O3 13 D3
O4 14 D4
O5 15 D5
O6 16 D6
O7 17 D7
ODD BANK
24 VCC
GND 12
VCC
2716(O)-ROM1
A1 8
A2 7
A3 6
A4 5
A5 4
A6 3
A7 2
A8 1
A9 23
A10 22
A11 19
ROM1(O) 18
MEMR' 20
21
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE
OE
VPP
O0 9 D8
O1 10 D9
O2 11 D10
O3 13 D11
O4 14 D12
O5 15 D13
O6 16 D14
O7 17 D15

2716-
2K ROM2

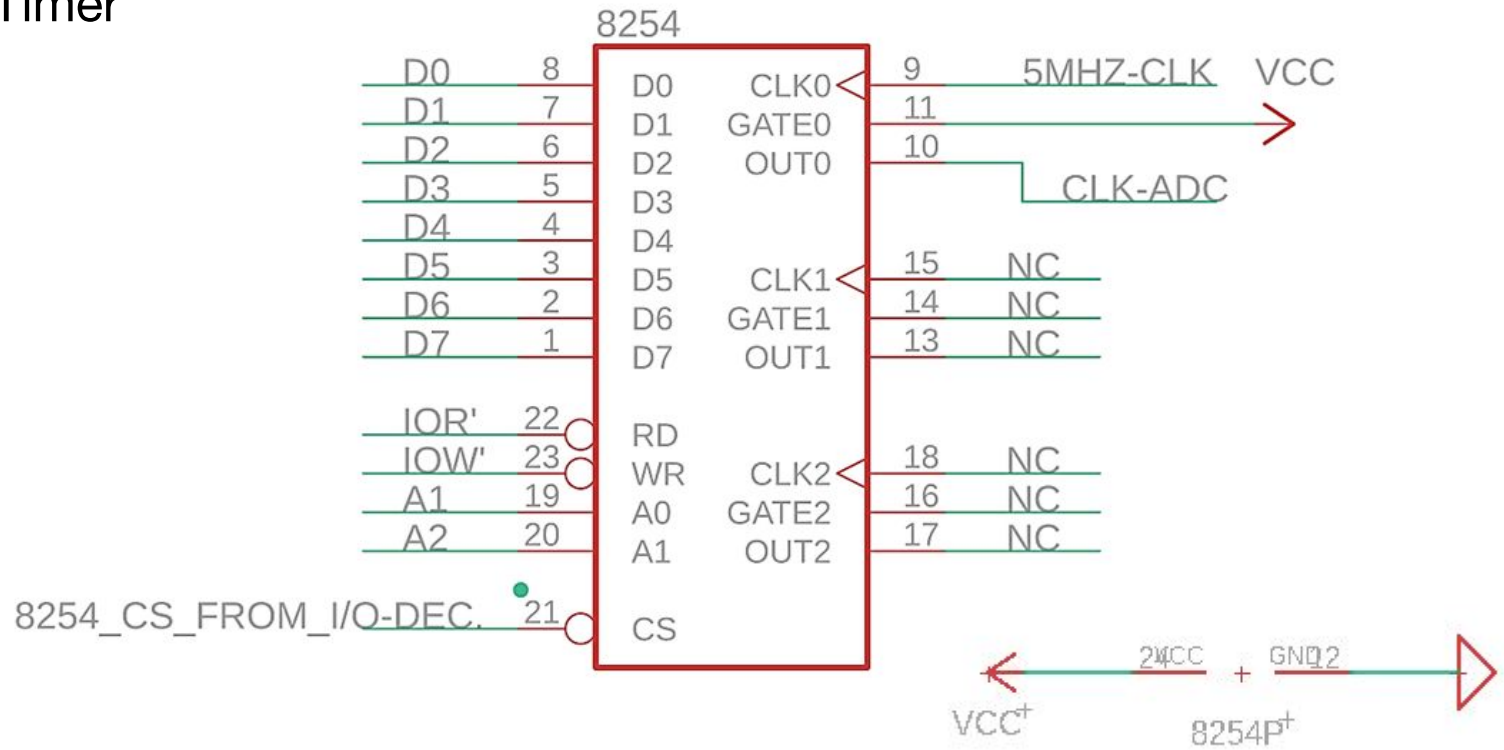

EVEN BANK
24 VCC
12 GND
VCC
2716(E)-ROM2
A1 8
A2 7
A3 6
A4 5
A5 4
A6 3
A7 2
A8 1
A9 23
A10 22
A11 19
ROM2(E) 18
MEMR' 20
21
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE
OE
VPP
O0 9 D0
O1 10 D1
O2 11 D2
O3 13 D3
O4 14 D4
O5 15 D5
O6 16 D6
O7 17 D7


ODD BANK
24 VCC
12 GND
VCC
2716(O)-ROM2
A1 8
A2 7
A3 6
A4 5
A5 4
A6 3
A7 2
A8 1
A9 23
A10 22
A11 19
ROM2(O) 18
MEMR' 20
21
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
CE
OE
VPP
O0 9 D8
O1 10 D9
O2 11 D10
O3 13 D11
O4 14 D12
O5 15 D13
O6 16 D14
O7 17 D15

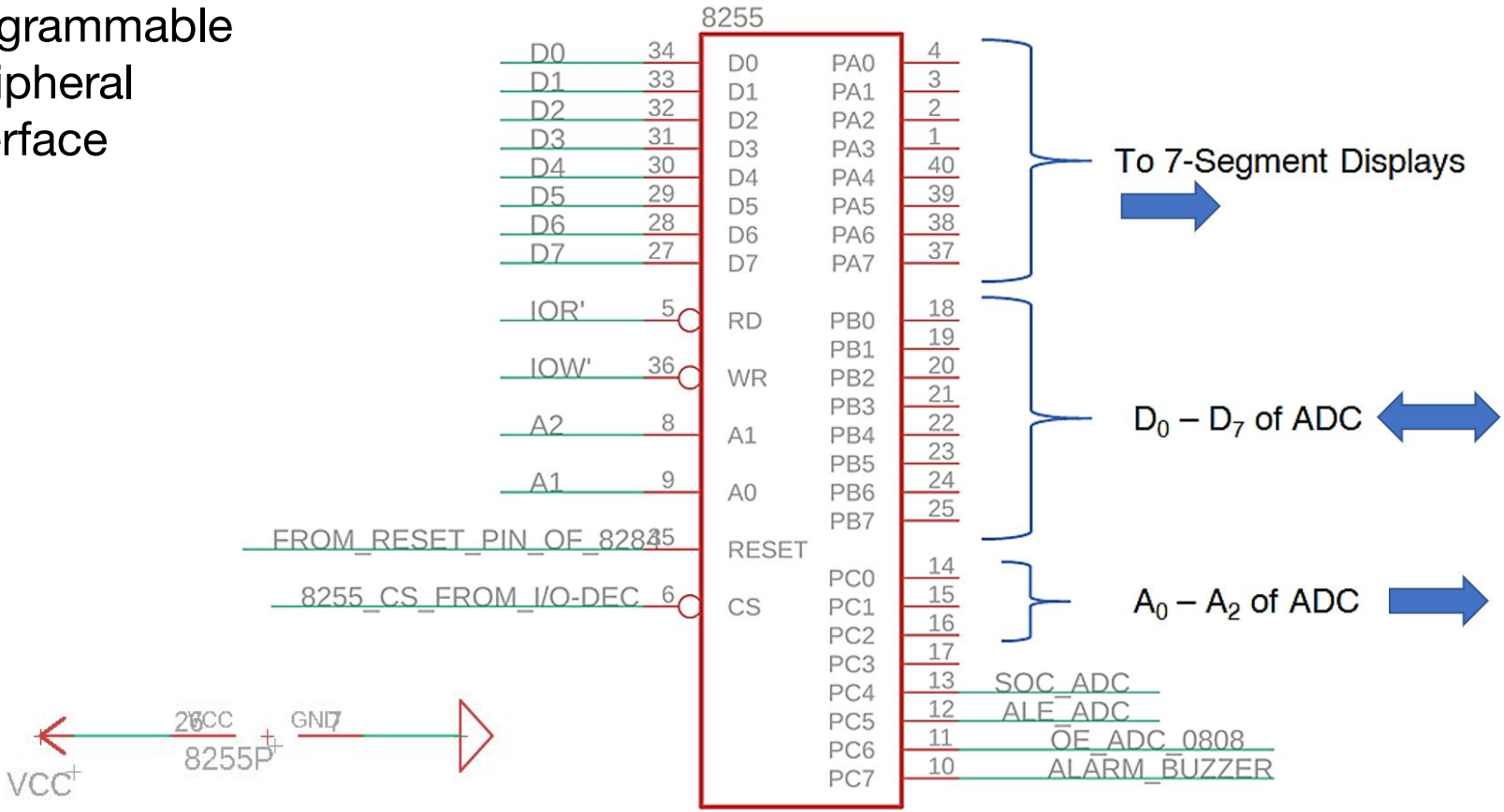
74LS138 -
IO
Decoder



8254 -
Programmable
Interval Timer



8255 -
Programmable
Peripheral
Interface



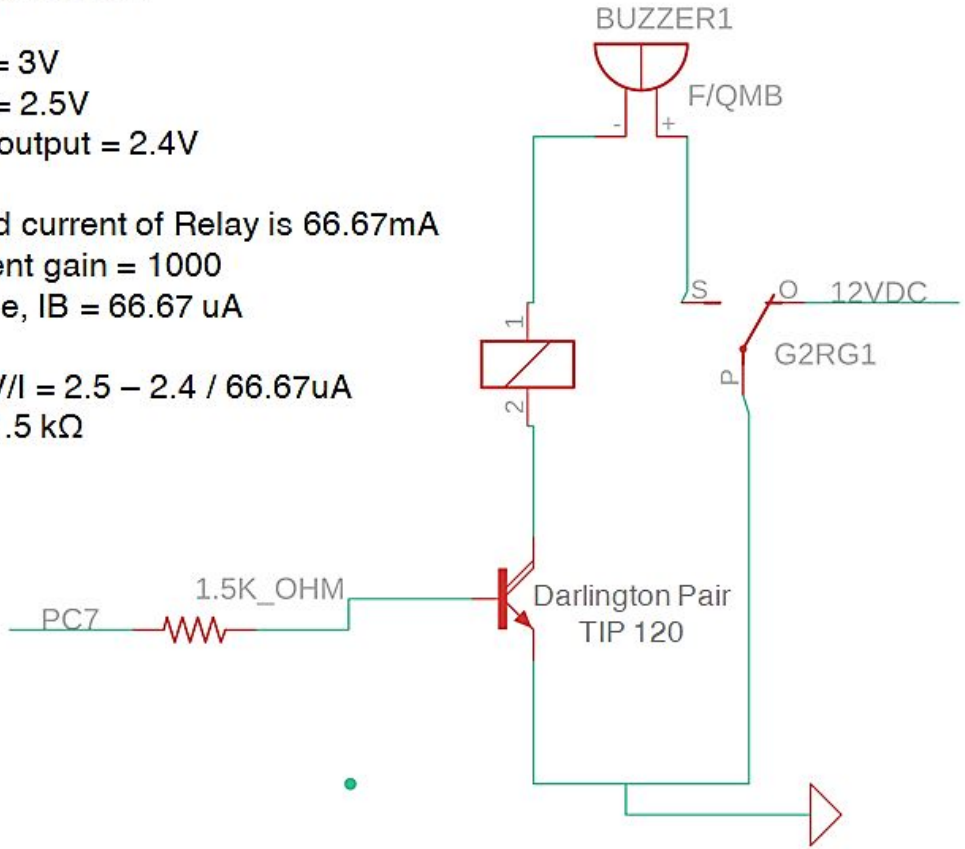
Relay for Alarm

Darlington Pair

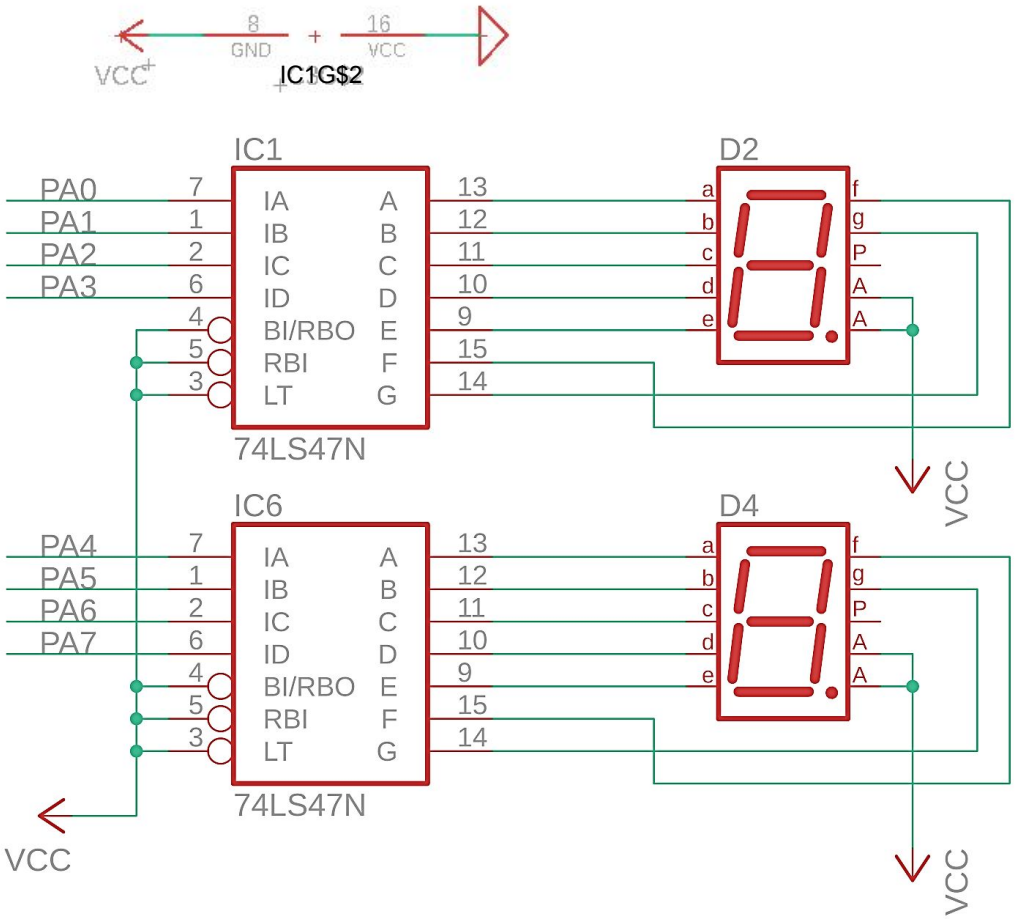
Vce = 3V
Vbe = 2.5V
PC7 output = 2.4V

Rated current of Relay is 66.67mA
Current gain = 1000
Hence, IB = 66.67 uA

R = V/I = 2.5 – 2.4 / 66.67uA
R = 1.5 kΩ



74LS47N & 7-segment displays
(common anode)



Units Place

10s Place

ADC 0808 - Analog-Digital Convertor

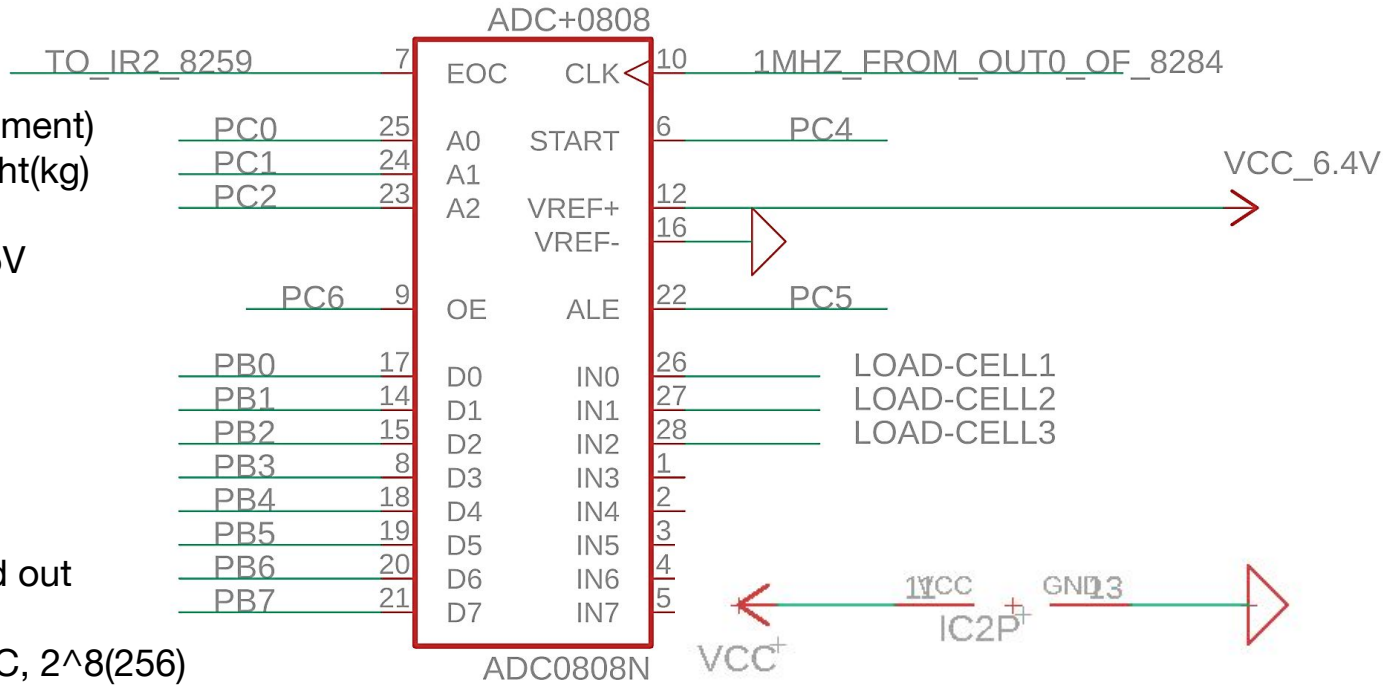
Vout (given in Problem Statement) for Load Cell = 0.025 x weight(kg)

Therefore resolution is 0.025V (25mV)

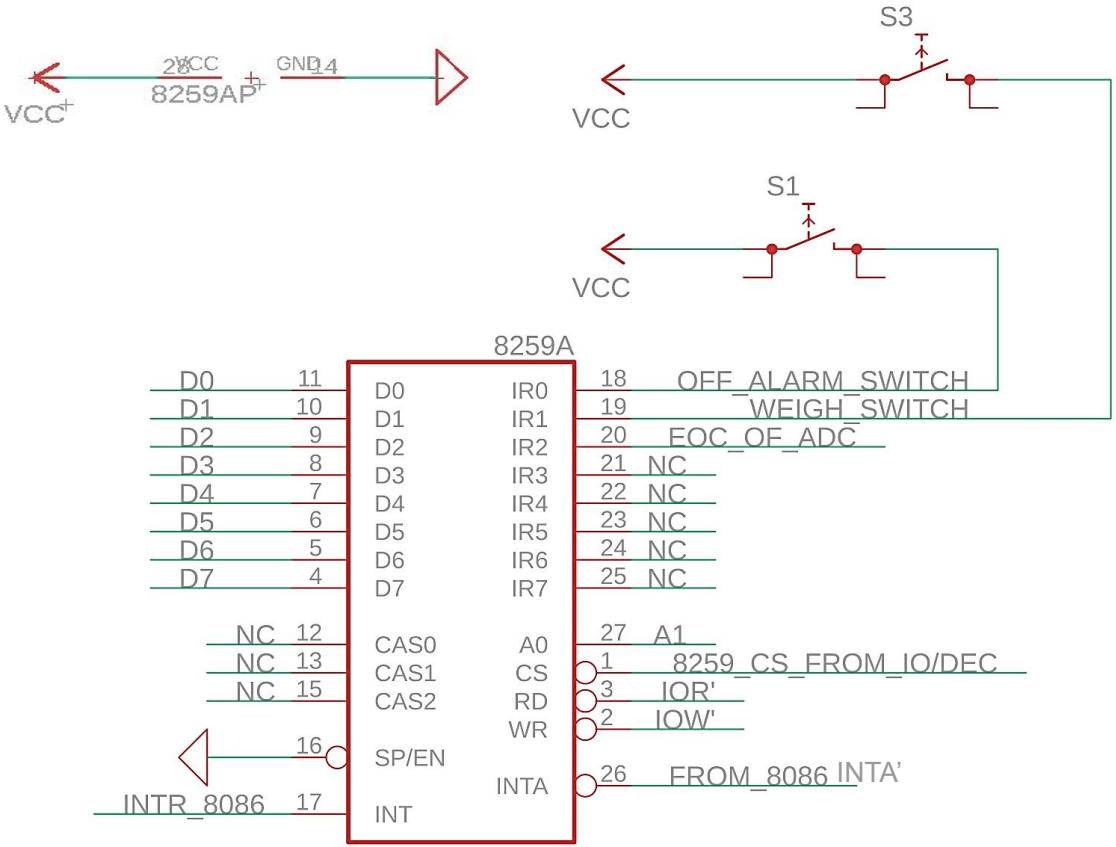
Now,
X / 256 = 0.025
X = 6.4 V

Where X is Vref+ to be found out

Since we are using 8-bit ADC, 2^8(256) mappings are possible



8259 - Interrupt Controller



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