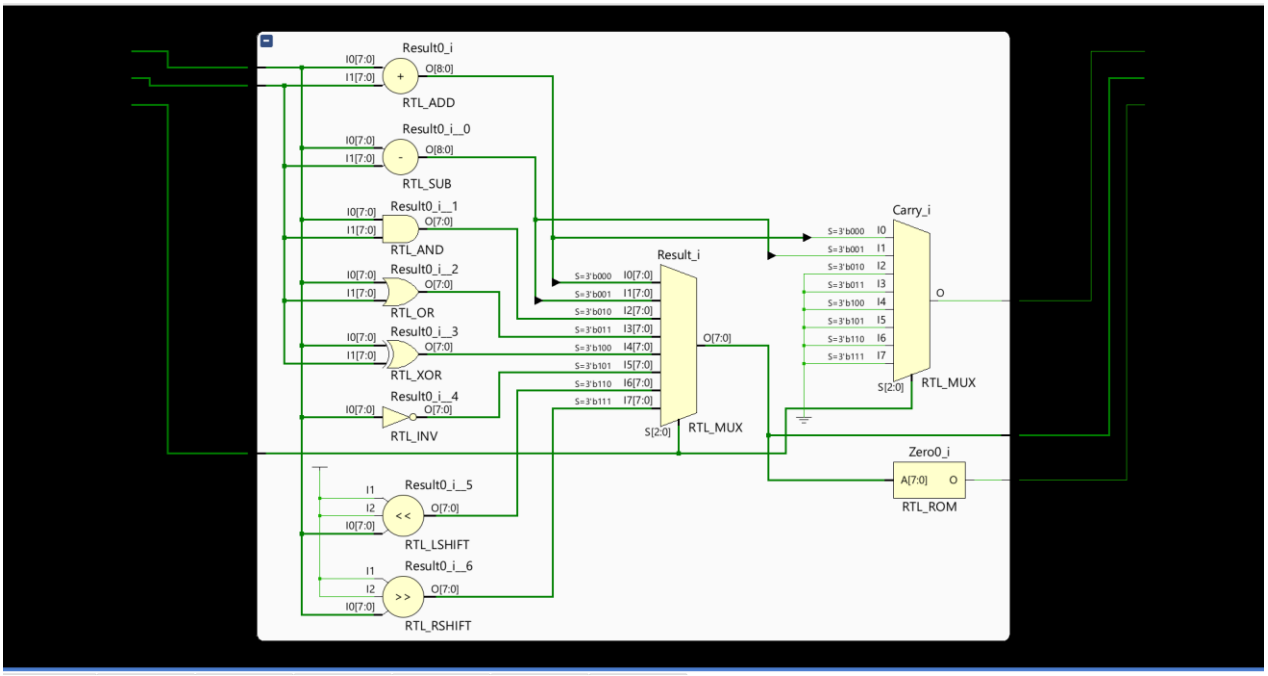
VLSI Design:

8-Bit Arithmetic Logic Unit (ALU) Using Verilog on Xilinx Vivado



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1. Project Title

Design and FPGA Implementation of an 8-bit ALU using Verilog on Xilinx Vivado

2. Objective

To design, simulate, and implement a functional 8-bit Arithmetic Logic Unit (ALU) that performs a set of arithmetic and logical operations using Verilog HDL. The design is targeted for simulation and future FPGA implementation on the Nexys A7 board.

3. Tools Used

- Xilinx Vivado – RTL design, simulation, synthesis, implementation, and bitstream generation.

4. ALU Functional Description

The ALU accepts two 8-bit inputs A and B, a 3-bit Opcode, and provides:
- An 8-bit output Result
- A Zero flag indicating a result of zero
- A Carry flag for arithmetic operations

5. Supported Operations

Opcode	**Operation**	**Description**
000	A + B	Addition
001	A - B	Subtraction
010	A & B	Bitwise AND
011	A | B	Bitwise OR
100	A ^ B	Bitwise XOR
101	~A	Bitwise NOT of A
110	A << 1	Logical left shift
111	A >> 1	Logical right shift

6. Verilog Design

A parameterized combinational ALU was written in Verilog. The always @(*) block uses a case statement to handle operations based on the opcode. Flags (Zero, Carry) are computed accordingly.

7. Simulation

- Testbenches were written to verify all operations with representative input values.
- Waveforms were generated in Vivado to verify correctness of output.
- Edge cases such as carry overflow and zero output were included.

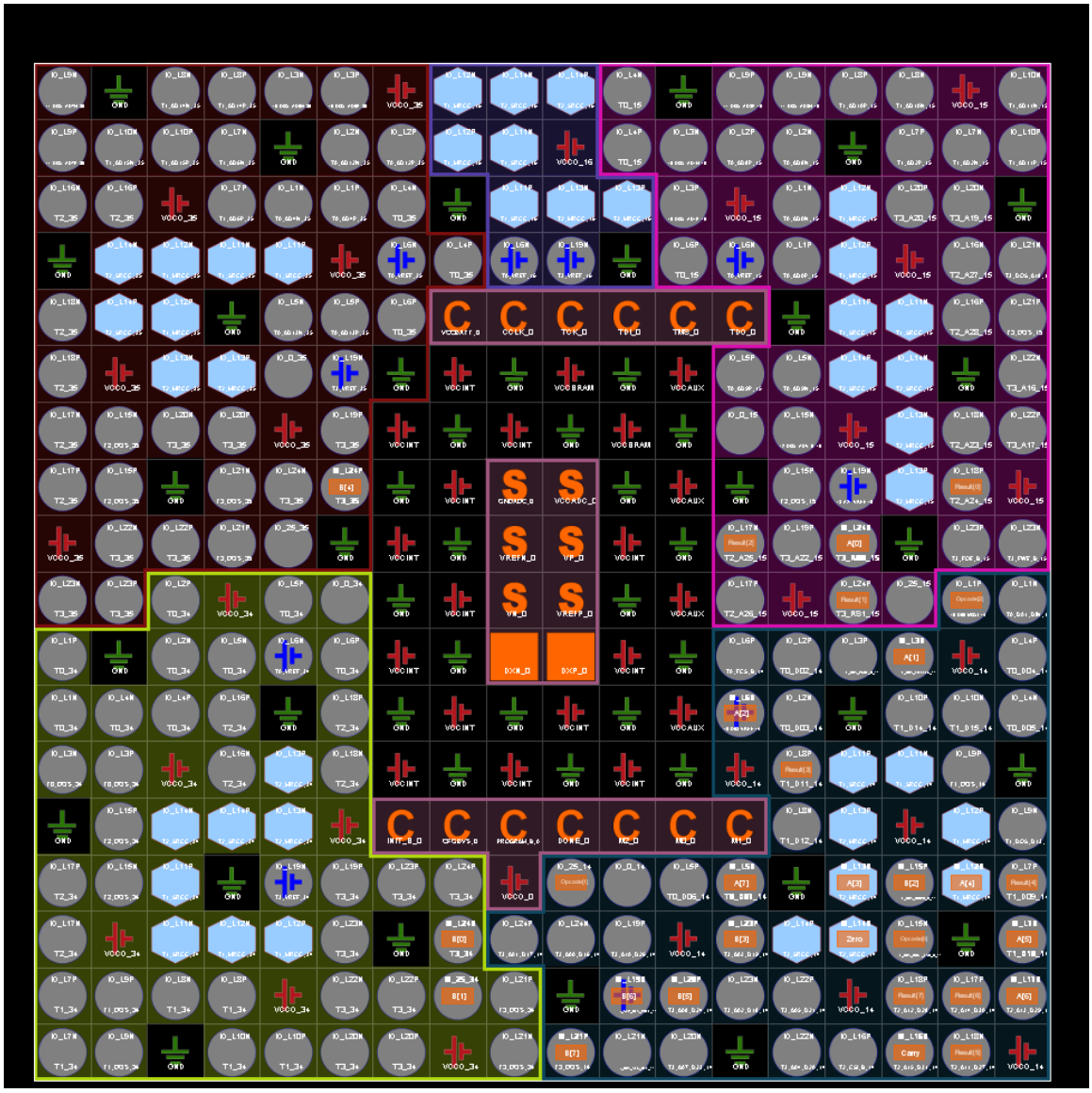

Figure 1: Pin Assignments on Nexys A7 FPGA

8. RTL Schematic

- RTL and Technology schematics were auto-generated by Vivado.
- Logic gates and MUXes were visually inspected to validate internal structure.

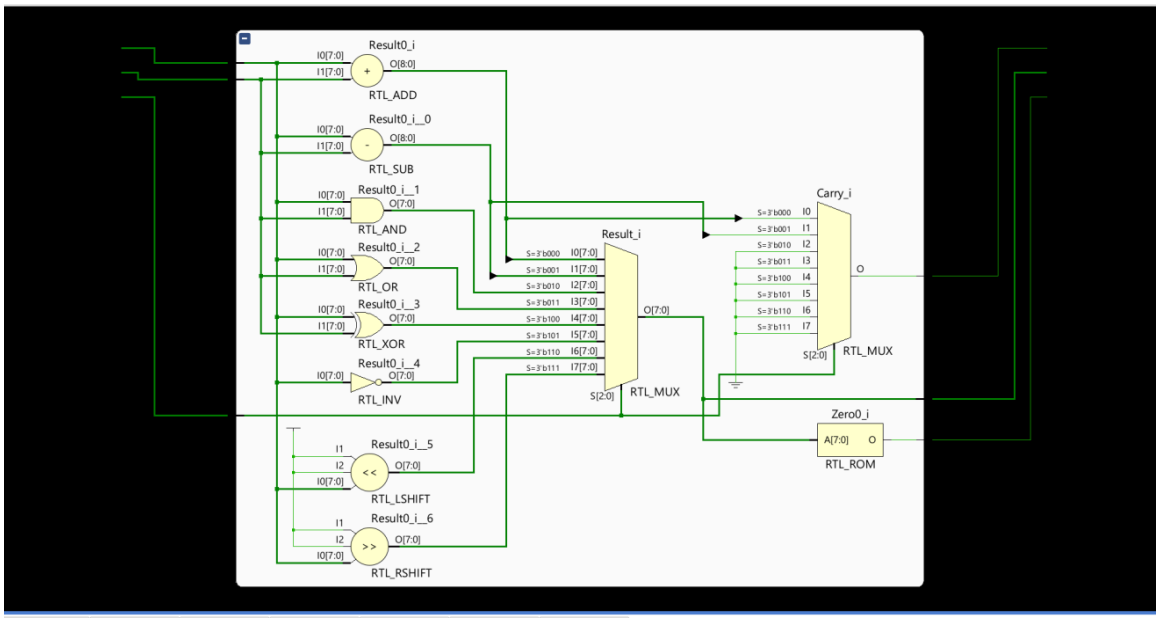

Figure 2: RTL Schematic of the 8-bit ALU

9. FPGA Implementation

- Target Board: Digilent Nexys A7 (Artix-7 FPGA)
- A complete XDC constraint file was written, assigning input/output signals to physical switches, buttons, and LEDs on the board.
- Bitstream was generated successfully after resolving DRC and IO constraint errors.
- Although actual hardware verification was not possible due to unavailability of the board, the project is fully implementation-ready.

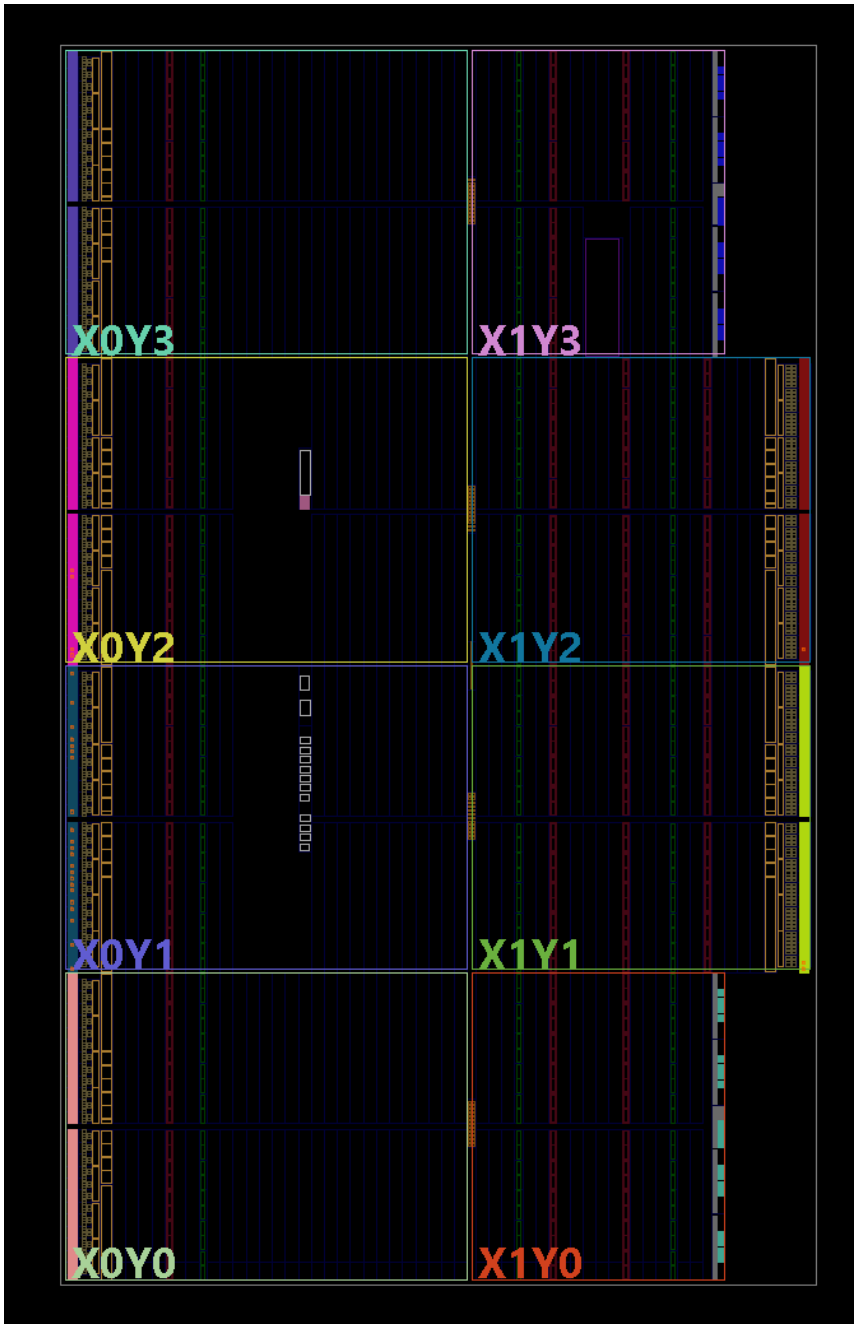

Figure 3: Implementation of 8-bit ALU on the Nexys A7 board

10. Skills Gained

- RTL Design using Verilog HDL
- Testbench creation and waveform analysis
- Combinational circuit design
- Static Timing Analysis using Vivado
- FPGA bitstream generation and IO constraints mapping
- Understanding of FPGA toolchain and implementation flow

11. Future Scope

- Extend this design into a pipelined ALU
- Integrate with a simple processor (RISC-V or custom ISA)
- Add signed operations, multiplication, and division
- Interface with peripherals via UART or GPIO