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Release 14.7 Trace (lin64)

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/opt/Xilinx/14.7/ISE\_DS/ISE/bin/lin64/unwrapped/trce -intstyle ise -v 3 -s 3 -n

3 -fastpaths -xml test.twx test.ncd -o test.twr test.pcf

Design file: test.ncd

Physical constraint file: test.pcf

Device,package,speed: xc7a100t,csg324,C,-3 (PRODUCTION 1.10 2013-10-13)

Report level: verbose report

Environment Variable Effect

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NONE No environment variables were set

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INFO:Timing:2698 - No timing constraints found, doing default enumeration.

INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).

INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths

option. All paths that are not constrained will be reported in the

unconstrained paths section(s) of the report.

INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on

a 50 Ohm transmission line loading model. For the details of this model,

and for more information on accounting for different loading conditions,

please see the device datasheet.

Data Sheet report:

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All values displayed in nanoseconds (ns)

Setup/Hold to clock Clk

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|Max Setup to| Process |Max Hold to | Process | | Clock |

Source | clk (edge) | Corner | clk (edge) | Corner |Internal Clock(s) | Phase |

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A | 0.101(R)| FAST | 1.883(R)| SLOW |Clk\_BUFGP | 0.000|

B | 0.019(R)| FAST | 1.997(R)| SLOW |Clk\_BUFGP | 0.000|

C | 0.241(R)| FAST | 1.667(R)| SLOW |Clk\_BUFGP | 0.000|

D | 0.071(R)| FAST | 1.912(R)| SLOW |Clk\_BUFGP | 0.000|

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Clock Clk to Pad

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|Max (slowest) clk| Process |Min (fastest) clk| Process | | Clock |

Destination | (edge) to PAD | Corner | (edge) to PAD | Corner |Internal Clock(s) | Phase |

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Q | 6.366(R)| SLOW | 2.783(R)| FAST |Clk\_BUFGP | 0.000|

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Analysis completed Mon Feb 24 19:53:07 2025

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Trace Settings:

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Trace Settings

Peak Memory Usage: 763 MB