

ASSIGNMENT 4

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Division: - 04

Year: - 2023-24

Subject: - Digital System Design (3EL42)

Branch: - Electronics (EL)

Q1. BCD TIMECOUNT

VERILOG CODE:-

```
module bcd_Count(
    input clock, reset,
    output reg [3:0]dout
);
initial dout = 0;

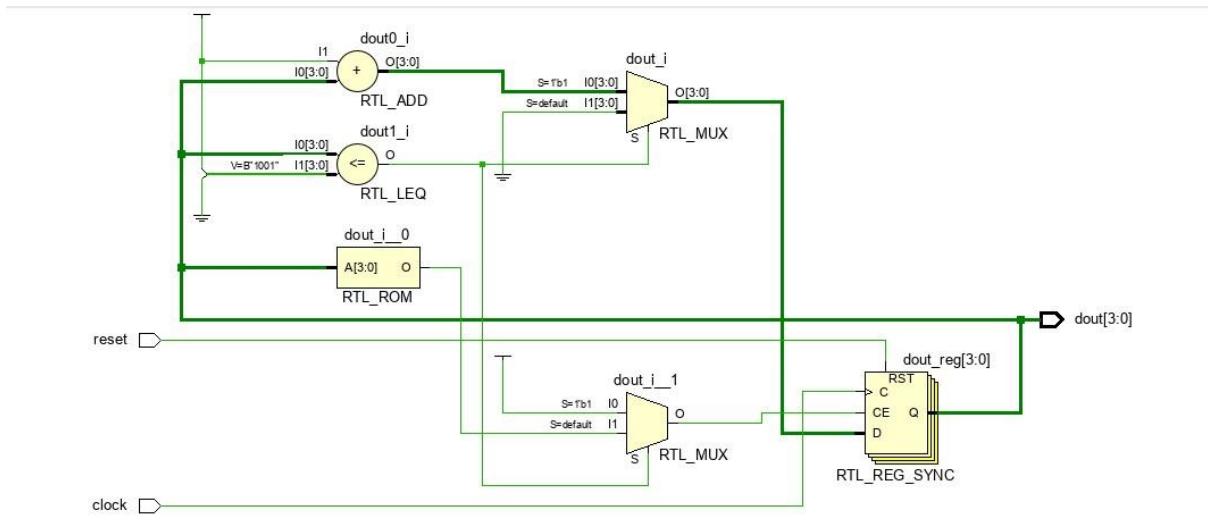
always @ (posedge (clock))
begin
    if (reset)
        dout <= 0;
    else if (dout <= 9)
        dout <= dout + 1;
    else if (dout == 9)
        dout <= 0;
end
endmodule
```

TEST BENCH:-

```
module bcdcounter_testbench();
reg clock, reset;
wire [3:0] dout;

bcd_counter dut(clock, reset, dout);
initial begin
clock=0;
forever #5 clock=~clock;
end
initial begin
reset=1;
#20;
reset=0;
end
endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |BUFG | 1|
|2 |LUT3 | 1|
|3 |LUT4 | 4|
|4 |FDRE | 4|
|5 |IBUF | 2|
|6 |OBUF | 4|
+-----+-----+
Report Instance Areas:
+-----+-----+
| |Instance |Module |Cells |
+-----+-----+
|1 |top | | 16|
+-----+-----+
-----
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:22 . Memory (MB): peak = 1019.316 ; gain = 0.000
-----
```

POWER REPORT:-

Summary

Power analysis from implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	2.855 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	30.4°C
Thermal Margin:	54.6°C (28.8 W)
Effective gJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q2. 3-1 MUX

VERILOG CODE:-

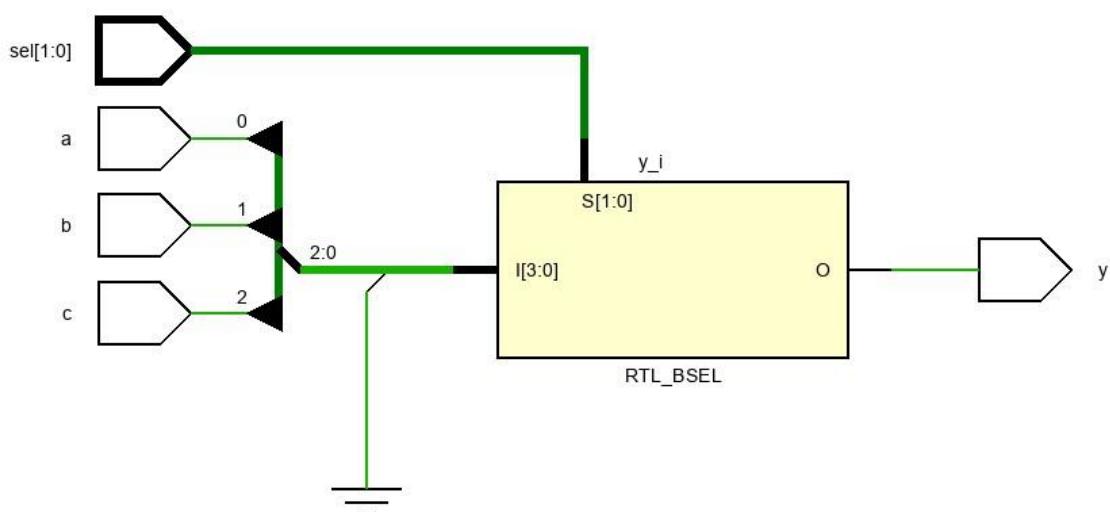
```
module mux_2_1(
    input sel,
    input i0, i1,
    output y);
    assign y = sel ? i1 : i0;
endmodule

module mux_3_1(
    input sel0, sel1,
    input i0,i1,i2,i3,
    output reg y);
    wire y0, y1;
    mux_2_1 m1(sel1, i0, i1, y0);
    mux_2_1 m2(sel0, y0, i2, y);
endmodule
```

TESTBENCH:-

```
module tb;
    reg sel0, sel1;
    reg i0,i1,i2,i3;
    wire y;
    mux_3_1 mux(sel0, sel1, i0, i1, i2, i3, y);
    initial begin
        $monitor("sel0=%b, sel1=%b -> i3 = %0b, i2 = %0b ,i1 = %0b, i0 = %0b -> y = %0b", sel0,sel1,i3,i2,i1,i0, y);
        {i3,i2,i1,i0} = 4'h5;
        repeat(8) begin
            {sel0, sel1} = $random;
            #5;
        end
    end
endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
++-----+-----+
| !BlackBox name |Instances |
++-----+-----+
++-----+-----+

Report Cell Usage:
++-----+-----+
|   |Cell |Count |
++-----+-----+
|1  |LUT5 |    1|
|2  |IBUF |    5|
|3  |OBUF |    1|
++-----+-----+

Report Instance Areas:
++-----+-----+-----+
|   |Instance |Module |Cells |
++-----+-----+-----+
|1  |top      |       |    7|
++-----+-----+-----+

```

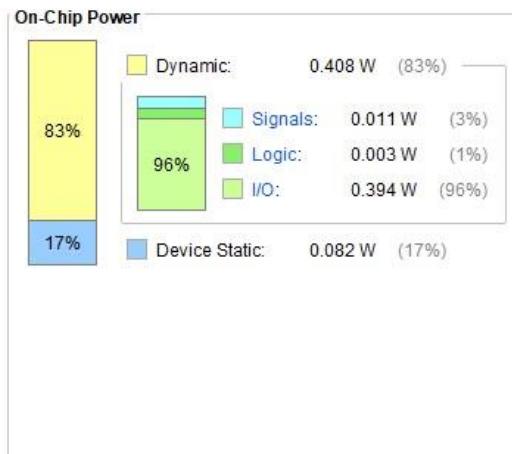
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:25 . Memory (MB): peak = 1014.996 ; gain = 0.000

POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.49 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	25.9°C
Thermal Margin:	59.1°C (31.2 W)
Effective SJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



Q3. BCD TO SEVEN SEGMENT DISPLAY

VERILOG CODE:-

```
1 //////////////////////////////////////////////////////////////////
2 module segment7(
3     bcd,
4     seg
5 );
6
7     //Declare inputs,outputs and internal variables.
8     input [3:0] bcd;
9     output [6:0] seg;
10    reg [6:0] seg;
11
12    //always block for converting bcd digit into 7 segment format
13    always @ (bcd)
14    begin
15        case (bcd) //case statement
16            0 : seg = 7'b0000001;
17            1 : seg = 7'b1001111;
18            2 : seg = 7'b0010010;
19            3 : seg = 7'b0000110;
20            4 : seg = 7'b1001100;
21            5 : seg = 7'b0100100;
22            6 : seg = 7'b0100000;
23            7 : seg = 7'b0001111;
24            8 : seg = 7'b0000000;
25            9 : seg = 7'b0000100;
26        //switch off 7 segment character when the bcd digit is not a decimal number.
27        default : seg = 7'b1111111;
28    endcase
29 end
30
31 endmodule
```

TESTBENCH:-

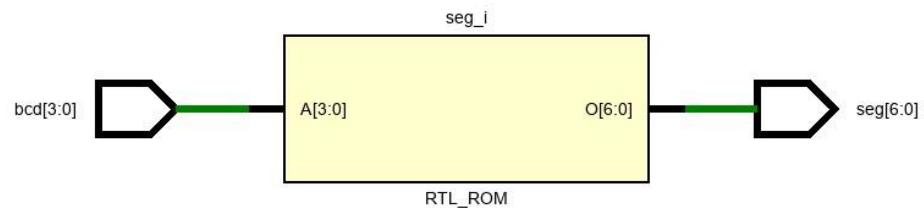
```
module tb_segment7;
reg [3:0] bcd;
wire [6:0] seg;
integer i;

// Instantiate the Unit Under Test (UUT)
segment7 uut (
    .bcd(bcd),
    .seg(seg)
);

//Apply inputs
initial begin
    for(i = 0;i < 16;i = i+1) //run loop for 0 to 15.
    begin
        bcd = i;
        #10; //wait for 10 ns
    end
end

endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

Start Writing Synthesis Report

Report BlackBoxes:

BlackBox name	Instances

Report Cell Usage:

Cell	Count
LUT4	7
IBUF	4
OBUF	7

Report Instance Areas:

Instance	Module	Cells
top		18

Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:17 . Memory (MB): peak = 1016.211 ; gain = 0.000

POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:

2.767 W

Design Power Budget:

Not Specified

Power Budget Margin:

N/A

Junction Temperature:

30.2°C

Thermal Margin:

54.8°C (28.9 W)

Effective SJA:

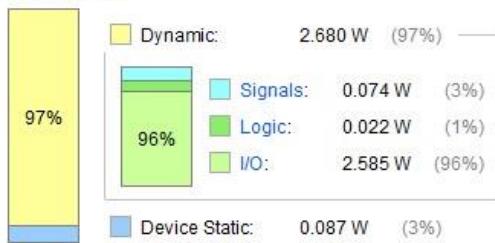
1.9°C/W

Power supplied to off-chip devices: **0 W**

Confidence level: **Low**

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power



Q4. D LATCH USING 2:1 MUX

VERILOG CODE:-

```
module DFFusingMUX(input d1, d0, sel, clk, rst, output reg q);
reg d;

always @ (*) begin
    case(sel)
        0 : d = d0;
        1 : d = d1;
    endcase
end

always @(posedge clk)
begin
    if(rst)
        q <= 0;
    else
        q <= d;
end
endmodule
```

TESTBENCH:-

```
module tb;
reg d1,d0;
reg clk;
reg rst;
wire q;

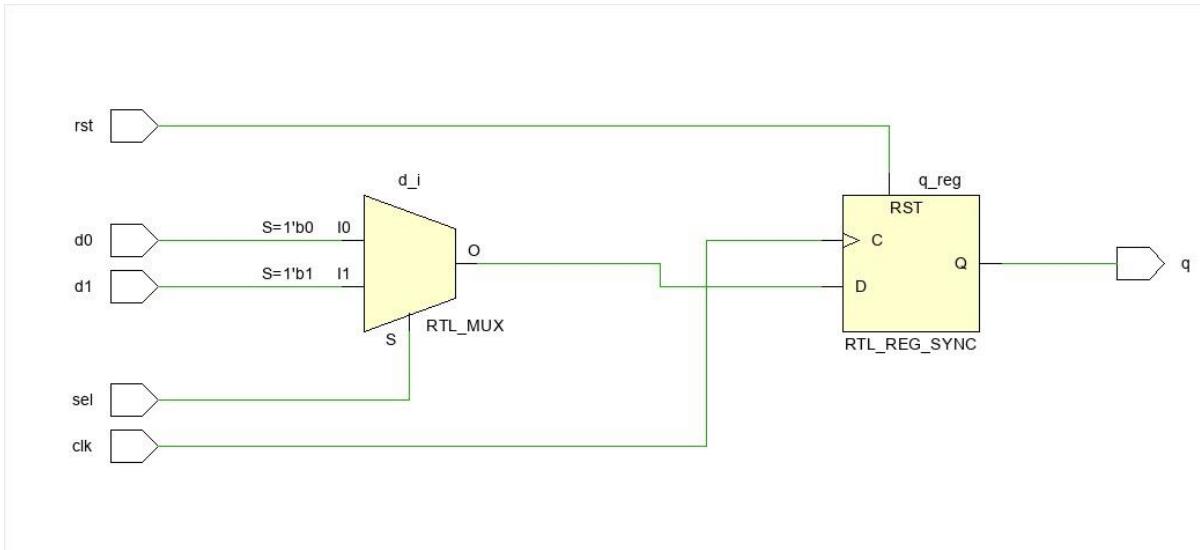
d_latch d3(q,d1,d0,clk,rst);

initial
begin
    clk = 1'b0;
    forever #20 clk = ~clk ;
end

initial
begin
    rst = 1'b1;
    #40;
    rst = 1'b0;
    #40;
    d0 = 1'b0;
    d1= 1'b0;
    #40
    d0 = 1'b1;
    d1 = 1'b0;
    #40;

    $finish ;
end
endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| |BlackBox name |Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+---+  
| |Cell |Count |  
+---+---+---+  
|1|BUFG|1|  
|2|LUT3|1|  
|3|FDRE|1|  
|4|IBUF|5|  
|5|OBUF|1|  
+---+---+---+  
  
Report Instance Areas:  
+---+---+---+---+  
| |Instance |Module |Cells |  
+---+---+---+---+  
|1|top| |9|  
+---+---+---+---+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:20 . Memory (MB): peak = 1019.727 ; gain = 0.000
```

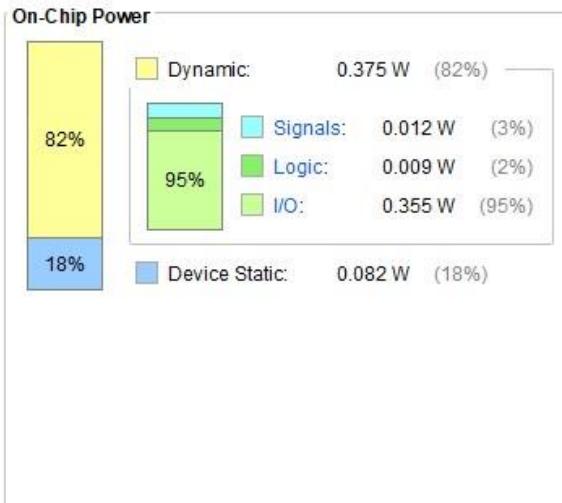
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.457 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	25.9°C
Thermal Margin:	59.1°C (31.2 W)
Effective RJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q5. 8-BIT BARREL SHIFTER

VERILOG CODE:-

```

    module barrel_shifter_8bit (in, ctrl, out);
        input [7:0] in;
        input [2:0] ctrl;
        output [7:0] out;
        wire [7:0] x,y;

        //4bit shift right
        mux2X1 ins_17 (.in0(in[7]),.in1(1'b0),.sel(ctrl[2]),.out(x[7]));
        mux2X1 ins_16 (.in0(in[6]),.in1(1'b0),.sel(ctrl[2]),.out(x[6]));
        mux2X1 ins_15 (.in0(in[5]),.in1(1'b0),.sel(ctrl[2]),.out(x[5]));
        mux2X1 ins_14 (.in0(in[4]),.in1(1'b0),.sel(ctrl[2]),.out(x[4]));
        mux2X1 ins_13 (.in0(in[3]),.in1(in[7]),.sel(ctrl[2]),.out(x[3]));
        mux2X1 ins_12 (.in0(in[2]),.in1(in[6]),.sel(ctrl[2]),.out(x[2]));
        mux2X1 ins_11 (.in0(in[1]),.in1(in[5]),.sel(ctrl[2]),.out(x[1]));
        mux2X1 ins_10 (.in0(in[0]),.in1(in[4]),.sel(ctrl[2]),.out(x[0]));

        //2 bit shift right

        mux2X1 ins_27 (.in0(x[7]),.in1(1'b0),.sel(ctrl[1]),.out(y[7]));
        mux2X1 ins_26 (.in0(x[6]),.in1(1'b0),.sel(ctrl[1]),.out(y[6]));
        mux2X1 ins_25 (.in0(x[5]),.in1(x[7]),.sel(ctrl[1]),.out(y[5]));
        mux2X1 ins_24 (.in0(x[4]),.in1(x[6]),.sel(ctrl[1]),.out(y[4]));
        mux2X1 ins_23 (.in0(x[3]),.in1(x[5]),.sel(ctrl[1]),.out(y[3]));
        mux2X1 ins_22 (.in0(x[2]),.in1(x[4]),.sel(ctrl[1]),.out(y[2]));
        mux2X1 ins_21 (.in0(x[1]),.in1(x[3]),.sel(ctrl[1]),.out(y[1]));
        mux2X1 ins_20 (.in0(x[0]),.in1(x[2]),.sel(ctrl[1]),.out(y[0]));

        //1 bit shift right
        mux2X1 ins_07 (.in0(y[7]),.in1(1'b0),.sel(ctrl[0]),.out(out[7]));
        mux2X1 ins_06 (.in0(y[6]),.in1(y[7]),.sel(ctrl[0]),.out(out[6]));
        mux2X1 ins_05 (.in0(y[5]),.in1(y[6]),.sel(ctrl[0]),.out(out[5]));
        mux2X1 ins_04 (.in0(y[4]),.in1(y[5]),.sel(ctrl[0]),.out(out[4]));
        mux2X1 ins_03 (.in0(y[3]),.in1(y[4]),.sel(ctrl[0]),.out(out[3]));
        mux2X1 ins_02 (.in0(y[2]),.in1(y[3]),.sel(ctrl[0]),.out(out[2]));

        //2 bit shift right

        mux2X1 ins_27 (.in0(x[7]),.in1(1'b0),.sel(ctrl[1]),.out(y[7]));
        mux2X1 ins_26 (.in0(x[6]),.in1(1'b0),.sel(ctrl[1]),.out(y[6]));
        mux2X1 ins_25 (.in0(x[5]),.in1(x[7]),.sel(ctrl[1]),.out(y[5]));
        mux2X1 ins_24 (.in0(x[4]),.in1(x[6]),.sel(ctrl[1]),.out(y[4]));
        mux2X1 ins_23 (.in0(x[3]),.in1(x[5]),.sel(ctrl[1]),.out(y[3]));
        mux2X1 ins_22 (.in0(x[2]),.in1(x[4]),.sel(ctrl[1]),.out(y[2]));
        mux2X1 ins_21 (.in0(x[1]),.in1(x[3]),.sel(ctrl[1]),.out(y[1]));
        mux2X1 ins_20 (.in0(x[0]),.in1(x[2]),.sel(ctrl[1]),.out(y[0]));

        //1 bit shift right
        mux2X1 ins_07 (.in0(y[7]),.in1(1'b0),.sel(ctrl[0]),.out(out[7]));
        mux2X1 ins_06 (.in0(y[6]),.in1(y[7]),.sel(ctrl[0]),.out(out[6]));
        mux2X1 ins_05 (.in0(y[5]),.in1(y[6]),.sel(ctrl[0]),.out(out[5]));
        mux2X1 ins_04 (.in0(y[4]),.in1(y[5]),.sel(ctrl[0]),.out(out[4]));
        mux2X1 ins_03 (.in0(y[3]),.in1(y[4]),.sel(ctrl[0]),.out(out[3]));
        mux2X1 ins_02 (.in0(y[2]),.in1(y[3]),.sel(ctrl[0]),.out(out[2]));
        mux2X1 ins_01 (.in0(y[1]),.in1(y[2]),.sel(ctrl[0]),.out(out[1]));
        mux2X1 ins_00 (.in0(y[0]),.in1(y[1]),.sel(ctrl[0]),.out(out[0]));

    endmodule

    //////////////////////////////
    //2X1 Mux
    //////////////////////////////

    module mux2X1( in0,in1,sel,out);
        input in0,in1;
        input sel;
        output out;
        assign out=(sel)?in1:in0;
    endmodule

```

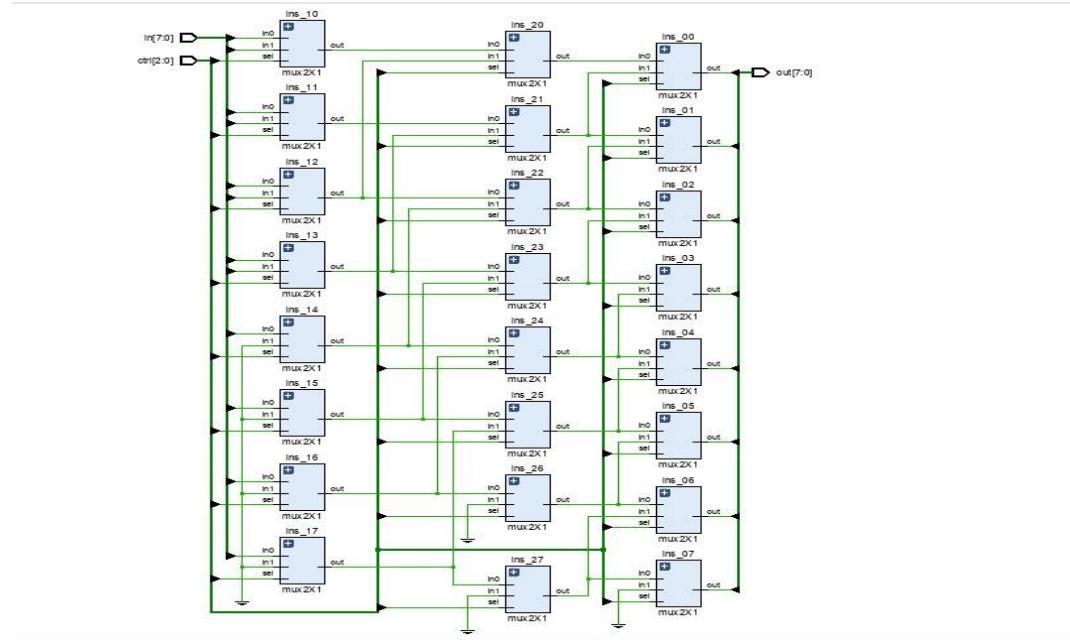
TESTBENCH:-

```
) module barrel_shifter_8bit_tb;
    reg [7:0] in;
    reg [2:0] ctrl;
    wire [7:0] out;

    barrel_shifter_8bit uut(.in(in), .ctrl(ctrl), .out(out));

) initial
) begin
    $display($time, " << Starting the Simulation >>");
    in= 8'd0;  ctrl=3'd0; //no shift
    #10 in=8'd128; ctrl= 3'd4; //shift 4 bit
    #10 in=8'd128; ctrl= 3'd2; //shift 2 bit
    #10 in=8'd128; ctrl= 3'd1; //shift by 1 bit
    #10 in=8'd255; ctrl= 3'd7; //shift by 7bit
) end
) initial begin
    $monitor("Input=%d, Control=%d, Output=%d",in,ctrl,out);
) end
) endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
++-----+-----+
| |BlackBox name |Instances |
++-----+-----+
++-----+-----+

Report Cell Usage:
++-----+-----+
| |Cell |Count |
++-----+-----+
|1 |LUT3 | 3|
|2 |LUT4 | 2|
|3 |LUT5 | 3|
|4 |LUT6 | 5|
|5 |IBUF | 11|
|6 |OBUF | 8|
++-----+-----+

Report Instance Areas:
++-----+-----+
| |Instance |Module |Cells |
++-----+-----+
|1 |top |  | 32|
++-----+-----+
-----
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16 . Memory (MB): peak = 1020.242 ; gain = 0.000

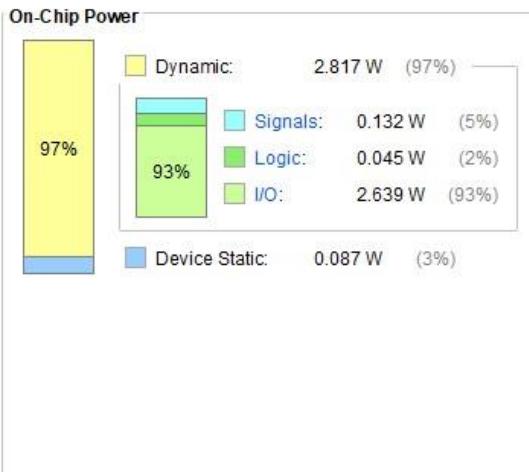
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 2.904 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 30.5°C
 Thermal Margin: 54.5°C (28.8 W)
 Effective 9JA: 1.9°C/W
 Power supplied to off-chip devices: 0 W
 Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q6. 1-BIT COMPARATOR USING 4X1 MUX

VERILOG CODE:-

```
/////////
module comp_lbit(out, a, b, c, d, s0, s1);

output out;
input a, b, c, d, s0, s1;
wire sobar, slbar, T1, T2, T3, T4;

not (sobar, s0), (slbar, s1);
and (T1, a, s0bar, slbar), (T2, b, s0bar, s1),(T3, c, s0, slbar), (T4, a, s0, s1);
or(out, T1, T2, T3, T4);

endmodule
```

TESTBENCH:-

```
) module tb;

wire out;
reg a;
reg b;
reg c;
reg d;
reg s0, s1;

m41 name(.out(out), .a(a), .b(b), .c(c), .d(d), .s0(s0), .s1(s1));
) initial
) begin

a=1'b0; b=1'b0; c=1'b0;
s0=1'b0; s1=1'b0;
#500 $finish;

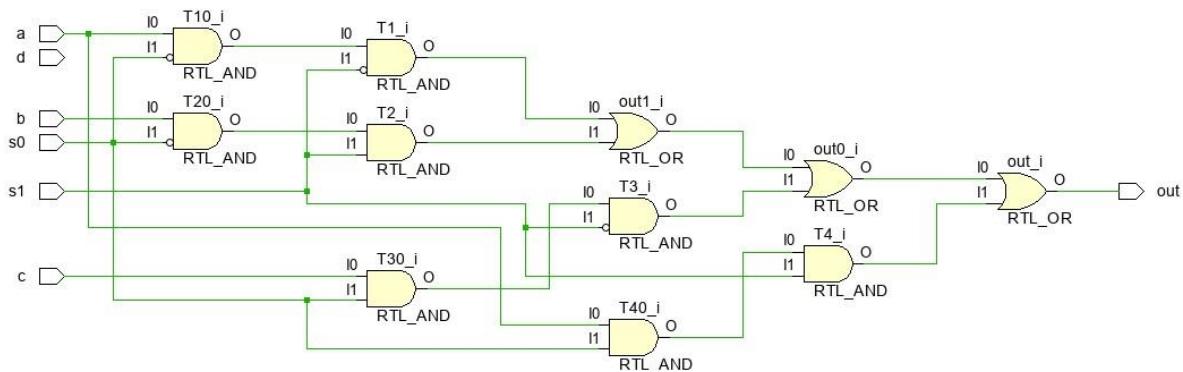
) end

always #40 a=~a;
always #20 b=~b;
always #10 c=~c;
always #80 s0=~s0;
always #160 s1=~s1;

) always@(a or b or c or s0 or s1)
) $monitor("At time = %t, Output = %d", $time, out);

) endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

Start Writing Synthesis Report
-----
Report BlackBoxes:
++-----+-----+
| BlackBox name | Instances |
++-----+-----+
++-----+-----+
Report Cell Usage:
++-----+-----+
|   Cell   | Count |
++-----+-----+
|1   |LUT5   |     1|
|2   |IBUF   |      5|
|3   |OBUF   |      1|
++-----+-----+
Report Instance Areas:
++-----+-----+-----+
|   Instance   |Module |Cells |
++-----+-----+-----+
|1   |top       |      |    7|
++-----+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:24 ; elapsed = 00:00:37 . Memory (MB): peak = 1021.613 ; gain = 0.000
-----
```

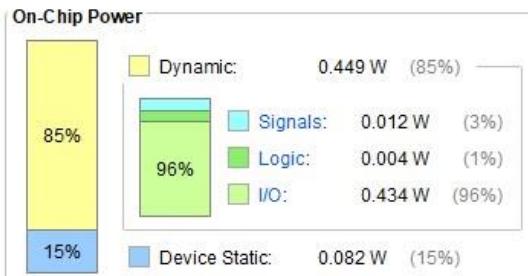
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.531 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.0°C
Thermal Margin:	59.0°C (31.1 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q7.LOGICAL, ALGEBRAIC, AND ROTATE SHIFT OPERATIONS VERILOG CODE:-

```

) module shift_rotate (a, opcode, result);
  input [7:0] a;
  input [2:0] opcode;
  output [7:0] result;
  wire [7:0] a;
  wire [2:0] opcode;
  reg [7:0] result;

  parameter sra_op = 3'b000,
  srl_op = 3'b001,
  sla_op = 3'b010,
  sll_op = 3'b011,
  ror_op = 3'b100,
  rol_op = 3'b101;

) always @ (a or opcode)
) begin
) case (opcode)
) sra_op : result = {a[7], a[7], a[6], a[5],
) a[4], a[3], a[2], a[1]};
) srl_op : result = a >> 1;
) sla_op : result = {a[6], a[5], a[4], a[3],
) a[2], a[1], a[0], 1'b0};
) sll_op : result = a << 1;
) ror_op : result = {a[0], a[7], a[6], a[5],
) a[4], a[3], a[2], a[1]};
) rol_op : result = {a[6], a[5], a[4], a[3],
) a[2], a[1], a[0], a[7]};
) default : result = 0;
) endcase
) end
) endmodule

```

TESTBENCH:-

```

| module shift_rotate_tb;

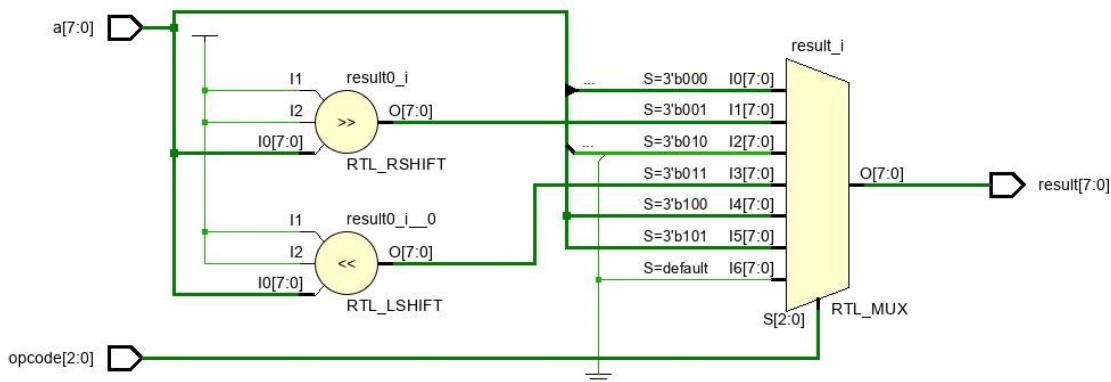
|     reg [7:0] a;
|     reg [2:0] opcode;
|     wire [7:0] result;
|     integer i;
|     shift_rotate uut (
|         .a(a),
|         .opcode(opcode),
|         .result(result)
|     );

|     initial begin
|         a=8'b10110101;
|         opcode = 000;
|
|     end
|
|     initial
|     begin
|         for(i=0;i<6;i=i+1)
|         begin
|             opcode=i;
|             #10;
|         end
|     end
|
|     initial
|     $monitor(" A=%b | Opcode=%b | Result =%b ",a,opcode,result);

| endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
+---+---+---+
| |BlackBox name |Instances |
+---+---+---+
+---+---+---+
Report Cell Usage:
+---+---+---+
| |Cell |Count |
+---+---+---+
|1 |LUT5 |    7|
|2 |LUT6 |    1|
|3 |IBUF |   11|
|4 |OBUF |    8|
+---+---+---+
Report Instance Areas:
+---+---+---+
| |Instance |Module |Cells |
+---+---+---+
|1 |top |    |  27|
+---+---+---+
-----  

Finished Writing Synthesis Report : Time (s): cpu = 00:00:23 ; elapsed = 00:00:33 . Memory (MB): peak = 1017.926 ; gain = 0.000
-----
```

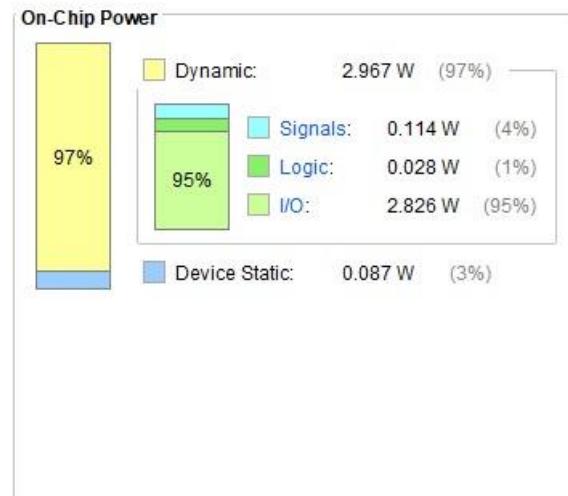
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	3.055 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	30.8°C
Thermal Margin:	54.2°C (28.6 W)
Effective θ_{JA} :	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q8. ALU

VERILOG CODE:-

```
module alu (a, b, opcode, rs1t);

input [3:0] a, b;
input [2:0] opcode;
output [7:0] rs1t;

reg [7:0] rs1t;

parameter add_op = 3'b000,
sub_op = 3'b001,
mul_op = 3'b010,
and_op = 3'b011,
or_op = 3'b100,
not_op = 3'b101,
xor_op = 3'b110,
xnor_op = 3'b111;

always @ (a or b or opcode)
begin
case (opcode)
add_op: rs1t = a + b;
sub_op: rs1t = a - b;
mul_op: rs1t = a * b;
and_op: rs1t = a & b; //also ab
or_op: rs1t = a | b;
not_op: rs1t = ~a; //also ~b
xor_op: rs1t = a ^ b;
xnor_op: rs1t = ~(a ^ b);
endcase
end
endmodule
```

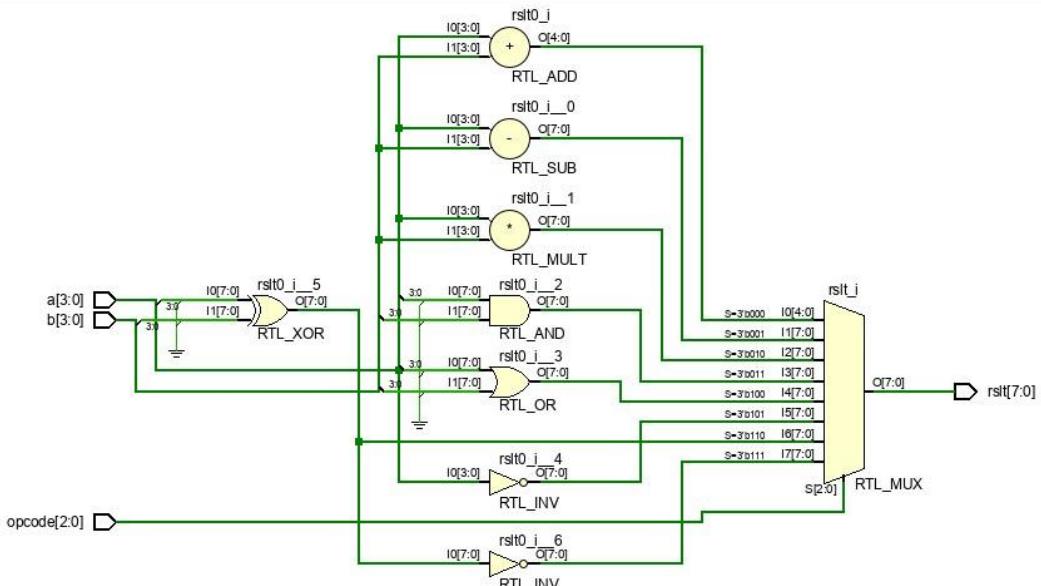
TEST BENCH:-

```

`timescale 1ns / 1ps
module alu_tb;
reg [3:0] a;
reg [3:0] b;
reg [2:0] opcode;
wire [7:0] rslt;
alu uut (.a(a), .b(b), .opcode(opcode), .rslt(rslt));
initial
begin
#0 a = 4'b0001; b = 4'b0010; opcode = 3'b000;
#10 a = 4'b0110; b = 4'b0110; opcode = 3'b000;
#10 a = 4'b1100; b = 4'b0011; opcode = 3'b001;
#10 a = 4'b1101; b = 4'b1010; opcode = 3'b001;
#10 a = 4'b1100; b = 4'b0111; opcode = 3'b010;
#10 a = 4'b1111; b = 4'b0011; opcode = 3'b010;
#10 a = 4'b1100; b = 4'b0111; opcode = 3'b011;
#10 a = 4'b1101; b = 4'b1011; opcode = 3'b011;
#10 a = 4'b0101; b = 4'b1011; opcode = 3'b100;
#10 a = 4'b1001; b = 4'b1010; opcode = 3'b100;
#10 a = 4'b1001; opcode = 3'b101;
#10 a = 4'b0011; opcode = 3'b101;
#10 a = 4'b0111; b = 4'b1011; opcode = 3'b110;
#10 a = 4'b1010; b = 4'b0101; opcode = 3'b110;
#10 a = 4'b0110; b = 4'b0110; opcode = 3'b111;
#10 a = 4'b0011; b = 4'b1110; opcode = 3'b111;
end
initial
begin
$monitor(" A=%b | B=%b | Opcode = %b | Result=%b",a,b,opcode,rslt);
#300 $finish;
end
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
++-----+-----+
| |BlackBox name |Instances |
++-----+-----+
++-----+-----+

Report Cell Usage:
++-----+-----+
| |Cell |Count |
++-----+-----+
|1 |CARRY4 | 2|
|2 |LUT2 | 6|
|3 |LUT4 | 6|
|4 |LUT5 | 7|
|5 |LUT6 | 19|
|6 |MUXF7 | 3|
|7 |IBUF | 11|
|8 |OBUF | 8|
++-----+-----+

Report Instance Areas:
++-----+-----+
| |Instance |Module |Cells |
++-----+-----+
|1 |top | | 62|
++-----+-----+
-----
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:21 . Memory (MB): peak = 1016.625 ; gain = 0.000

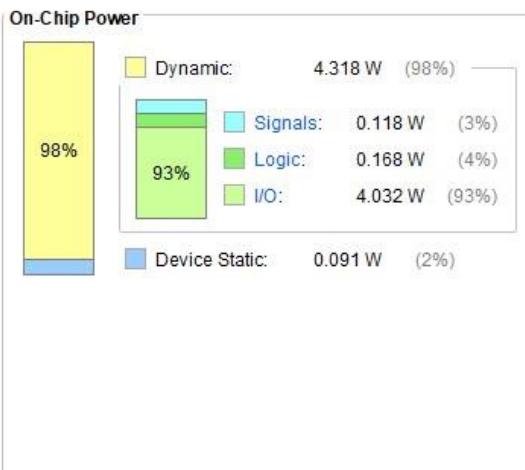
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	4.409 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	33.3°C
Thermal Margin:	51.7°C (27.3 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q9. 4-BIT ASYNCHRONOUS DOWN COUNTER

VERILOG CODE:-

```

module dff(q,qbar,clk,rst,d);
    output reg q;
    output qbar;
    input clk, rst;
    input d;

    assign qbar = ~q;

    always @ (posedge clk, posedge rst)
    begin
        if (rst)
            q <= 0;
        else
            q <= d;
    end
endmodule

module async_counter(count,countbar,clk,rst);
    input clk, rst;
    output [3:0] count, countbar;
    dffdff1(count[0],countbar[0],clk      ,rst,countbar[0]);
    dffdff2(count[1],countbar[1],count[0],rst,countbar[1]);
    dffdff3(count[2],countbar[2],count[1],rst,countbar[2]);
    dffdff4(count[3],countbar[3],count[2],rst,countbar[3]);

endmodule

```

TESTBENCH:-

```

`module async_counter_tb;

// Inputs
reg clk;
reg rst;

// Outputs
wire [3:0] count;
wire [3:0] countbar;

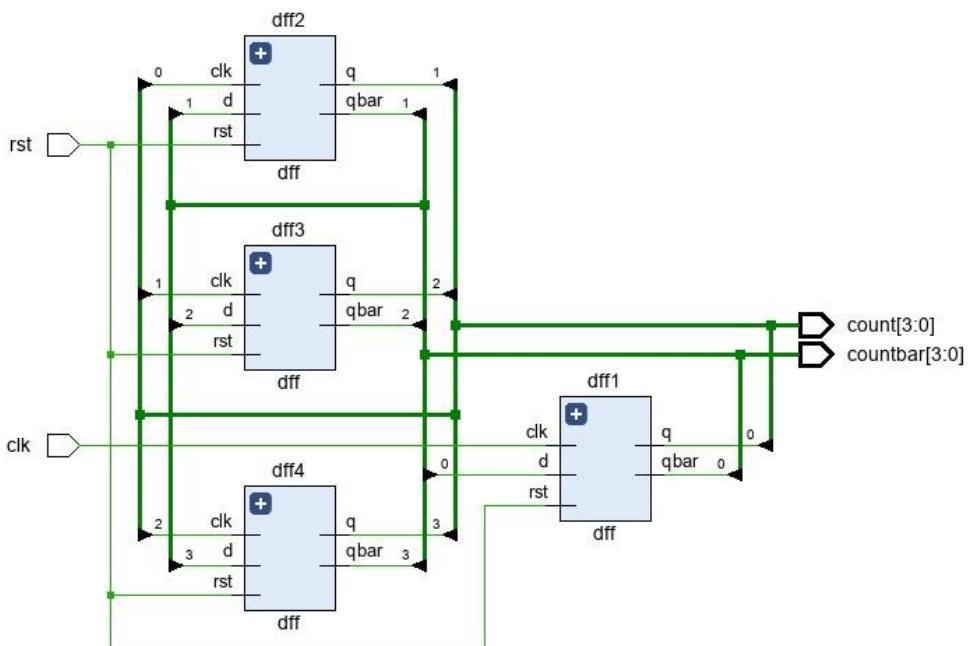
// Instantiate the Unit Under Test (UUT)
async_counter uut (
    .count(count),
    .countbar(countbar),
    .clk(clk),
    .rst(rst)
);

initial
begin
    clk = 0;
    rst = 1;
    #23; // Just give enough time to reset the design
    rst = 0;
    #200;
    $finish;
end
always #5 clk = ~clk;

endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

Start Writing Synthesis Report
-----
Report BlackBoxes:
++-----+
| |BlackBox name |Instances |
++-----+
+-----+
Report Cell Usage:
++-----+
| |Cell |Count |
+-----+
|1 |BUFG | 1|
|2 |LUT1 | 4|
|3 |FDCE | 4|
|4 |IBUF | 2|
|5 |OBUF | 8|
+-----+
Report Instance Areas:
++-----+
| |Instance |Module |Cells |
+-----+
|1 |top | | 19|
|2 |dff1 |dff | 2|
|3 |dff2 |dff_0 | 2|
|4 |dff3 |dff_1 | 2|
|5 |dff4 |dff_2 | 2|
+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:27 ; elapsed = 00:00:37 . Memory (MB): peak = 1017.906 ; gain = 0.000
-----
```

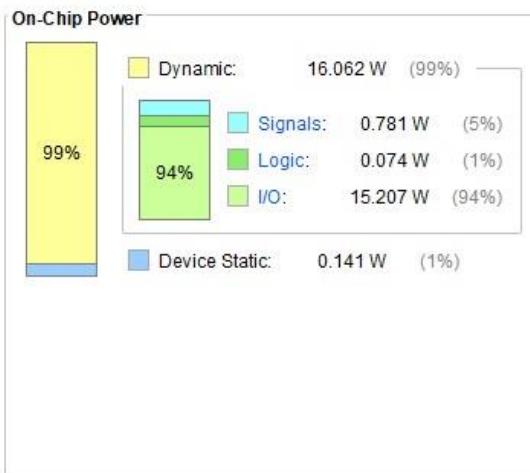
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	16.203 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	55.5°C
Thermal Margin:	29.5°C (15.5 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q10. MOD-N UPDOWN COUNTER

VERILOG CODE:-

```
timescale 1ns / 1ps
module modN_counter
# (parameter N = 10,
 parameter WIDTH = 4)

( input    clk,
  input    reset,
  input updown,
  output  reg[WIDTH-1:0] count);

always @ (posedge clk)
begin
  if (reset==1)
    count <= 0;

  else
    if(updown==1)      //Up Mode is selected
      if (count == N-1)
        count <= 0;
      else
        count<=count+1; //increment counter

    else                //Down Mode is selected
      if(count==0)
        count<=N-1;
      else
        count<=count-1; //Decrement the counter

  end
endmodule
```

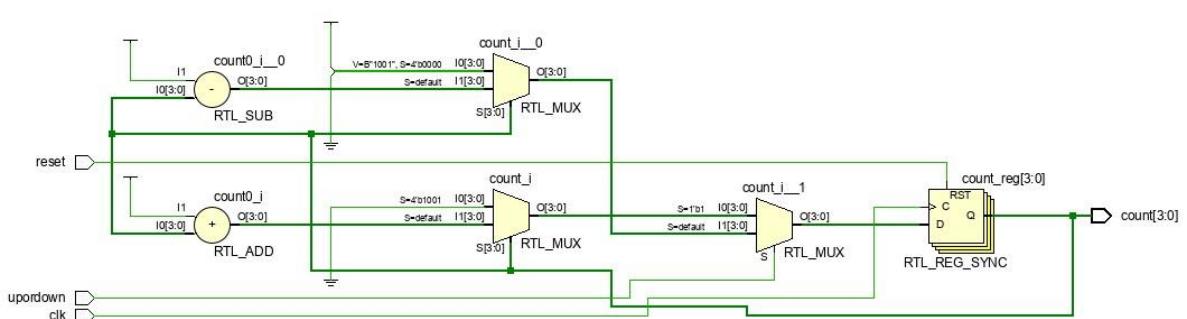
TESTBENCH:-

```

`timescale 1ns / 1ps
`module modN_updown_tb;
    reg clk;
    reg reset;
    reg upordown;
    wire [3:0] count;
    modN_counter uut (
        .clk(clk),
        .reset(reset),
        .upordown(upordown),
        .count(count)
    );
    initial begin
        clk = 0;
        reset = 1;
        #50 reset = 0; upordown = 0;
        #200;
        upordown = 1;
        #200;
        reset = 1;
        upordown = 0;
        #100;
        reset = 0;
    end
    always #10 clk=~clk;
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+

Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |BUFG | 1|
|2 |LUT1 | 1|
|3 |LUT5 | 3|
|4 |FDRE | 4|
|5 |IBUF | 3|
|6 |OBUF | 4|
+-----+-----+

Report Instance Areas:
+-----+-----+
| |Instance |Module |Cells |
+-----+-----+
|1 |top | 16|
+-----+-----+
-----
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:22 . Memory (MB): peak = 1015.855 ; gain = 0.000

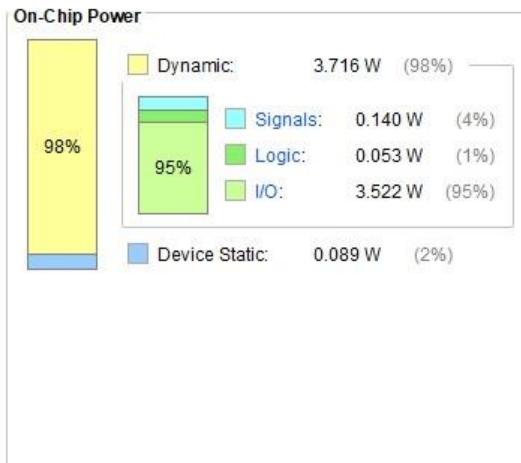
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	3.805 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	32.2°C
Thermal Margin:	52.8°C (27.9 W)
Effective SJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q11. UNIVERSAL BINARY COUNTER

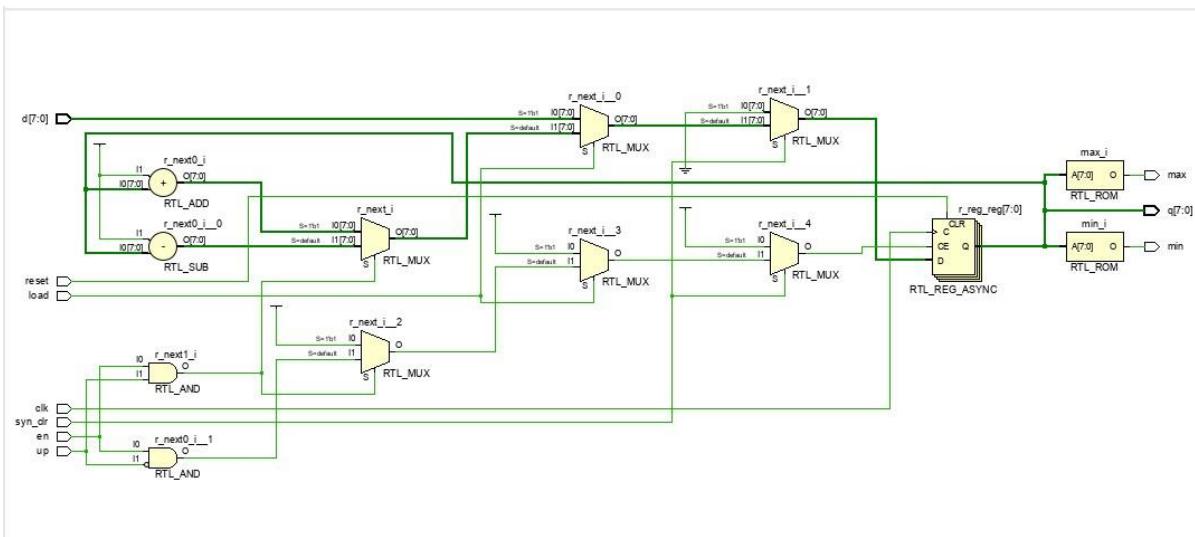
VERILOG CODE:-

```
`timescale 1ns / 1ps
module univ_bin_counter
#(parameter N=8)
(
  input wire clk, reset,
  input wire syn_clr , load, en, up,
  input wire [N-1:0] d,
  output wire max, min,
  output wire [N-1:0] q
);
  reg [N-1:0] r_reg, r_next;
  always @(posedge clk, posedge reset)
  if (reset)
    r_reg <= 0; //
  else
    r_reg <= r_next;
  always @(*)
  if (syn_clr)
    r_next = 0;
  else if (load)
    r_next = d;
  else if (en & up)
    r_next = r_reg + 1;
  else if (en & ~up)
    r_next = r_reg - 1;
  else
    r_next = r_reg;
  assign q = r_reg;
  assign max = (r_reg==2**N-1) ? 1'b1 : 1'b0;
  assign min = (r_reg==0) ? 1'b1 : 1'b0;
endmodule
```

TESTBENCH:-

```
`timescale 1ns / 1ps
module univ_bin_counter_tb;
  reg clk;
  reg reset;
  reg syn_clr;
  reg load;
  reg en;
  reg up;
  reg [7:0] d;
  wire max;
  wire min;
  wire [7:0] q;
  univ_bin_counter uut (.clk(clk), .reset(reset), .syn_clr(syn_clr), .load(load), .en(en), .up(up), .d(d), .max(max), .min(min), .q(q));
  initial begin
    clk = 0;
    reset = 0;
    syn_clr = 0;
    load = 0;
    en = 0;
    up = 0;
    d = 0;
    #10 reset =1; syn_clr=1; load=1; en=1;up=1; d=1;
    #10 reset =0; syn_clr=0; load=1; en=1;up=1; d=1;
    #10 reset =0; syn_clr=0; load=0; en=1;up=1; d=1;
    #400 reset =0;syn_clr=0 ; load=0; en=1;up=0; d=1;
  end
  always #5 clk=~clk;
  initial
  begin
    $monitor(" Reset=%b | Sync_clr=%b | Load=%b| En=%b | Up=%b| D=%b | Q=%b",reset,syn_clr,load,en,up,d,q);
    #1000 $finish;
  end
endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```
-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
++-----+-----+
| |BlackBox name |Instances |
++-----+-----+
++-----+-----+
++-----+-----+
Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |BUFG | 1|
|2 |CARRY4 | 2|
|3 |LUT1 | 1|
|4 |LUT2 | 6|
|5 |LUT3 | 2|
|6 |LUT4 | 10|
|7 |LUT5 | 2|
|8 |FDCE | 8|
|9 |IBUF | 14|
|10 |OBUF | 10|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
| |Instance |Module |Cells |
+-----+-----+-----+
|1 |top | | 56|
+-----+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:26 ; elapsed = 00:00:34 . Memory (MB): peak = 1019.758 ; gain = 0.000
-----
```

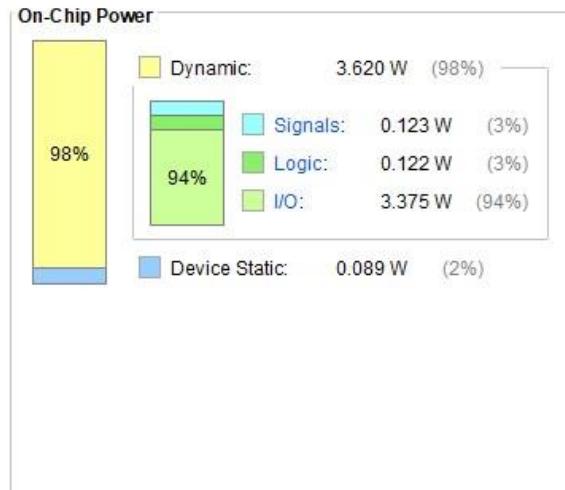
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	3.709 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	32.0°C
Thermal Margin:	53.0°C (28.0 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q12. UNIVERSAL SHIFT REGISTER

VERILOG CODE:-

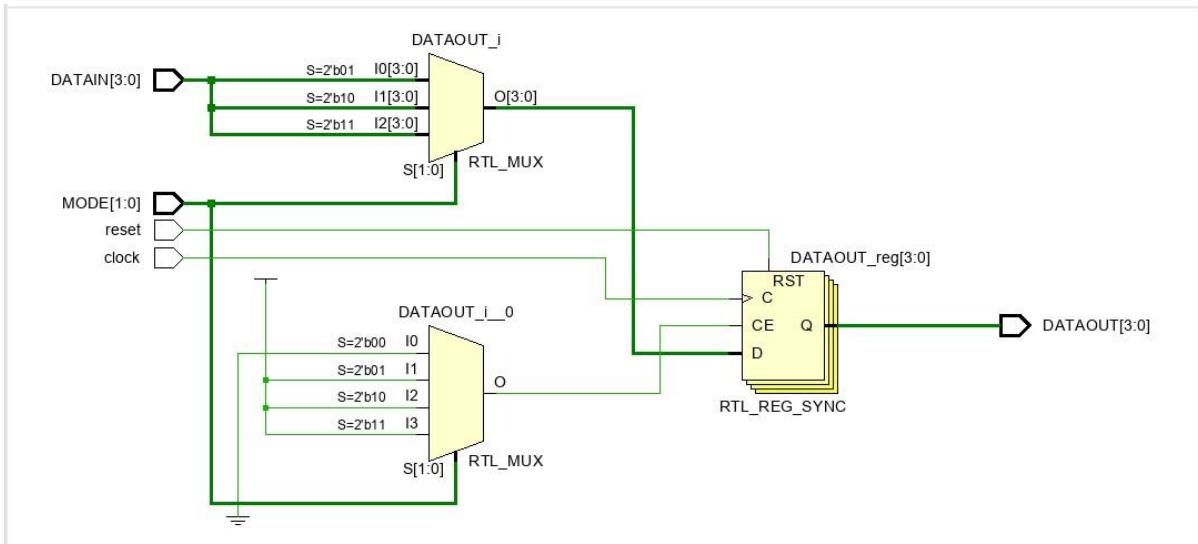
```
'timescale 1ns / 1ps
module universal_shiftreg(DATAOUT, clock, reset, MODE, DATAIN);
    output reg [3:0] DATAOUT;
    input clock, reset;
    input [1:0] MODE;
    input [3:0] DATAIN;

    always @(posedge clock)
    begin
        if(reset)
            DATAOUT <= 0;
        else
            begin
                case(MODE)
                    2'b00 : DATAOUT <= DATAOUT;      // locked mode, do nothing
                    2'b01 : DATAOUT <= {DATAIN[0], DATAIN[3:1]};//DATAOUT >> 1;
                    2'b10 : DATAOUT <= {DATAIN[2:0], DATAIN[3]};//DATAOUT << 1;
                    2'b11 : DATAOUT <= DATAIN;        // parallel in parallel out
                endcase
            end
    end
endmodule
```

TESTBENCH:-

```
'timescale 1ns / 1ps
module univ_bin_counter_tb;
    reg clk;
    reg reset;
    reg syn_clr;
    reg load;
    reg en;
    reg up;
    reg [7:0] d;
    wire max;
    wire min;
    wire [7:0] q;
    univ_bin_counter uut (.clk(clk), .reset(reset), .syn_clr(syn_clr), .load(load), .en(en), .up(up), .d(d), .max(max), .min(min), .q(q));
initial begin
    clk = 0;
    reset = 0;
    syn_clr = 0;
    load = 0;
    en = 0;
    up = 0;
    d = 0;
    #10 reset =1; syn_clr=1; load=1; en=1;up=1; d=1;
    #10 reset =0; syn_clr=0; load=1; en=1;up=1; d=1;
    #10 reset =0; syn_clr=0; load=0; en=1;up=1; d=1;
    #400 reset =0;syn_clr=0 ; load=0; en=1;up=0; d=1;
end
always #5 clk=~clk;
initial
begin
    $monitor(" Reset=%b | Sync_clr=%b | Load=%b| En=%b | Up=%b| D=%b | Q=%b",reset,syn_clr,load,en,up,d,q);
    #1000 $finish;
end
endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |BUFG | 1|
|2 |LUT2 | 1|
|3 |LUT5 | 4|
|4 |FDRE | 4|
|5 |IBUF | 8|
|6 |OBUF | 4|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
| |Instance |Module |Cells |
+-----+-----+-----+
|1 |top | | 22|
+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:25 ; elapsed = 00:00:35 . Memory (MB): peak = 1017.617 ; gain = 0.000
-----
```

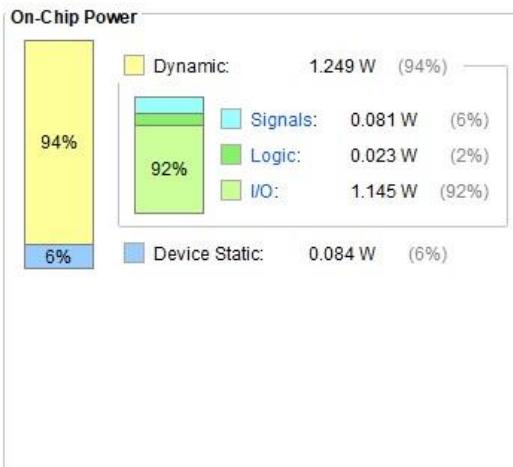
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	1.333 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	27.5°C
Thermal Margin:	57.5°C (30.3 W)
Effective θ_{JA} :	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q13. CN(CHANGE-NO CHANGE FLIPFLOP) USING 2:1 MUX
VERILOG CODE:-

```

module mux2X1(a,b,s,y);
input a,b,s;
output reg y;
always @(a or b or s)
begin
case(s)
0: y=a;
1:y=b;
default: y=1'b0;
endcase
end
endmodule

module d_ff(d,clk,reset,q);
input d,clk,reset;
output reg q;
always @(posedge clk)
begin
if(reset)
q=0;
else
q=d;
end
endmodule

module cn_flipflop(c,n,clk,q,qbar);
input c,n,clk;
output q,qbar;
wire cn,n_bar,d_wire;
mux2X1 mux1(1'b0,c,n,cn);
mux2X1 mux2(1'b1,1'b0,n,n_bar);
mux2X1 mux3(cn,n_bar,q,d_wire);
d_ff df1(.d(d_wire),.clk(clk),.reset(),.q(q));
assign qbar=~q;
endmodule

```

TESTBENCH:-

```

`timescale 1ns / 1ps
) module cn_flipflop_tb;

    reg c;
    reg n;
    reg clk;
    wire q,qbar;

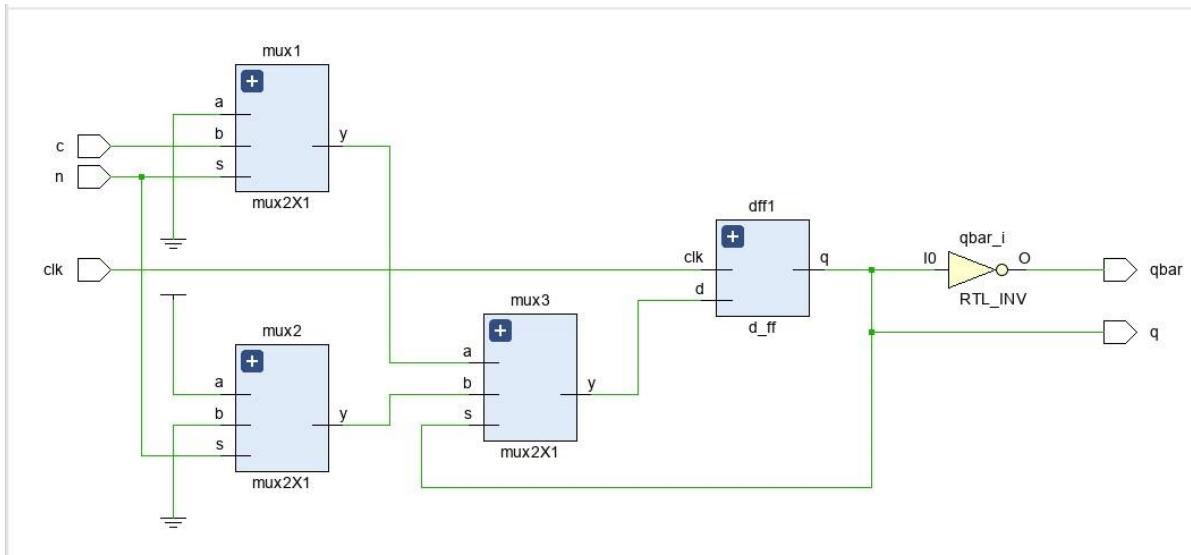
    cn_flipflop uut (.c(c),.n(n),.clk(clk),.q(q),.qbar(qbar));

) initial begin
    c = 0;
    n = 0;
    clk = 0;
    #10 c=0;n=1;
    #10 c=1;n=0;
    #10 c=1;n=1;
) end
always #5 clk=~clk;
initial
begin $monitor("C=%b | N=%b | Q=%b | Qbar=%b",c,n,q,qbar);
#100 $finish;
) end

) endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
++-----+-----+
| |BlackBox name |Instances |
++-----+-----+
++-----+-----+
++-----+-----+
Report Cell Usage:
++-----+-----+
| |Cell |Count |
++-----+-----+
|1 |BUFG | 1|
|2 |LUT1 | 1|
|3 |LUT3 | 1|
|4 |FDRE | 1|
|5 |IBUF | 3|
|6 |OBUF | 2|
++-----+-----+

Report Instance Areas:
++-----+-----+
| |Instance |Module |Cells |
++-----+-----+
|1 |top |  | 9|
|2 |dff1 |d_ff | 3|
++-----+-----+
-----
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:24 ; elapsed = 00:00:34 . Memory (MB): peak = 1014.594 ; gain = 0.000

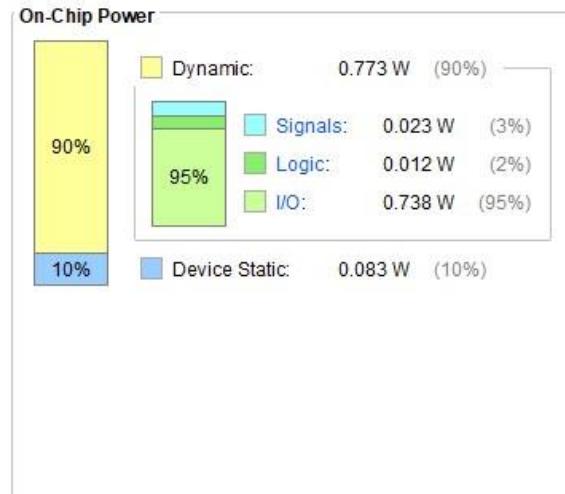
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.856 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.6°C
Thermal Margin:	58.4°C (30.8 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q14.FREQUENCY DIVIDER BY ODD NUMBERS

VERILOG CODE:-

```
`timescale 1ns / 1ps
`module clk_div_odd
#(parameter N=5)
( input  clk_in,output  clk_out);

reg [3:0] count = 4'b0;
reg A1 = 0;
reg B1 = 0;
reg Tff_A = 0;
reg Tff_B = 0;
wire clock_out;
wire wTff_A;
wire wTff_B;
assign wTff_A = Tff_A;
assign wTff_B = Tff_B;

assign clk_out = wTff_B ^ wTff_A;
`always@(posedge clk_in)
`begin
`if(count == N-1)
`begin
count <= 4'b0000;
`end
`else
`begin
count <= count + 1;
`end
`end
`always@(posedge clk_in)
`begin
`if(count == 4'b0000)
A1 <= 1;
`else
`A1 <= 0;
`end
```

```

|     A1 <= 0;
| end
| always@(posedge clk_in)
| begin
|   if(count == (N+1)/2)
|     B1 <= 1;
|   else
|     B1 <= 0;
| end
| always@(negedge A1)
| begin
|   Tff_A <= ~Tff_A;
| end

| always@(negedge clk_in)
| begin
|   if(B1)
|     begin
|       Tff_B <= ~Tff_B;
|     end
|   end
| endmodule

```

TESTBENCH:-

```

`timescale 1ns / 1ps
) module clk_div_odd_tb;
  reg clk_in;
  wire clk_out;
  clk_div_odd uut (
    .clk_in(clk_in),
    .clk_out(clk_out)
  );

) initial begin
  clk_in=1;
) end

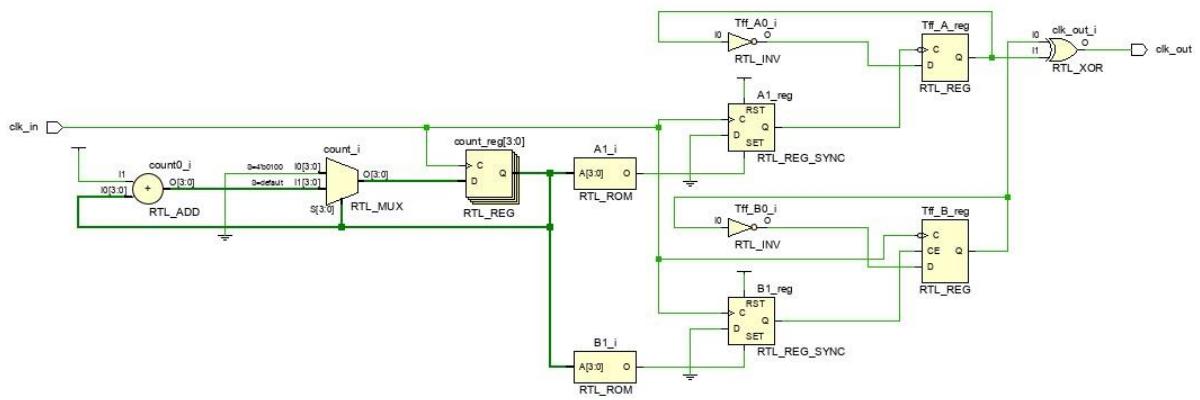
always #10 clk_in= ~clk_in;

) initial
) #200 $finish;

) endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```
-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |BUFQ | 1|
|2 |LUT1 | 2|
|3 |LUT2 | 3|
|4 |LUT3 | 1|
|5 |LUT4 | 4|
|6 |FDRE | 8|
|7 |IBUF | 1|
|8 |OBUF | 1|
+-----+-----+
Report Instance Areas:
+-----+-----+
| |Instance |Module |Cells |
+-----+-----+
|1 |top | | 21|
+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:25 ; elapsed = 00:00:34 . Memory (MB): peak = 1015.637 ; gain = 0.000
-----
```

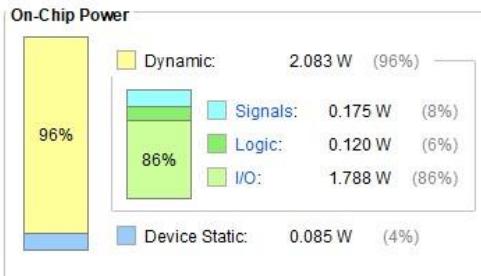
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 2.168 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 29.1°C
Thermal Margin: 55.9°C (29.5 W)
Effective θJA: 1.9°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q15. GREATEST COMMON DIVISOR USING BEHAVIOURAL MODELLING

VERILOG CODE:-

```
'timescale 1ns / 1ps
`module gcd_beh #( parameter W = 4 )
(
  input [W-1:0] A, B,
  input clk,rst,
  output reg [W-1:0] GCD
);
reg [W-1:0] Ain, Bin;
`always @(posedge clk or negedge rst)
`begin
  Ain = A; Bin = B;
`while( Ain != Bin)
`begin
`if ( Ain < Bin )
  Bin = Bin-Ain;
`else
  Ain = Ain - Bin;
`end
  GCD = Ain;
`end
`endmodule
```

TESTBENCH:-

```
`timescale 1ns / 1ps
`module gcd_beh_tb;
parameter W=7;
reg [W-1:0] A;
reg [W-1:0] B;
wire [W-1:0] GCD;
gcd_beh uut (.A(A),.B(B),.GCD(GCD));
initial begin
    A=90;B=86;
    #10 A=48; B=12;
    #10 A=65;B=4;
    #10 A=48;B=7;
    #10 A=8;B=2;
    #10 A=125;B=6;
    #10 A=85;B=76;
    #10 A=54;B=44;
    #10 A=95;B=32;
    #10 A=109;B=91;
    #10 A=75;B=34;
end
initial
begin
    $monitor("A= %d | B=%d | GCD=%d", A,B,GCD);
    #200 $finish;
end
endmodule
```

Q16.SINGLE PORT RAM

VERILOG CODE:-

```
module single_port_ram
#(parameter addr_width = 6,
parameter data_width = 8,
parameter depth = 64)
(
    input [data_width-1:0] data,
    input [addr_width-1:0] addr,
    input we,clk,
    output [data_width-1:0] q
);

reg [data_width-1:0] ram [depth-1:0];
reg [addr_width-1:0] addr_reg;

always @(posedge clk)
begin
if(we)
    ram[addr] <=data;
else
    addr_reg <=addr;
end
assign q= ram[addr_reg];
endmodule
```

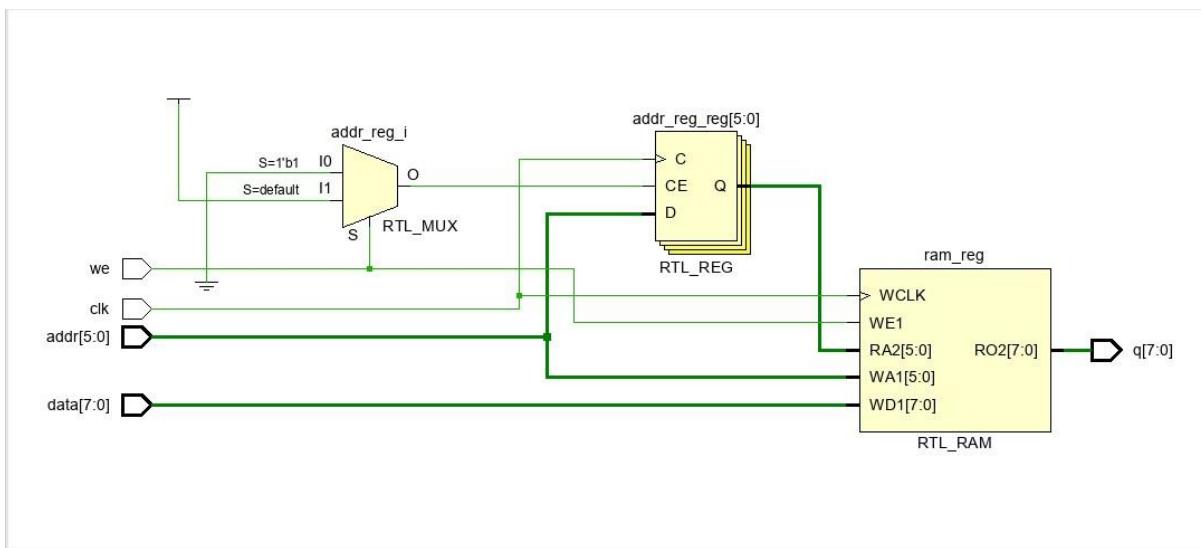
TESTBENCH:-

```

`timescale 1ns / 1ps
module single_port_ram_tb;
parameter addr_width = 6;
parameter data_width = 8;
parameter depth = 64;
reg [data_width-1:0] data;
reg [addr_width:0] addr;
reg we;
reg clk;
wire [data_width-1:0] q;
single_port_ram uut (.data(data),.addr(addr), .we(we),.clk(clk),.q(q));
initial begin
    clk=0;
    forever #5 clk=~clk;
end
initial begin
    data=8'h01;
    addr=5'd0;
    we=1'b1;
#10
    data=8'h02;
    addr=5'd1;
#10;
    data=8'h03;
    addr=5'd2;
#10;
    addr=5'd0;
    we=1'b0;
#10;
    addr=5'd1;
#10;
    addr=5'd2;
#10;
end
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```
-----  
Start Writing Synthesis Report  
-----  
  
Report BlackBoxes:  
+---+---+  
| |BlackBox name |Instances |  
+---+---+  
+---+---+  
  
Report Cell Usage:  
+---+---+  
| |Cell |Count |  
+---+---+  
|1 |BUFGE | 1|  
|2 |LUT1 | 1|  
|3 |RAM64M | 2|  
|4 |RAM64X1D | 2|  
|5 |FDRE | 6|  
|6 |IBUF | 16|  
|7 |OBUF | 8|  
+---+---+  
  
Report Instance Areas:  
+---+---+  
| |Instance |Module |Cells |  
+---+---+  
|1 |top | | 36|  
+---+---+  
-----  
Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:18 . Memory (MB): peak = 1017.363 ; gain = 0.000
```

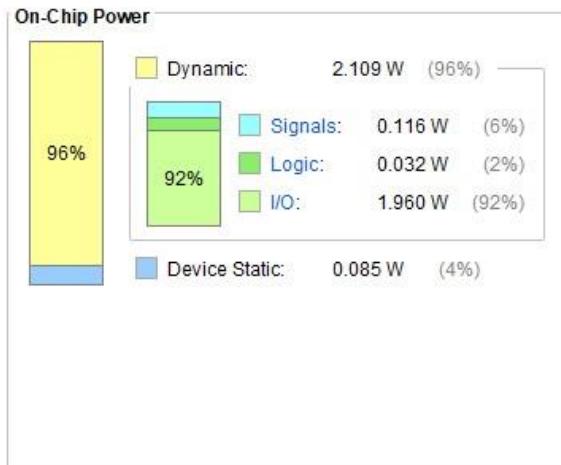
POWER REPORT:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	2.194 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	29.1°C
Thermal Margin:	55.9°C (29.5 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q17. DUAL PORT RAM

VERILOG CODE:-

```

) module dual_port_ram
)     # (parameter data_width=8,
)         parameter addr_width=4,
)             parameter depth=16
)
(   input clk,
    input wr_en,
    input [data_width-1:0] data_in,
    input [addr_width-1:0] addr_in_0,
    input [addr_width-1:0] addr_in_1,
    input port_en_0,
    input port_en_1,
    output [data_width-1:0] data_out_0,
    output [data_width-1:0] data_out_1
);

```

```

reg [data_width-1:0] ram[0:depth-1];

) always@(posedge clk)
) begin
)     if(port_en_0 == 1 && wr_en == 1)
)         ram[addr_in_0] <= data_in;
) end

assign data_out_0 = port_en_0 ? ram[addr_in_0] : 'dZ;
assign data_out_1 = port_en_1 ? ram[addr_in_1] : 'dZ;

) endmodule

```

TESTBENCH:-

```

module dual_port_ram_tb;
parameter addr_width = 4;
parameter data_width = 8;
parameter depth = 16;
integer i;
reg clk;
reg wr_en;
reg [data_width-1:0] data_in;
reg [addr_width-1:0] addr_in_0;
reg [addr_width-1:0] addr_in_1;
reg port_en_0;
reg port_en_1;
wire [data_width-1:0] data_out_0;
wire [data_width-1:0] data_out_1;
dual_port_ram uut (.clk(clk), .wr_en(wr_en), .data_in(data_in), .addr_in_0(addr_in_0), .addr_in_1(addr_in_1), .port_en_0(port_en_0), .port_en_1(port_en_1),
.data_out_0(data_out_0), .data_out_1(data_out_1));
always
#5 clk = ~clk;
initial begin
    clk = 1;
    addr_in_1 = 0;
    port_en_0 = 0;
    port_en_1 = 0;
    wr_en = 0;
    data_in = 0;
    addr_in_0 = 0;
    #20;
    port_en_0 = 1;
    wr_en = 1;
    for(i=1; i <= 16; i = i + 1) begin
        data_in = i;
        addr_in_0 = i-1;
        #10;
    end
    wr_en = 0;
}

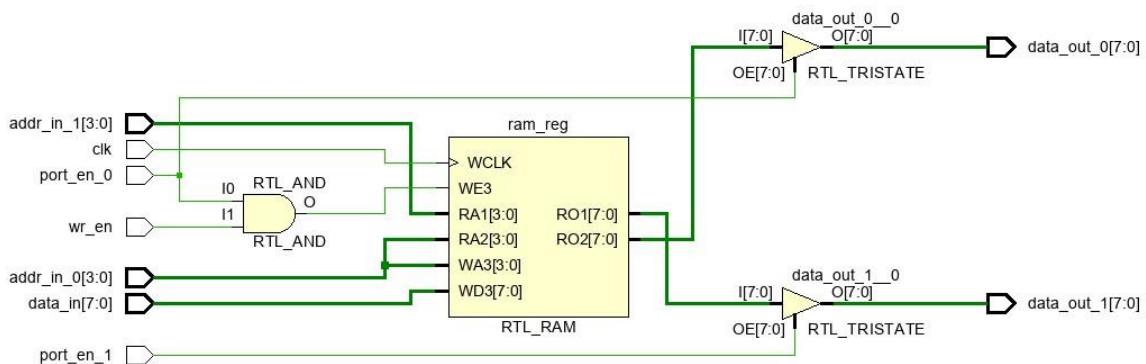
```

```

wr_en = 0;
port_en_0 = 0;
port_en_1 = 1;
for(i=1; i <= 16; i = i + 1) begin
    addr_in_1 = i-1;
    #10;
end
port_en_1 = 0;
end
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

Start Writing Synthesis Report

Report BlackBoxes:

BlackBox name	Instances

Report Cell Usage:

Cell	Count
BUF	11
LUT	21
RAM16X1D	81
IBUF	201
OBUFT	161

Report Instance Areas:

Instance	Module	Cells
top		481

Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:20 . Memory (MB): peak = 1018.852 ; gain = 0.000

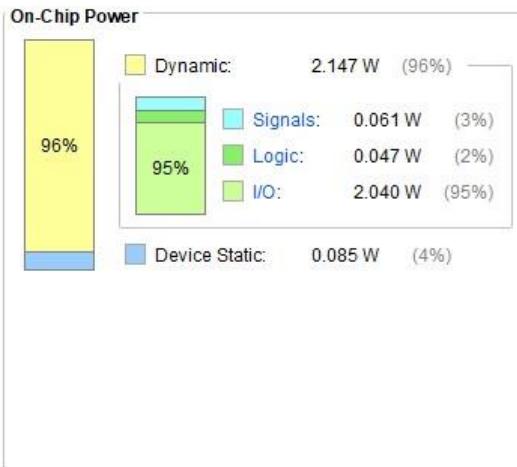
POWER REPORT:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 2.233 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 29.2°C
Thermal Margin: 55.8°C (29.4 W)
Effective 9JA: 1.9°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q18. CLOCK BUFFER

VERILOG CODE:-

```

`timescale 1ns / 1ps
module clock_buffer(mclk,bclk);
    input mclk;
    output bclk;
    buf bl(bclk,mclk);
endmodule

```

TESTBENCH:-

```

`timescale 1ns / 1ps
module clock_buffer_tb();
    reg mclk;
    wire bclk;
    realtime t1,t2,t3,t4,t5,t6;
    parameter T=10;
    clock_buffer dut(mclk,bclk);
initial
begin
    mclk=1'b0;
    forever #(T/2) mclk=~mclk;
end
task master;
begin
    @(posedge mclk) t1=$realtime;
    @(posedge mclk) t2=$realtime;
    t3=t2-t1;
end
endtask
task bufout;
begin
    @(posedge bclk) t4=$realtime;
    @(posedge bclk) t5=$realtime;
    t6=t5-t4;
end
endtask
task freq_phase;
    realtime f,p;
begin
    f=t6-t3;
    p=t4-t1;
    $display("freq_diff=%0t,phase_diff=%0t",f,p);
end
endtask
initial
begin
    fork master;
    bufout;
    join freq_phase;
end
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |IBUF | 1|
|2 |OBUF | 1|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
| |Instance |Module |Cells |
+-----+-----+-----+
|1 |top | | 2|
+-----+-----+-----+
-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1015.395 ; gain = 0.000

```

POWER REPORT:-

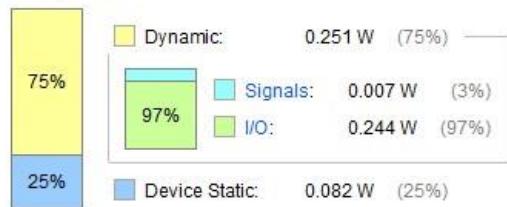
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 0.333 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 25.6°C
Thermal Margin: 59.4°C (31.3 W)
Effective 9JA: 1.9°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power



Q19. SYNCHRONOUS FIFO

VERILOG CODE:-

```
module sync_fifo (input [7:0] data_in, input clk, rst, rd, wr,
output empty, full, output reg [3:0]fifo_cnt,
output reg [7:0] data_out);

reg [7:0] fifo_ram [0:7];
reg [2:0] rd_ptr, wr_ptr;
assign empty= (fifo_cnt==0);
assign full =(fifo_cnt==8);
always @(posedge clk) begin: write
if (wr && ! full)
fifo_ram [wr_ptr] <= data_in;
else if (wr && rd)
fifo_ram [wr_ptr] <= data_in;
end

//Read and Write Clock
always @ (posedge clk) begin: read
if (rd && !empty)
data_out <= fifo_ram [rd_ptr];
else if (rd && wr)
data_out <= fifo_ram [rd_ptr];
end

//pointer block
always @(posedge clk) begin: pointer
if (rst) begin
wr_ptr <= 0;
rd_ptr <= 0;
end
else begin
wr_ptr <= ((wr && ! full) || (wr && rd)) ? wr_ptr+1 :
wr_ptr;
end
endmodule
```

```
-  
wr_ptr;  
rd_ptr <= ((rd && !empty) || (wr && rd)) ? rd_ptr+1:  
rd_ptr;  
end  
end  
  
//counter  
always @(posedge clk) begin: count  
if (rst) fifo_cnt <= 0;  
else begin  
case ({wr, rd})  
2'b00: fifo_cnt <= fifo_cnt;  
2'b01: fifo_cnt <= (fifo_cnt==0) ? 0: fifo_cnt-1;  
2'b10: fifo_cnt <= (fifo_cnt==8) ? 8: fifo_cnt+1;  
2'b11 : fifo_cnt <= fifo_cnt;  
default: fifo_cnt <= fifo_cnt;  
endcase  
end  
end  
endmodule
```

TESTBENCH:-

```
| module sync_fifo_tb();
|   reg clk, rst, wr, rd ;
|   reg[7:0] data_in;
|   reg[7:0] tempdata;
|   wire [7:0] data_out;
|   wire [3:0] fifo_cnt;

|   sync_fifo fifo( .clk(clk), .rst(rst), .data_in(data_in), .data_out(data_out),
|                 .wr(wr), .rd(rd), .empty(empty),
|                 .full(full), .fifo_cnt(fifo_cnt) );

| initial
| begin
|   clk = 0;
|   rst = 1;
|   rd = 0;
|   wr = 0;
|   tempdata = 0;
|   data_in = 0;

|   #15 rst = 0;

|   push(1);
|   fork
|     push(2);
|     pop(tempdata);
|   join
|   push(10);
|   push(20);
|   push(30);
|   push(40);
|   push(50);
|   push(60);
|   push(70);
```

```
    push(70);
    push(80);
    push(90);
    push(100);
    push(110);
    push(120);
    push(130);

    pop(tempdata);
    push(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    push(140);
    pop(tempdata);
    push(tempdata);//
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    pop(tempdata);
    push(5);
    pop(tempdata);
)
end

)
always
)
#5 clk = ~clk;
```

```
always
#5 clk = ~clk;

task push;
input[7:0] data;

if( full )
    $display("----Cannot push: FIFO Full---");
else
begin
    $display("Pushed ",data );
    data_in = data;
    wr= 1;
    @(posedge clk);
    #1 wr = 0;
end

endtask

task pop;
output [7:0] data;

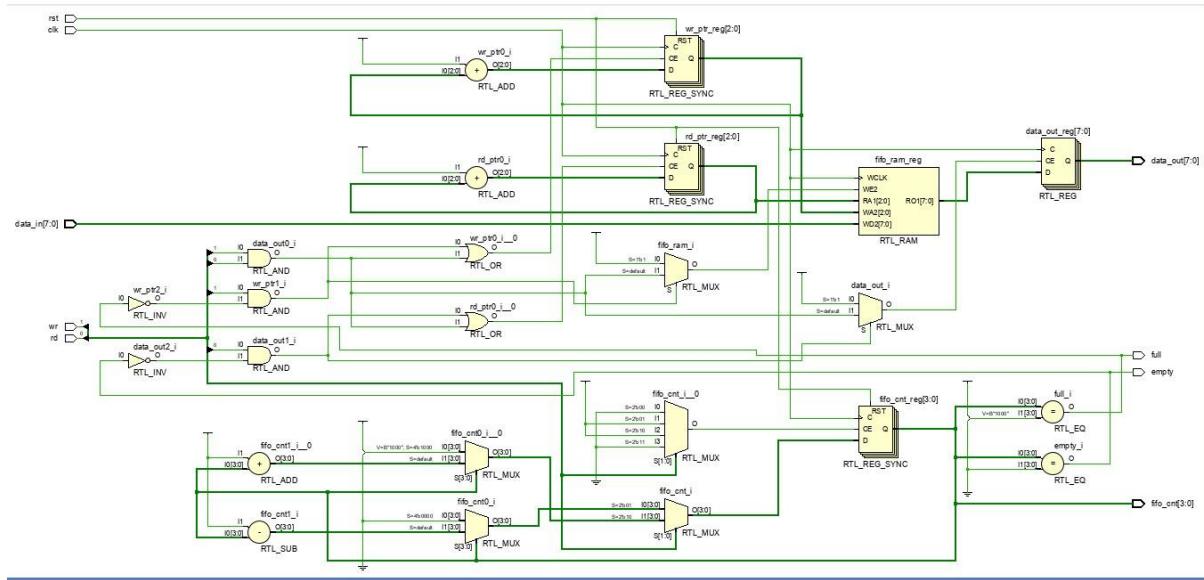
if( empty )
    $display("----Cannot Pop: FIFO Empty---");
else
begin

rd = 1;
@(posedge clk);

#1 rd = 0;
data = data_out;
$display("-----Poped ", data);

end
endtask
endmodule
```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
+-----+-----+
| !BlackBox name | Instances |
+-----+-----+
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
|   |Cell     |Count |
+-----+-----+
|1|BUFG     | 1|
|2|LUT2     | 3|
|3|LUT3     | 2|
|4|LUT4     | 4|
|5|LUT5     | 4|
|6|LUT6     | 4|
|7|RAM32M   | 2|
|8|FDRE     | 18|
|9|IBUF     | 12|
|10|OBUF    | 14|
+-----+-----+
Report Instance Areas:
+-----+-----+
|   |Instance |Module |Cells |
+-----+-----+
|1|top      ||       64|
+-----+-----+
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1017.957 ; gain = 0.000
-----
```

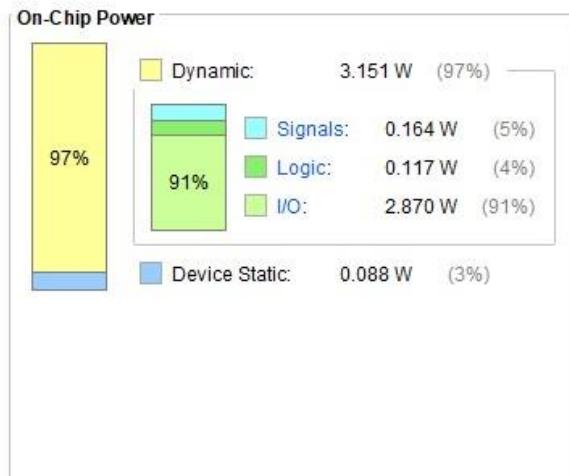
POWER REPORT:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	3.239 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	31.1°C
Thermal Margin:	53.9°C (28.4 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q20. PRIORITY ENCODER

VERILOG CODE:-

```
module pri_en(d,y,en);
  input [7:0] d;
  input en;
  output [2:0] y;
  reg [2:0] y;
  always @(d or en )
begin
  if(en)
begin
  casex(d)
  8'b00000001:y=3'b000;
  8'b0000001x:y=3'b001;
  8'b000001xx:y=3'b010;
  8'b00001xxx:y=3'b011;
  8'b0001xxxx:y=3'b100;
  8'b001xxxxx:y=3'b101;
  8'b01xxxxxx:y=3'b110;
  8'b1xxxxxxxx:y=3'b111;
  endcase
end
else
begin
y=3'bXXX;
end
end
endmodule
```

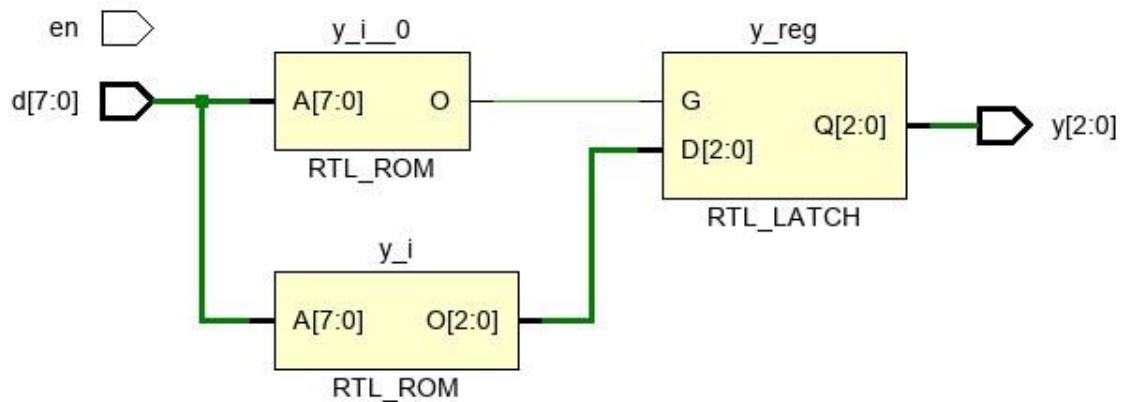
TEST BENCH:-

```

module pri_en_tb();
reg [7:0] d;
reg en;
wire [2:0] y;
pri_en dut(d,y,en);
initial
begin
en=1'b1;
d=8'b00000001; #10;
d=8'b00000011; #10;
d=8'b00000101; #10;
d=8'b00001001; #10;
d=8'b00010001; #10;
d=8'b00110001; #10;
d=8'b01110001; #10;
d=8'b11001001; #10;
#10 d=8'b10111001;
#10 d=8'b00101010;
#10 d=8'b00000001;
#10 d=8'b10100010;
end
initial
$monitor("Input %8b | Output %3b | Enable %b ",d,y,en);
initial #100 $finish;
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

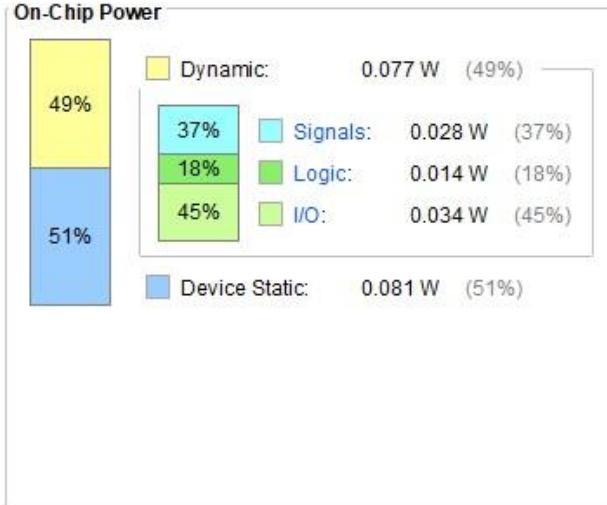
```
Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
|     |Cell  |Count |
+-----+-----+
|1    |LUT4  |    2|
|2    |LUT5  |    2|
|3    |LUT6  |    1|
|4    |LD    |    3|
|5    |IBUF  |    8|
|6    |OBUF  |    3|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
|     |Instance |Module |Cells |
+-----+-----+-----+
|1    |top    |      |   19|
+-----+-----+-----+
-----
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16 . Memory (MB): peak = 1018.668 ; gain = 0.000
```

POWER REPORT:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.158 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	25.3°C
Thermal Margin:	59.7°C (31.5 W)
Effective θ _{JA} :	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



Q21. SEVEN SEGMENT DISPLAY USING ROM

VERILOG CODE:-

```
| module ROM_sevenSegment
| #(
|   parameter addr_width = 16,
|   addr_bits = 4,
|   data_width = 7
| )
| {
|   input wire [addr_bits-1:0] addr,
|   output reg [data_width-1:0] data
| );
| always @*
| begin
| case(addr)
|   4'b0000 : data = 7'b1000000;
|   4'b0001 : data = 7'b1111001;
|   4'b0010 : data = 7'b0100100;
|   4'b0011 : data = 7'b0110000;
|   4'b0100 : data = 7'b0011001;
|   4'b0101 : data = 7'b00100010;
|   4'b0110 : data = 7'b00000010;
|   4'b0111 : data = 7'b1111000;
|   4'b1000 : data = 7'b00000000;
|   4'b1001 : data = 7'b00100000;
|   4'b1010 : data = 7'b00010000;
|   4'b1011 : data = 7'b00000011;
|   4'b1100 : data = 7'b10000110;
|   4'b1101 : data = 7'b0100001;
|   4'b1110 : data = 7'b00000110;
|   default : data = 7'b0001110;
| endcase
| end
| endmodule
```

TESTBENCH:-

```

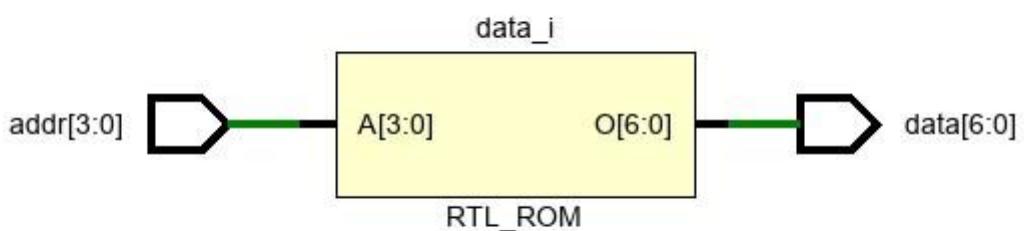
`timescale 1ns / 1ps
module ROM_sevenSegment_Test
();
reg [3:0] SW;
wire [6:0] HEX0;
wire [6:0] LEDR;

integer i;
wire [6:0] data;
ROM_sevenSegment seven_segment_ROM(.addr(SW), .data(data));

initial begin
for(i=0;i<16;i=i+1)
begin
SW=i;
#10;
end
end
assign HEX0 = data;
assign LEDR = data;
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
++-----+-----+
| |BlackBox name |Instances |
++-----+-----+
++-----+-----+

Report Cell Usage:
++-----+-----+
| |Cell |Count |
++-----+-----+
|1 |LUT4 |    7|
|2 |IBUF |     4|
|3 |OBUF |     7|
++-----+-----+

Report Instance Areas:
++-----+-----+-----+
| |Instance |Module |Cells |
++-----+-----+-----+
|1 |top |      |   18|
++-----+-----+-----+
-----  

Finished Writing Synthesis Report : Time (s): cpu = 00:00:33 ; elapsed = 00:00:43 . Memory (MB): peak = 1018.848 ; gain = 0.000
-----
```

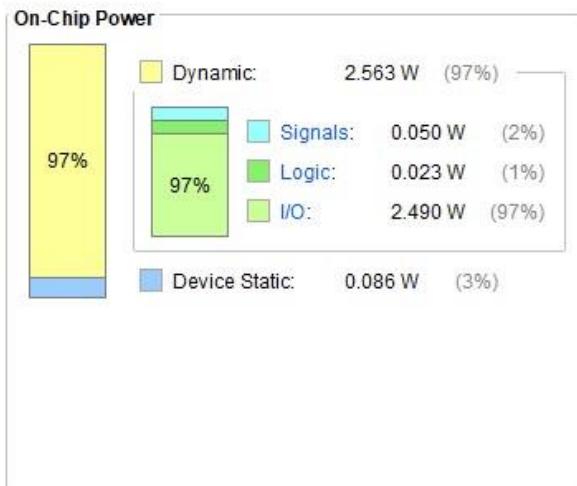
POWER REPORT:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	2.649 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	30.0°C
Thermal Margin:	55.0°C (29.0 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q22. SERIAL ADDER

VERILOG CODE:-

```

`timescale 1ns / 1ps
module serial_adder
  (  input clk,reset,
    input a,b,cin,
    output reg s,cout
  );

reg c,flag;

always@(posedge clk or posedge reset)
begin
  if(reset == 1) begin
    s = 0;
    cout = c;
    flag = 0;
  end else begin
    if(flag == 0)
      begin
        c = cin;
        flag = 1;
      end
    cout = 0;
    s = a ^ b ^ c;
    c = (a & b) | (c & b) | (a & c);
  end
end
endmodule

```

TESTBENCH:-

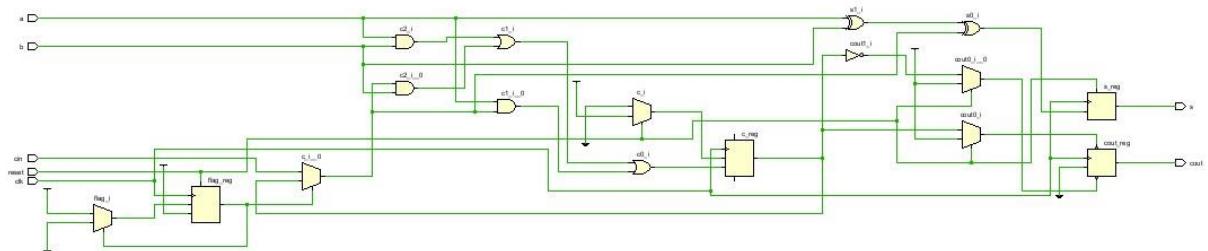
```

module serial_adder_tb();
    reg clk;
    reg reset;
    reg a;
    reg b;
    reg cin;
    wire s;
    wire cout;
    serial_adder uut (.clk(clk), .reset(reset), .a(a), .b(b), .cin(cin), .s(s), .cout(cout));
    always
        #5 clk = ~clk;
    initial begin
        clk = 1; reset = 0;
        a = 0; b = 0; cin = 0; reset = 1;
        #20;
        reset = 0;
        a = 1; b = 1; cin = 1;    #10;
        a = 1; b = 0; cin = 0;  #10;
        a = 1; b = 1; cin = 0;  #10;
        a = 1; b = 1; cin = 0;  #10;
        reset = 1;
        #10;
        reset = 0;

        a = 1; b = 1; cin = 1;    #10;
        a = 1; b = 0; cin = 0;  #10;
        a = 0; b = 0; cin = 0;  #10;
        a = 1; b = 0; cin = 0;  #10;
        a = 1; b = 1; cin = 0;  #10;
        reset = 1;
        #10;
    end
    initial $monitor(" A=%b | B=%b | Cin=%b | Sum=%b | Cout=%b | Clock =%b",a,b,cin,s,cout,clk);
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----

Report BlackBoxes:
++-----+-----+
| BlackBox name | Instances |
++-----+-----+
++-----+-----+

Report Cell Usage:
++-----+-----+
|   |Cell |Count |
++-----+-----+
|1  |BUFGE | 1|
|2  |LUT2 | 3|
|3  |LUT5 | 1|
|4  |LUT6 | 1|
|5  |FDCE | 2|
|6  |FDPE | 1|
|7  |FDRE | 1|
|8  |LDC | 1|
|9  |IBUF | 5|
|10 |OBUF | 2|
++-----+-----+

Report Instance Areas:
++-----+-----+
|   |Instance |Module |Cells |
++-----+-----+
|1  |top      |       | 18|
++-----+-----+

```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:20 ; elapsed = 00:00:28 . Memory (MB): peak = 1014.773 ; gain = 0.000

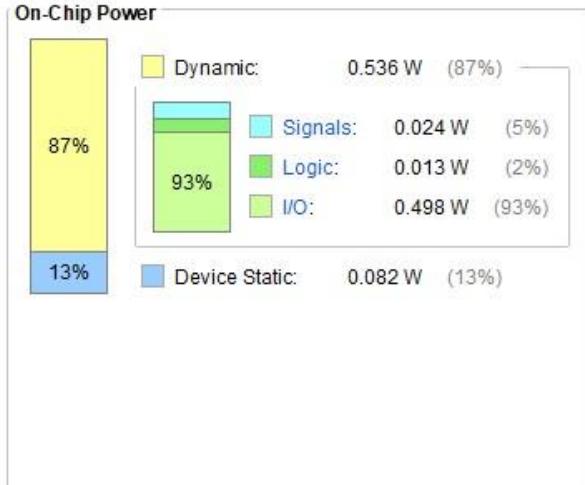
POWER REPORT:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.618 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.2°C
Thermal Margin:	58.8°C (31.0 W)
Effective gJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q23. FIXED PRIORITY ARBITER

VERILOG CODE:-

```
module fixedpriority_arbiter(output reg [3:0] GNT,
    input [3:0] REQ,
    input clk,reset
);
    always @(posedge clk or negedge reset)
// PRIORITY 3>1>0>2
    begin
        if(!reset)
            GNT<= 4'b0000;
        else if(REQ[3])
            GNT<= 4'b1000;
        else if(REQ[1])
            GNT<= 4'b0010;
        else if(REQ[0])
            GNT<= 4'b0001;
        else if(REQ[2])
            GNT<= 4'b0100;
        else
            GNT<= 4'b0000;
    end
endmodule
```

TESTBENCH:-

```

`timescale 1ns / 1ps
module fixedpriority_arbiter_tb();
wire [3:0] GNT;

reg [3:0] REQ;
reg clk,reset ;

fixedpoint_arbiter dut(.GNT(GNT),.REQ(REQ),.clk(clk),.reset(reset));

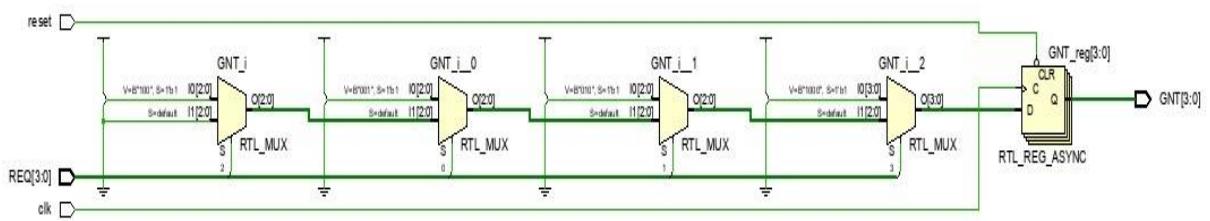
initial
clk=0;
always #4 clk <= ~clk ;

initial
begin
reset =0;
#4 reset =1;
repeat(20)
begin
#5 REQ<=$random();

end
#100 $finish();
end
initial begin
$monitor("REQ=%b,GNT=%b,reset=%b",REQ,GNT,reset);
end
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

```

-----
Start Writing Synthesis Report
-----
Report BlackBoxes:
+-----+-----+
| |BlackBox name |Instances |
+-----+-----+
+-----+-----+
Report Cell Usage:
+-----+-----+
| |Cell |Count |
+-----+-----+
|1 |BUFGE | 1|
|2 |LUT1 | 1|
|3 |LUT2 | 1|
|4 |LUT3 | 1|
|5 |LUT4 | 1|
|6 |FDCE | 4|
|7 |IBUF | 6|
|8 |OBUF | 4|
+-----+-----+
Report Instance Areas:
+-----+-----+-----+
| |Instance |Module |Cells |
+-----+-----+-----+
|1 |top | | 19|
+-----+-----+
-----
Finished Writing Synthesis Report : Time (s): cpu = 00:00:25 ; elapsed = 00:00:35 . Memory (MB): peak = 1015.289 ; gain = 0.000
-----
```

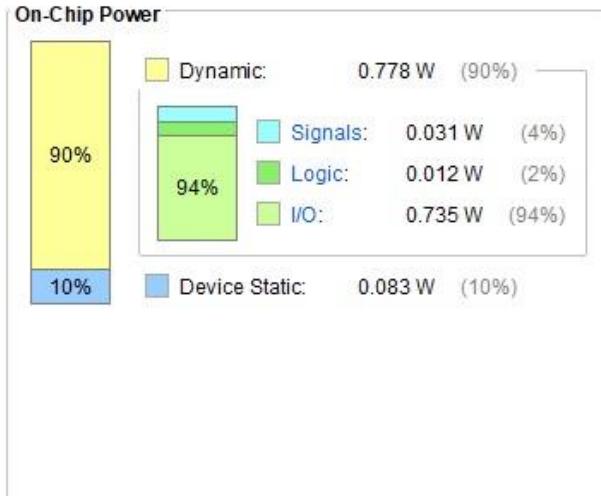
POWER REPORT:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	0.861 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	26.6°C
Thermal Margin:	58.4°C (30.8 W)
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Q24. ROUND ROBIN ARBITER

VERILOG CODE:-

```
`timescale 1ns / 1ps
`module roundrobin_arbiter(
    input clk,rst_n,
    input [3:0] REQ,
    output reg [3:0] GNT
);
    reg[2:0] pr_state;
    reg[2:0] nxt_state;

    parameter [2:0] Sideal = 3'b000;
    parameter [2:0]     S0 = 3'b001;
    parameter [2:0]     S1 = 3'b010;
    parameter [2:0]     S2 = 3'b011;
    parameter [2:0]     S3 = 3'b100;

    always @(posedge clk or negedge rst_n)

    begin
        if(!rst_n)
            pr_state <= Sideal;
        else
            pr_state <=nxt_state;
    end

    always@(*)
    begin
        case(pr_state)
            Sideal:
                begin
                    if(REQ[0])
                        nxt_state = S0;
                    else if (REQ[1])
                        nxt_state = S1;
                    else if (REQ[2])
                        nxt state = S2;
```

```
always@(*)  
begin  
    case(pr_state)  
        Sideal:  
            begin  
                if(REQ[0])  
                    nxt_state = S0;  
                else if (REQ[1])  
                    nxt_state = S1;  
                else if (REQ[2])  
                    nxt_state = S2;  
                else if (REQ[3])  
                    nxt_state = S3;  
                else  
                    nxt_state =Sideal;  
            end  
        S0:  
            begin  
                if (REQ[1])  
                    nxt_state = S1;  
                else if (REQ[2])  
                    nxt_state = S2;  
                else if (REQ[3])  
                    nxt_state = S3;  
                else if(REQ[0])  
                    nxt_state =S0;  
                else  
                    nxt_state =Sideal;  
            end  
        S1:  
            begin  
                if (REQ[2])  
                    nxt_state = S2;  
                else if (REQ[3])
```

```
S1:
begin
    if (REQ[2])
        nxt_state = S2;
    else if (REQ[3])
        nxt_state = S3;
    else if(REQ[0])
        nxt_state =S0;
    else if (REQ[1])
        nxt_state = S1;
    else
        nxt_state =Sideal;
end
S2:
begin
    if (REQ[3])
        nxt_state = S3;
    else if(REQ[0])
        nxt_state =S0;
    else if (REQ[1])
        nxt_state = S1;
    else if (REQ[2])
        nxt_state = S2;
    else
        nxt_state =Sideal;
end
S3:
begin
    if(REQ[0])
        nxt_state =S0;
    else if (REQ[1])
        nxt_state = S1;
    else if (REQ[2])
        nxt_state = S2;
    else if (REQ[3])
```

```

        nxt_state = S2;
    } else if (REQ[3])
        nxt_state = S3;
    else
        nxt_state = Sideal;
end
endcase

end

always @(*)
begin
    case (pr_state)
        S0: GNT=4'b0001;
        S1: GNT=4'b0010;
        S2: GNT=4'b0011;
        S3: GNT=4'b0100;
        default: GNT=4'b0000;
    endcase
end
endmodule

```

TESTBENCH:-

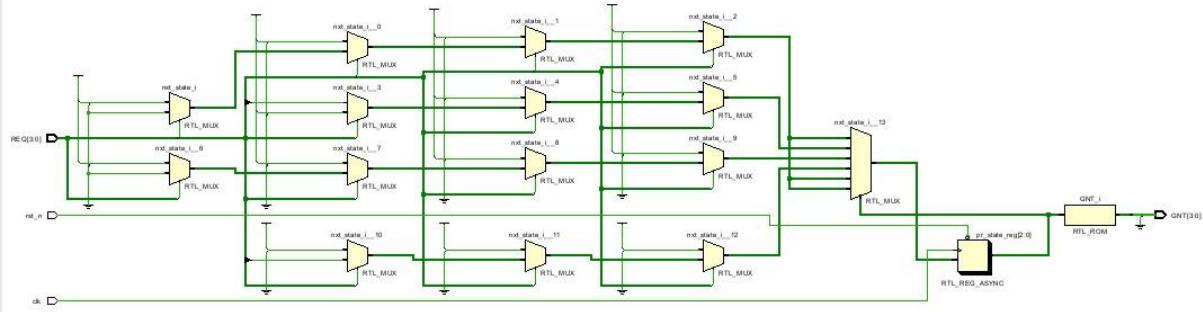
```

`timescale 1ns / 1ps
module roundrobin_arbiter_tb();
    reg clk;
    reg rst_n;
    reg [3:0] REQ;
    wire [3:0] GNT;
    roundrobin_arbiter DUT(.clk(clk), .rst_n(rst_n), .REQ(REQ), .GNT(GNT));

    always #5 clk = ~clk;
initial begin
    clk = 0;
    rst_n = 1;
    REQ = 4'b0;
    #5 rst_n = 1;
    @(negedge clk) REQ = 4'b1000;
    @(negedge clk) REQ = 4'b1010;
    @(negedge clk) REQ = 4'b0010;
    @(negedge clk) REQ = 4'b0110;
    @(negedge clk) REQ = 4'b1110;
    @(negedge clk) REQ = 4'b1111;
    @(negedge clk) REQ = 4'b0100;
    @(negedge clk) REQ = 4'b0010;
    #5 rst_n = 0;
    #100 $finish;
end
endmodule

```

RTL SCHEMATIC:-



SYNTHESIS REPORT:-

Start Writing Synthesis Report

Report BlackBoxes:

BlackBox name	Instances

Report Cell Usage:

Cell	Count
BUF	1
LUT	1
LUT2	2
LUT3	2
LUT5	1
LUT6	4
MUXF7	2
FDCE	3
IBUF	6
OBUF	4

Report Instance Areas:

Instance	Module	Cells
top		26

Finished Writing Synthesis Report : Time (s): cpu = 00:00:19 ; elapsed = 00:00:25 . Memory (MB): peak = 1017.727 ; gain = 0.000

POWER REPORT:-

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	1.408 W
Design Power Budget:	Not Specified
Power Budget Margin:	N/A
Junction Temperature:	27.7°C
Thermal Margin:	57.3°C (30.3 W)
Effective 9JA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power

