CS220: Computer Organization
Quiz#1 Solution Sketch

Name:
Roll No.:

1. A purely combinational logic module takes two inputs A and B, each of which is three-bit wide. The module computes four outputs: $A < B$, $A > B$, $A == B$, and $|A - B|$. If this module is implemented using a read-only memory (ROM), calculate the number of rows and the width of the ROM. **(1+2 points)**

Solution: Since the total number of input bits is six, the number of rows would be 2^6 or 64. The width of the ROM is equal to the number of bits stored in each row. Each of $A < B$, $A > B$, $A == B$ can be stored using one bit. If A and B are assumed to be non-negative integers, the maximum value of $|A - B|$ is 7 requiring three bits to store. If A and B are assumed to be arbitrary three-bit integers using one bit for representing the sign, the maximum value of $|A - B|$ is 6 requiring three bits to store. Therefore, the width of the ROM needs to be six bits (three bits for $A < B$, $A > B$, $A == B$ and three more bits for $|A - B|$).

2. A single-chip SRAM module has 32 rows and 32-bit width. It has three read ports. Calculate the number of decoders, number of inputs to each decoder, total number of wordlines, and total number of bitlines. **(1+1+1+1 points)**

Solution: Number of decoders = number of ports = 3. Number of inputs to each decoder = $\log_2(\text{number of rows})$ = 5. Total number of wordlines = number of wordlines per port $\times$ number of ports = 32 $\times$ 3 = 96. Total number of bitlines = number of bitlines per port $\times$ number of ports = 32 $\times$ 3 = 96.

3. Consider a combinational logic function f that takes a three-bit input from flip-flops x_1, x_2, x_3 and produces a four-bit output which is stored in flip-flops y_1, y_2, y_3, y_4. All flip-flops are positive edge-triggered. The hold time and the setup time of the flip-flops are 100 picoseconds and 180 picoseconds, respectively. The propagation delay through each flip-flop is 80 picoseconds. Assume the clock skew to be zero. A 1 GHz clock is applied to this design. The paths of f that compute y_1, y_2, y_3, y_4 take respectively 500, 200, 900, and 800 picoseconds. Which of the outputs won't be stored correctly? **(3 points)**

Solution: For correct storage of output, clock cycle time must be at least as large as the sum of propagation delay, setup time, skew time, and computation time of the combinational logic path producing the output. This condition does not hold for y_3 and y_4.