FACULTY PROFILE FORMAT (Format 3)		
Staff Name	:	Dr. P. LATHA
Faculty ID	:	TEC26
Designation	:	Associate Professor
Qualification	:	M.E., Ph.D
Teaching Experience	:	25 years and 3 months
Area of Specialization	:	VLSI Design, RSoC, Image Processing and WSN
Subjects Handled	:	**UG Subjects:** 1. Basic Electronics and Devices 2. Circuit Theory 3. Linear Integrated circuits 4. Digital Principles and system Design 5. Digital Logic Circuits 6. Digital System Design 7. Digital Electronics 8. Microprocessor and Microcontroller 9. Electronics and Microprocessor 10. Embedded Systems 11. Computer Communication Networks 12. VLSI Design **PG Subjects:** 13. High Performance Communication Networks 14. ASIC Design 15. Advanced Digital Logic System Design 16. System on Chip 17. ASIC and FPGA Design
Books Published	:	-
Journals Published	:	1. **Latha, P**, Bhagyaveni, MA & Ancilin, J, DECEMBER 2012, 'VLSI Implementation of Reconfigurable WSN Node for Surveillance', European Journal of Scientific Research**,** vol. 92, no. 2, pp. 238-256, ISSN: 1450-216X. (Anna University, Chennai, ANNEXURE – II, Version 2012.2.1, Sl.No.5855). **Index: Elsevier (Scopus), Web of Science Master & SCI. Impact Factor: 0.713.** http://www.europeanjournalofscientificresearch.com. 2. **Latha, P**, Bhagyaveni, MA & Steffi Lionel, FEBRUARY 2014, 'Reconfigurable SoC Architecture for Ship Intrusion Detection', Journal of Theoretical and Applied Information Technology, vol. 60, no. 1, pp. 95-105, ISSN: 1992-8645. (Anna University, Chennai, ANNEXURE – II, Version 2013.2.1, Sl.No.12050). **Index: Elsevier (Scopus), DBLP & SCI. Impact Factor: 1.71.** http://www.jatit.org. 3. **Latha, P**, Bhagyaveni, MA & Preethi, SR**,** JUNE 2014, 'Efficient Removal of Impulse Noise from Video using Adaptive Threshold Algorithm' Journal of Theoretical and Applied Information Technology, vol. 64 no.1, pp. 22-31, ISSN: 1992-8645. (Anna University, Chennai, ANNEXURE –

		II, Version 2013.2.1, Sl.No.12050). **Index: Elsevier (Scopus), DBLP & SCI. Impact Factor: 1.71. Cited: 2 Times.** 4. Preethi, SR & **Latha, P**, MARCH 2015, 'ADAPTIVE DENOISING TECHNIQUE FOR COLOUR IMAGES' IJRET: International Journal of Research in Engineering and Technology, Vol. 04, no. 03, eISSN: 2319-1163, pISSN: 2321-7308. **Index: Google Scholar. Impact Factor: 2.375**. http://www.ijret.org. 5. M. Subhashini**, P. Latha** and Dr. M. A. Bhagyaveni, MARCH-2015, "Design and Implementation of Cascaded-H-Bridge Multilevel Inverter by FPGA Controller for Photo Voltaic Application", International Journal for Technological Research, Volume 2, Issue 7, ISSN(online): 2347-4718. **Index: Google Scholar, Academia.edu, CiteFactor, DRJI. Impact Factor: 1.46**. http://www.ijtre.org**.** 6. M. Subhashini**, P. Latha** and Dr. M. A. Bhagyaveni, MARCH-2015, "Determining the Modulation Index and Switching angles as a Mitigation Technique for Elimination of Harmonic Distortion in Cascaded-H-Bridge Multilevel Inverter fed Solar Photo Voltaic Module", International Journal for Technological Research, Volume 2, Issue 7, ISSN(online): 2347-4718. **Index: Google Scholar, Academia.edu, CiteFactor, DRJI. Impact Factor: 1.46.** http://www.ijtre.org. 7. M. Subhashini, **P. Latha** and Dr. M. A. Bhagyaveni, MARCH-2015, "Implementation of a Solar Photo Voltaic Module in Cascaded-H-Bridge Multilevel Inverter Controlled by Xilinx System Generator Tool", "International Journal for Technological Research", Volume 2, Issue 7, ISSN(online): 2347-4718. **Index: Google Scholar, Academia.edu, CiteFactor, DRJI. Impact Factor: 1.46.** http://www.ijtre.org. 8. M. Subhashini, **P. Latha** and Dr. M. A. Bhagyaveni, "Comparative Analysis of Harmonic Distortion of a Solar PV fed Cascaded- H-Bridge Multilevel Inverter Controlled by FPGA and Diode Clamped Inverter", Indian Journal of Science and Technology, Volume 8, Issue 16, ISSN (Print) : 0974-6846, ISSN (Online) : 0974-5645 (Anna University, Chennai, ANNEXURE-II Journal, Version 2014.2, Sl.No.8167). **Index: Scopus, EBSCO & j-Scholar.** http://www.indjst.org.
Conference /Workshop Attended	:	**Conference:** **1.** Denesh Kumar Sundar, Hari Venkateswaran, **Latha. P** and Bhagyaveni. M. A, "Analysis of Sub-5nm Novel FinFET Device over 180nm Bulk CMOS Device", 1st International Conference on Nano-electronics, Circuits & Communication Systems (NCCS-2015) on 9-10th May-2015. IETE Ranchi Centre. **2. Latha P** and Steffi Lionel (2013) "Wireless Sensor Network Based Ship Intrusion Detection", in proceedings of an International Conference on Computational Intelligence and Advanced Manufacturing Research (ICCIAMR-2013) in VELS UNIVERSITY, Chennai. **3. P.Latha** and S. Simcy, "Reconfigurable Architecture for Moving Object Detection using Background Subtraction Algorithm **",** International

		conference on Innovative Trends in Computing and Technology, ICITCT 2013, pp 237-243, March 2013. **4.** **P.Latha** , R.K.Mugelan, J.Boobalan, L.Ravikiran, Dr. M. A. Bhagyaveni, "Surveillance ROVER with 3G Live Video Streaming and GPS Tracker", in proceedings of International Conference on Control,Communication and Computer Technology (CCCT- 2012) **5.** **P.Latha**, Jane J Jim, "A Reconfigurable Architecture for Encryption Algorithm using Subband Re-orientation", in proceedings of APEC-National Conference on Advanced Computing & Commn-NCACC11 **6.** **P.Latha** , J.Ancilin, Dr. Bhagyaveni.M.A. "Remote Reconfiguration for Wireless Sensor Networks", in proceedings of IIST 2010 **7.** **Latha P**, Dr. Bhagyaveni. M. A. "Reconfigurable FPGA Based Architecture for Surveillance Systems in WSN", in Proceeding of IEEE International Conference on Wireless Communication and Sensor Computing (*ICWCSC 2010)* January 2-4, 2010. **<u>Workshop & FDP:</u>** **8.** Resource Person, FDP on VLSI DESIGN at Tagore Institute of Engineering and Technology, Salem, December 15, 2014. **9.** Workshop on Xilinx FPGA Solutions for Image & Signal Processing Applications at TIFAC-CORE, VIT University, Vellore-14, April 4-6, 2013. **10.** Workshop on Image Processing Framework using FPGA at MIT, Anna University, Chennai, October 15-16, 2012. **11.** Workshop on Reconfigurable Technology and Its Applications at CEG, Anna University, Chennai, October 18, 2011. **12.** FDP on EDA Tools for VLSI Design and Signal Processing at SSN College of Engineering, Chennai, November 15-18, 2010 **13.** FDP on Computer Networks and Networks Lab at Easwari Engineering College, Chennai, 19.11.2007 to 01.12.2007 **14.** Workshop on Network Simulators for Wireless Networks at MIT, Chennai, September 08-09, 2007. **15.** Workshop on Designing Systems on Programmable Chip(SOPC) at National Institute of Technology, Tiruchirappalli, December 23-24, 2005. **16.** Workshop on Networking, Digital Signal Processing and Biomedical Engineering at GCT, Coimbatore, January 6-7, 2003.
Patent Details	:	-
Funded Project Details		-