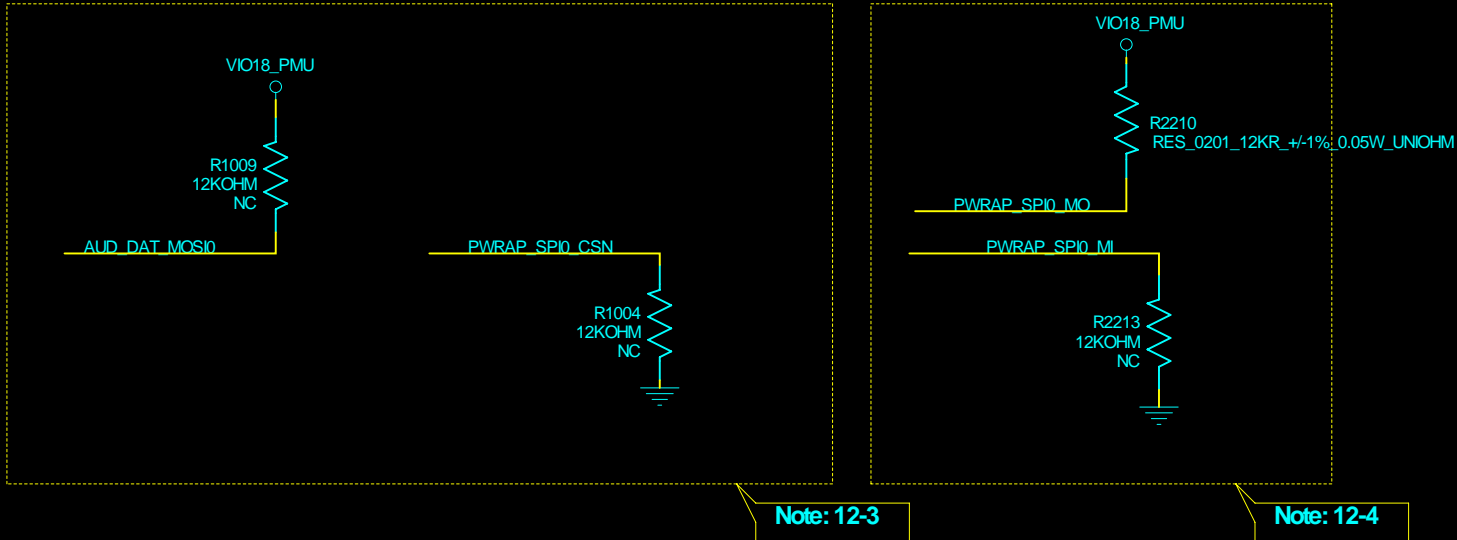
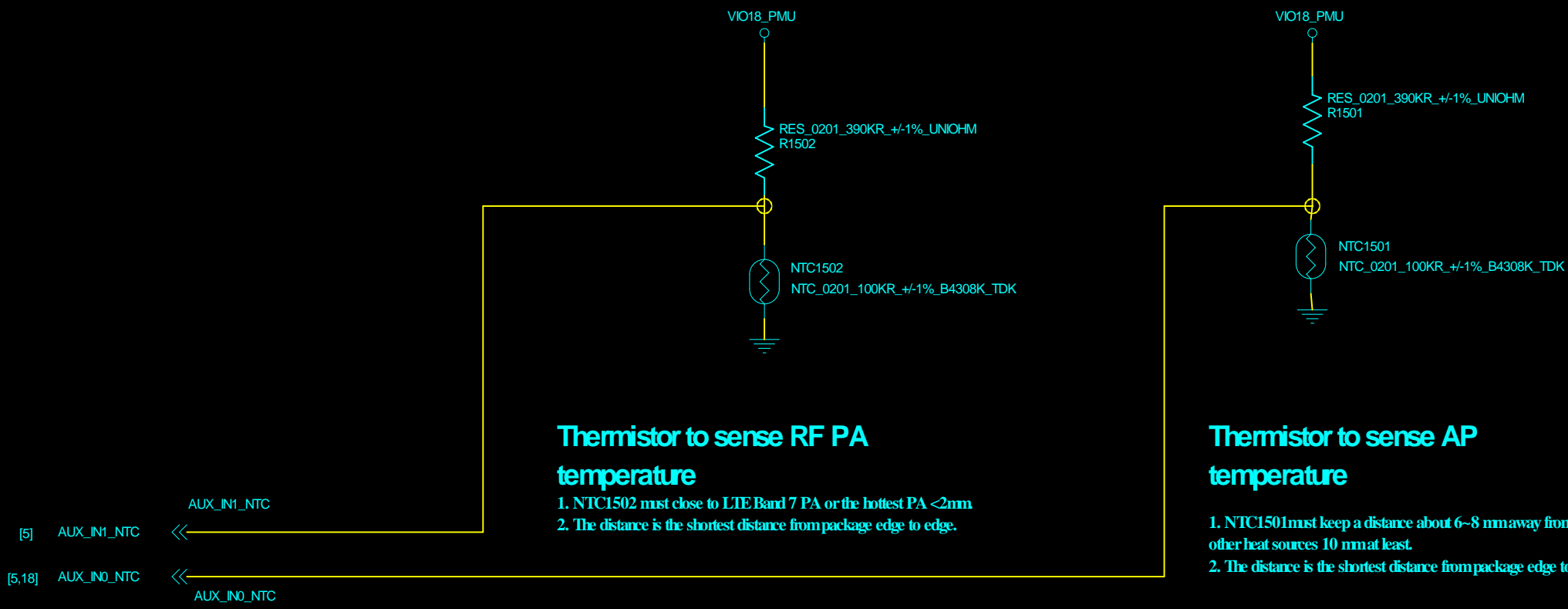
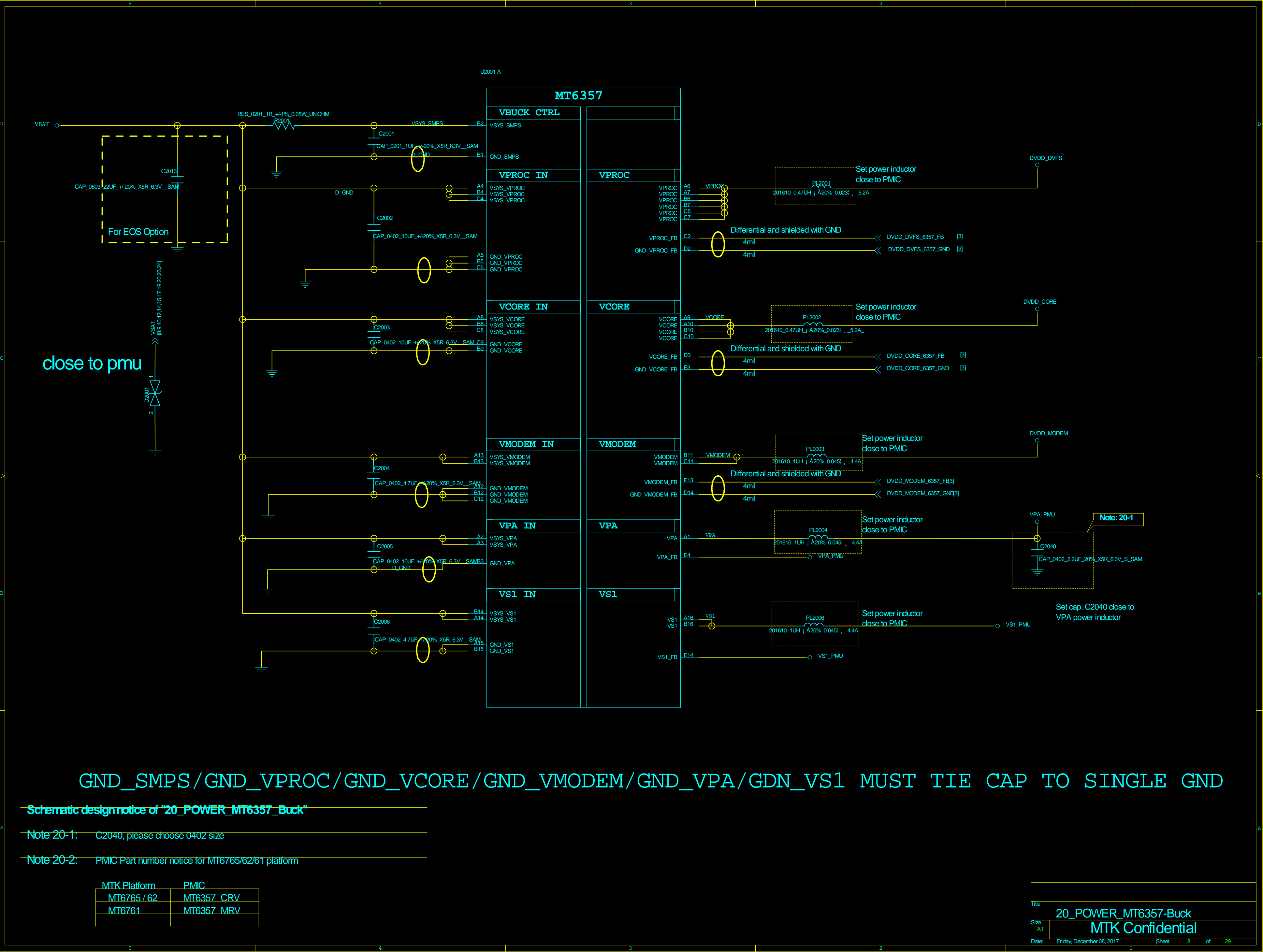


Schematic design notice of "12_BB_1" page.			
Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.			
Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.			
Note 12-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSIO" are bootstrap pin to select which interface will be the JTAG pin out.			
PWRAP_SPI0_CSN	AUD_DAT_MOSIO	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by ext. PU)	SPI0+EINT8	SPI1+SPI3
LO (by ext. PD)	LO	SPI0+EINT8	N/A
LO (by ext. PD)	HI (by ext. PU)	MSDC1	N/A

Note 12-4: PWRAP_SPI0_MO and PWRAP_SPI0_MI are DDR type feature in bootstrap		
PWRAP_SPI0_MI	Bootling interface	
default=PU	DDR	MSDC0 pin mux
LO (by ext. PD)	LPDDR3	follow LP3 Ref SCH.
HI	LPDDR4X	follow LP4X Ref SCH.

Note 12-5: Please set unused IQ pins in NC





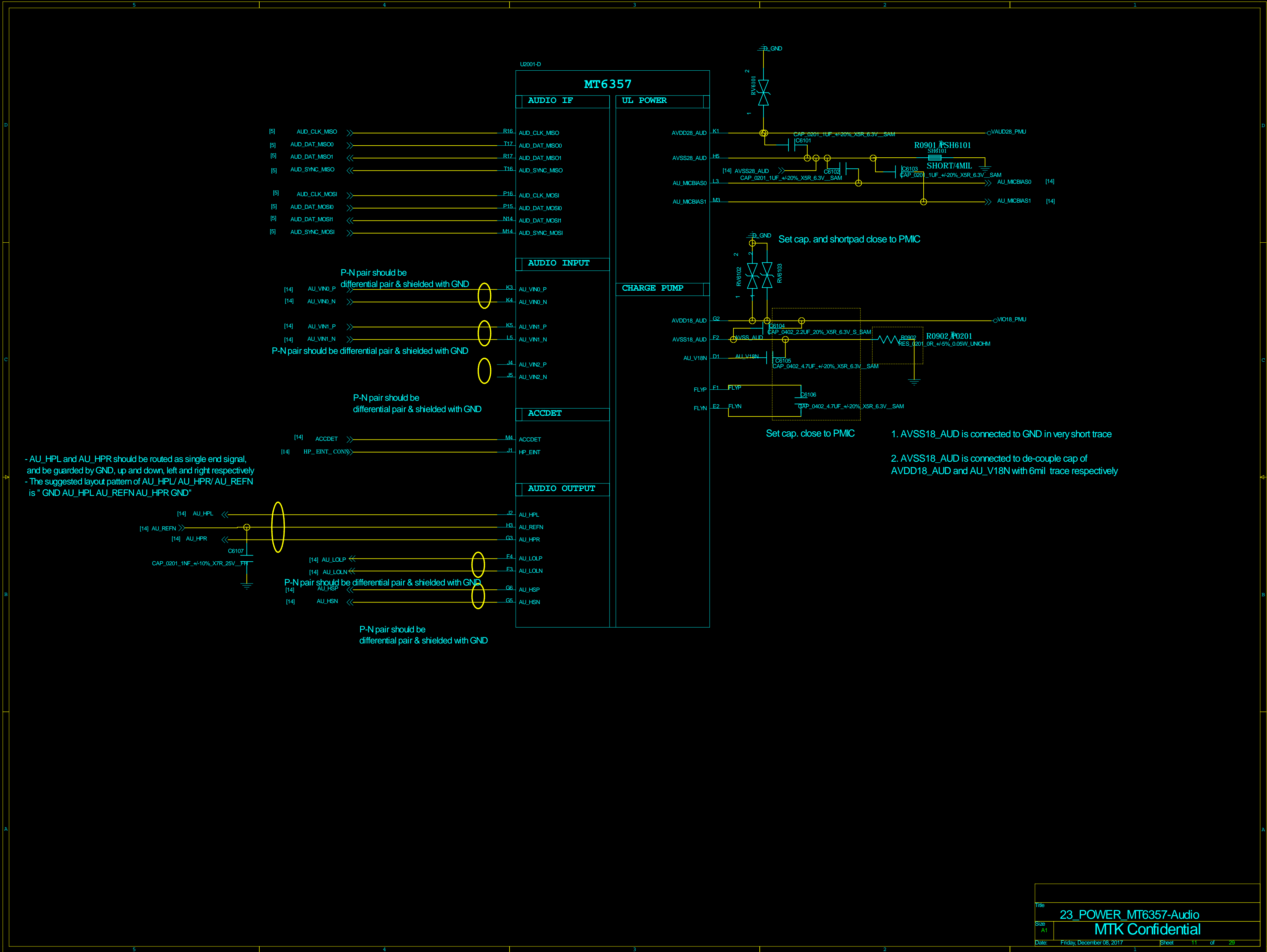
GND_SMPS/GND_VPROC/GND_VCORE/GND_VMODEM/GND_VPA/GDN_VS1 MUST TIE CAP TO SINGLE GND

Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: C2040, please choose 0402 size

Note 20-2: PMIC Part number notice for MT6765/62/61 platform

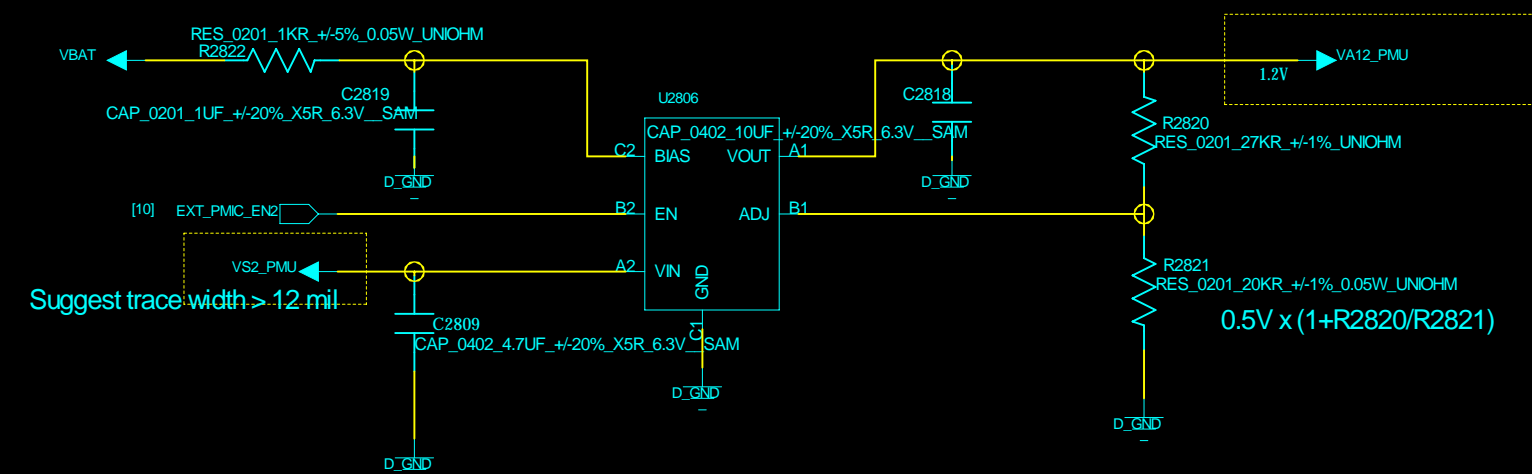




LDO for VA12

Note: 28-1

Suggest trace width > 12 mil



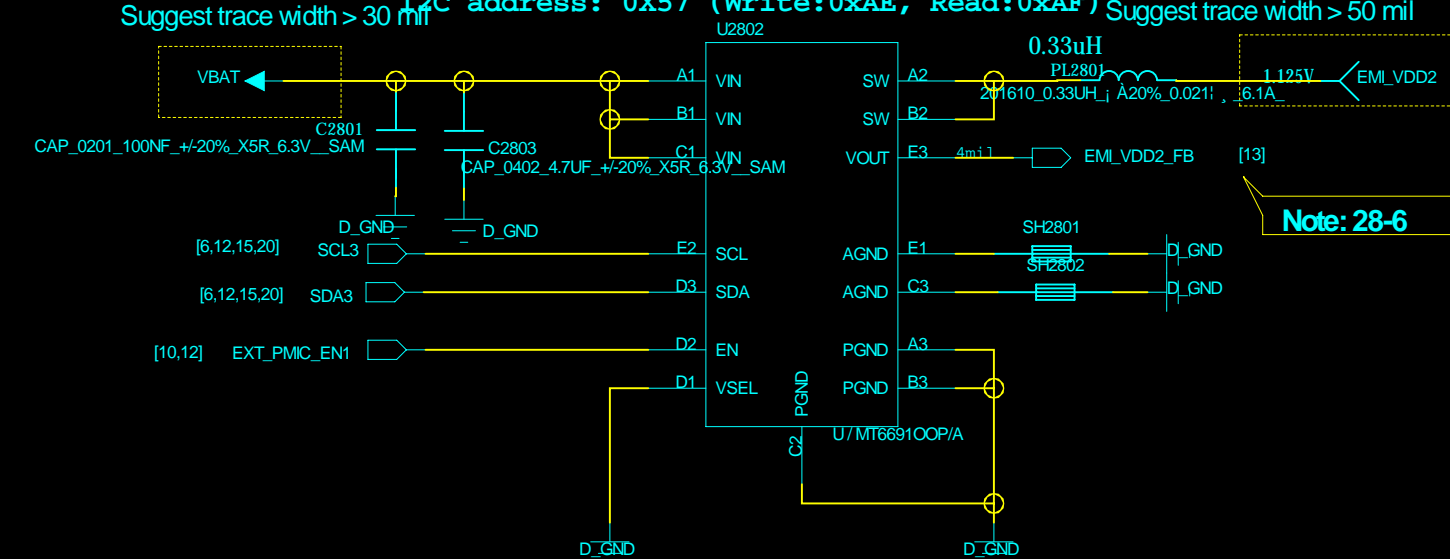
Ext. buck LPDDR4X/LPDDR4 VDRAM

Note: 28-4

MT6691OOP/A / Ext. buck LP4X/LP4 VDRAM (VDD2)

I2C address: 0X57 (Write:0xAE, Read:0xAF) Suggest trace width > 50 mil

7) Suggest trace width > 50 mil

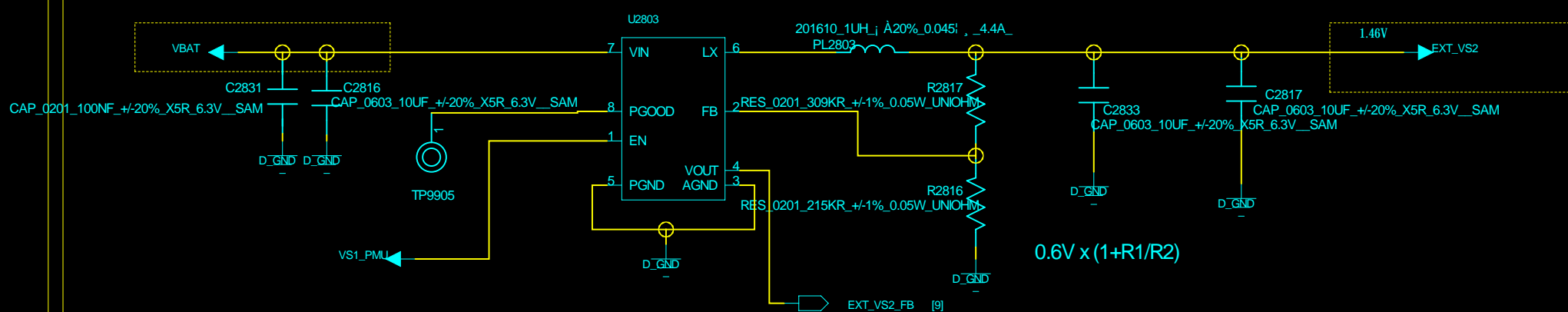


Ext. Bulk for VS2

Note: 28-2

Suggest trace width > 25 mil

Suggest trace width > 40 mil



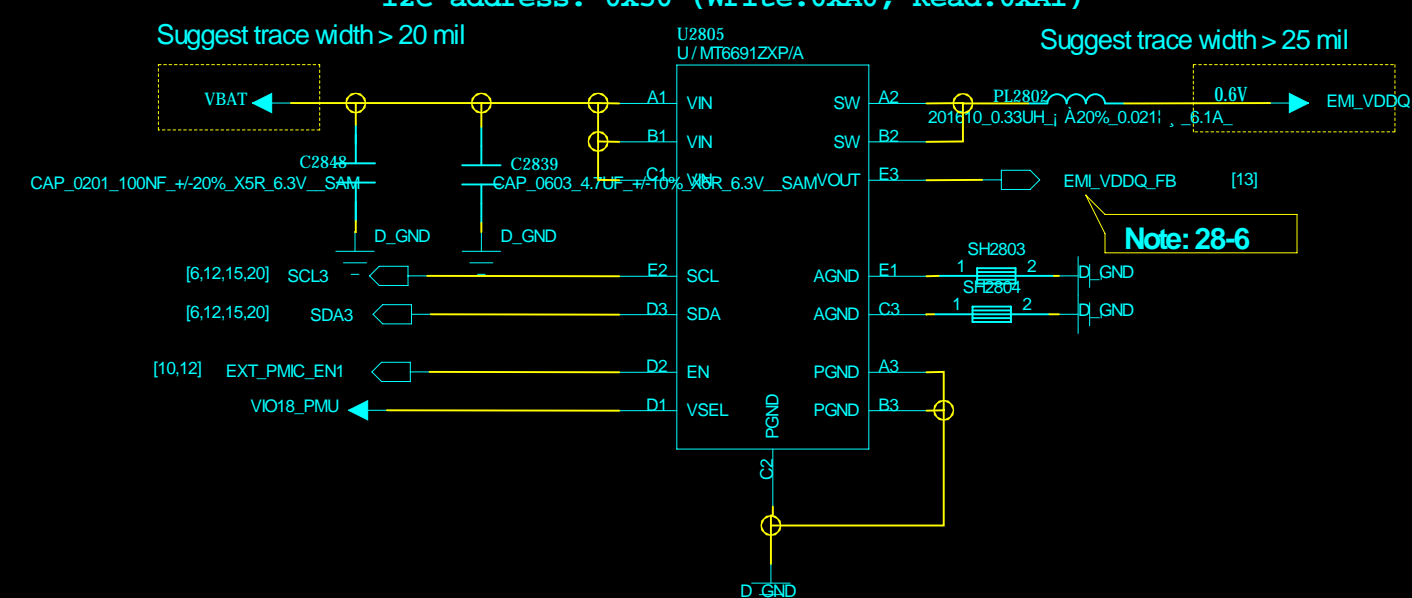
Ext. buck LPDDR4X VDDQ

Note: 28-4

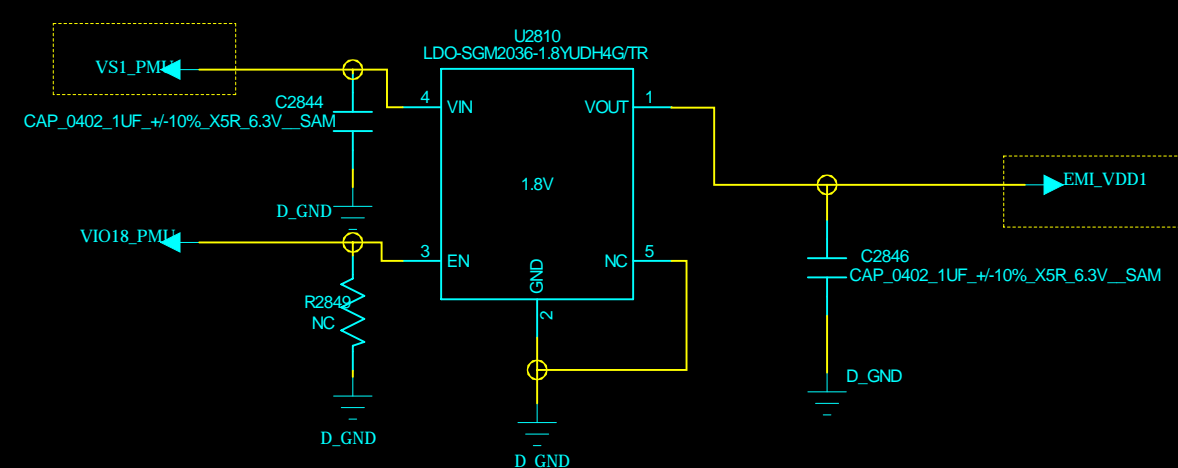
MT6691ZXP/A / Ext. buck LP4X VDRAM(VDDQ)

```
I2C address: 0x50 (Write:0xA0, Read:0xA1)
```

Suggest trace width > 25 mil



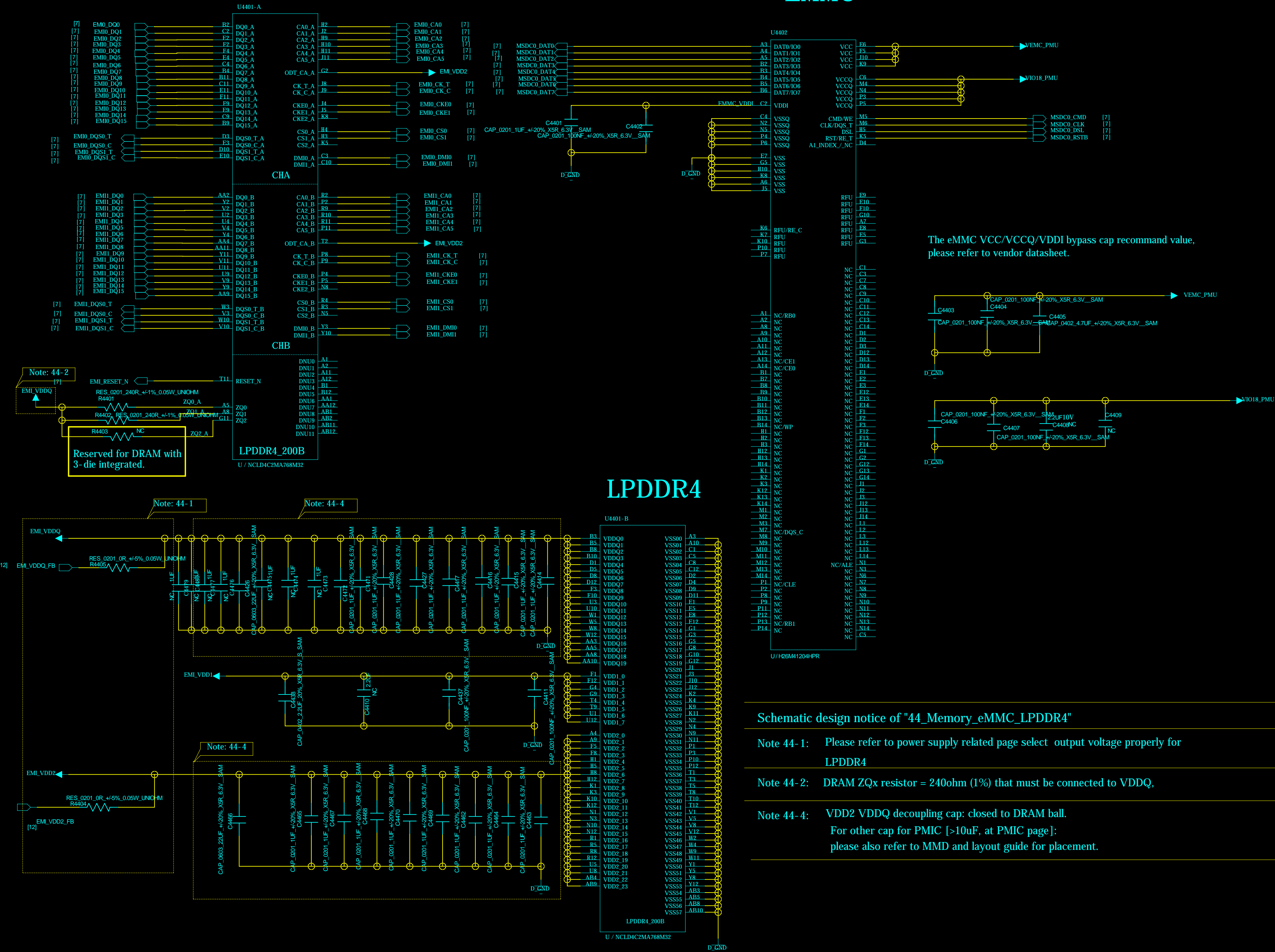
LPDDR4 VDD1 1.8V LDO



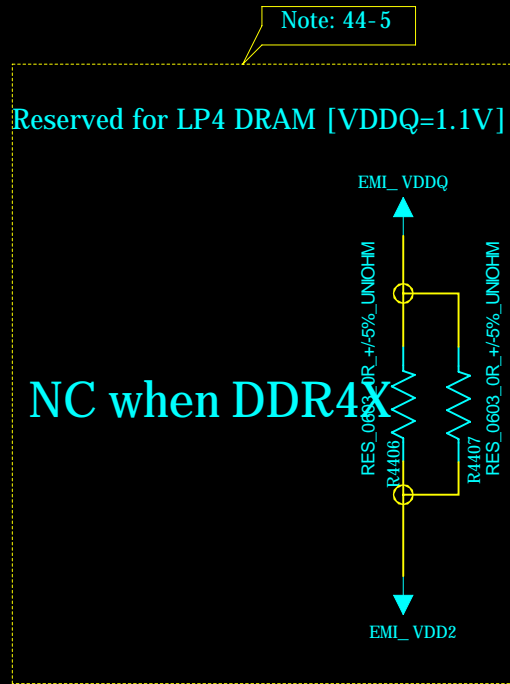
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LPDDR4

EMMC



The eMMC VCC/VCCQ/VDDI bypass cap recommend value, please refer to vendor datasheet.



Schematic design notice of "44_Memory_eMMC_LPDDR4"

Note 44-1: Please refer to power supply related page select output voltage properly for LPDDR4

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10nF, at PMIC page]: please also refer to MMD and layout guide for placement.

COMPANY: <Company Name>

TITLE: <Title>

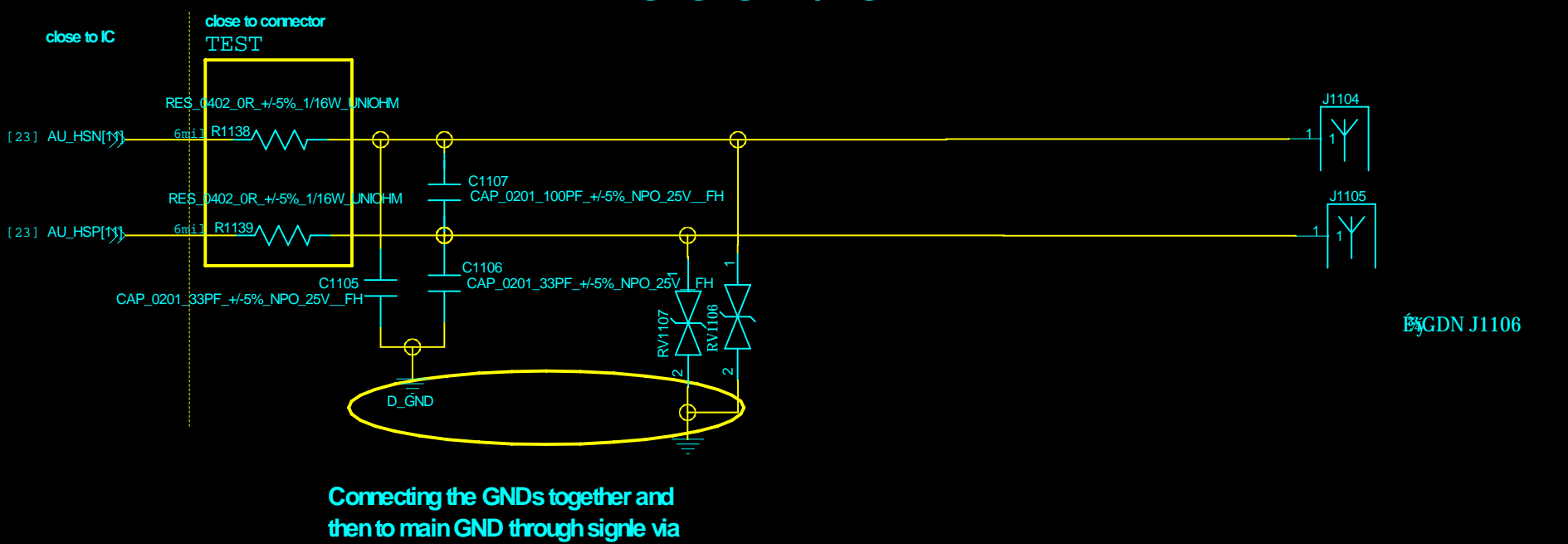
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CHECKED: <Checked By>	DATED: <Checked Date>
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RELEASED: <Released By>	DATED: <Release Date>

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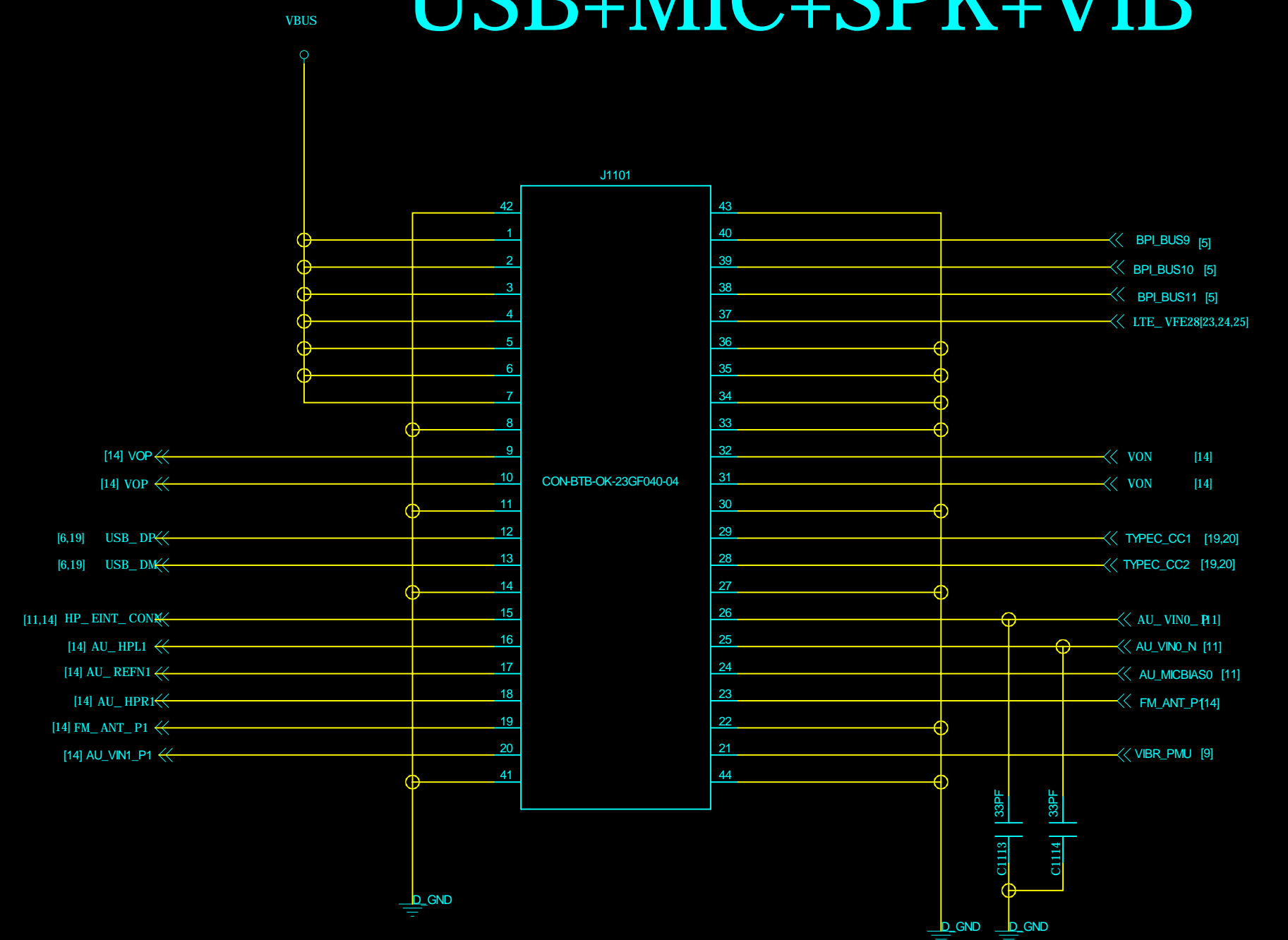


Platform	MT6357	
Mode	ACC mode	DCC mode
EINT	HP_EINT	HP_EINT
Key-Detection	ACCPST	AU_VIN1_P
RI126	1uP	0 ohm
RI127	1uP	0 ohm
RI132	1K	NC
RI133	1.5K	NC
RI131	NC	2.49K
CI140	4.7uP	0 ohm
RI129	0 ohm	NC
RE208	47K ohm	47K ohm

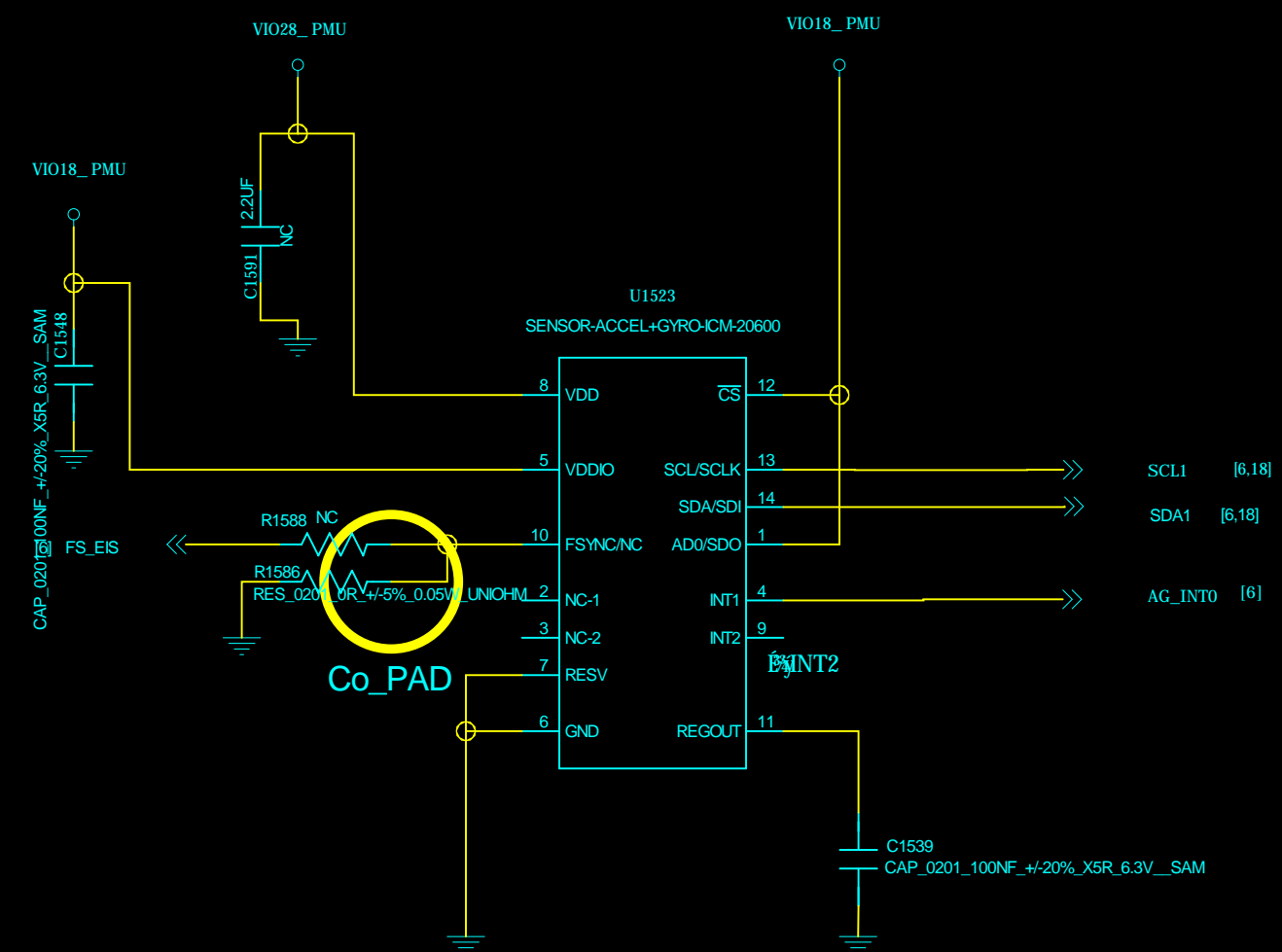
Note 62-5: Please select R6231 with 0402 size



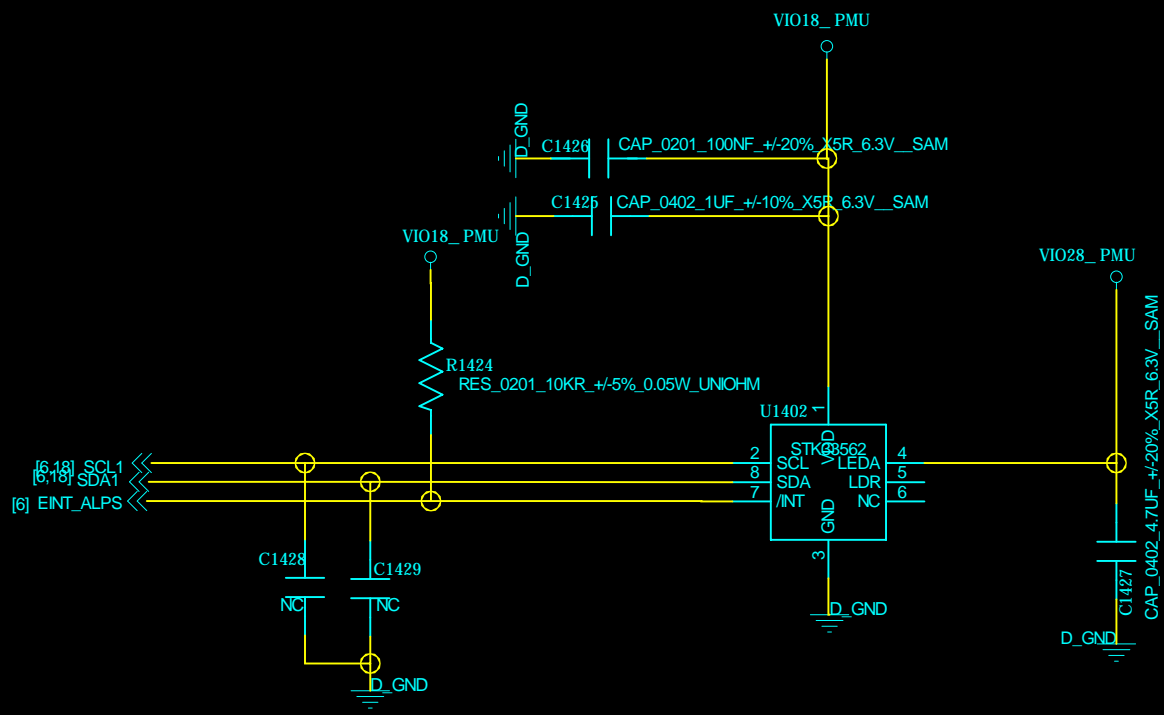
USB+MIC+SPK+VIB



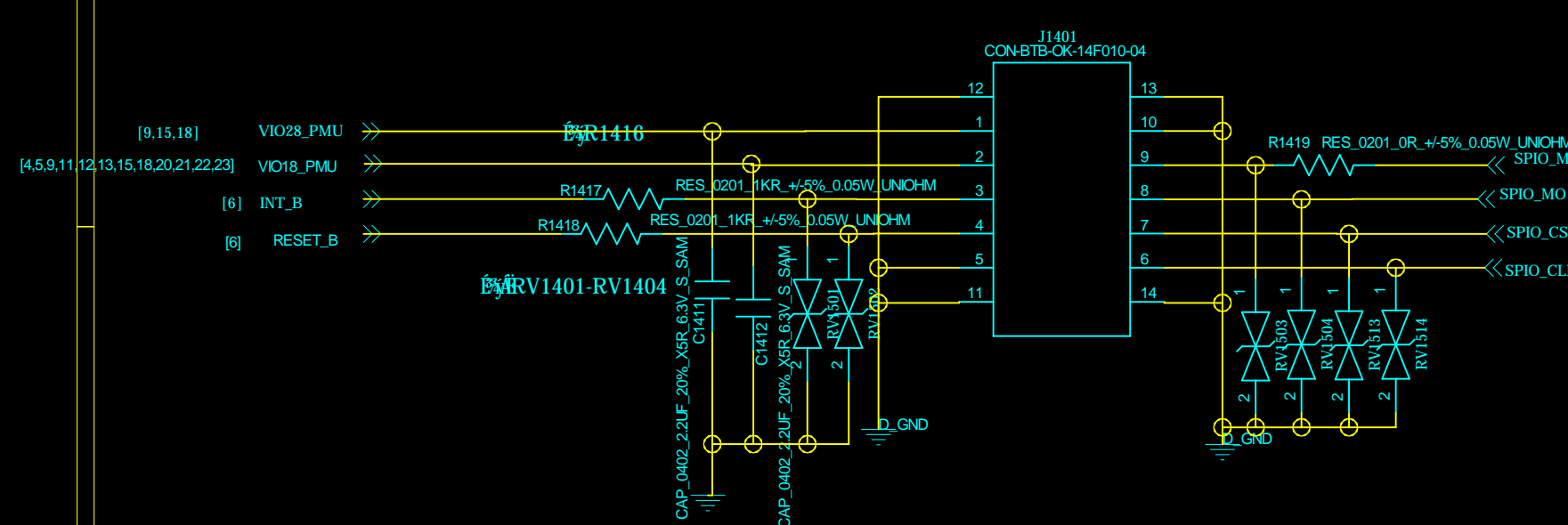
Accelerometer&GYRO: ICM-20600



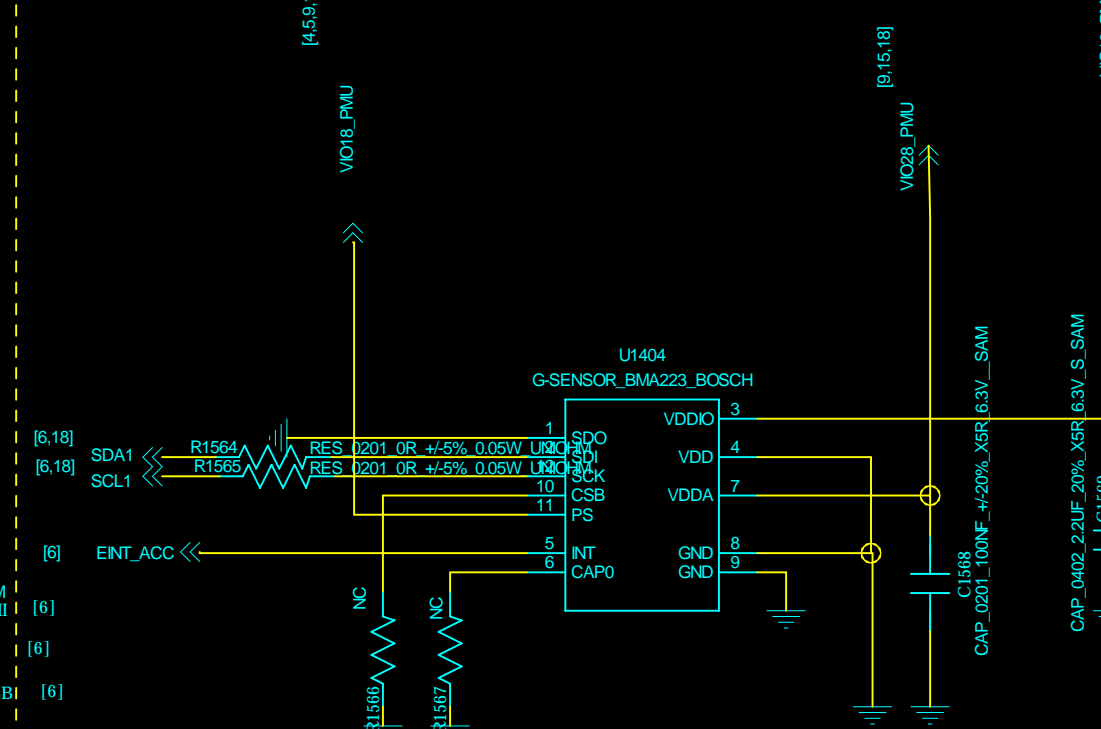
ALS & PS Sensor



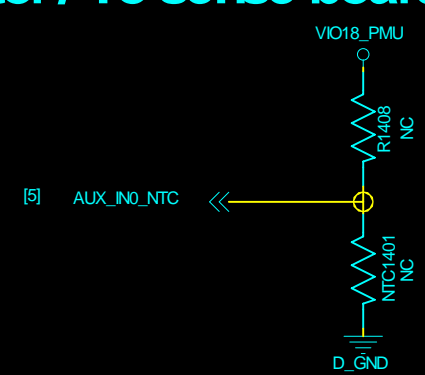
FINGER FPC



G Sensor

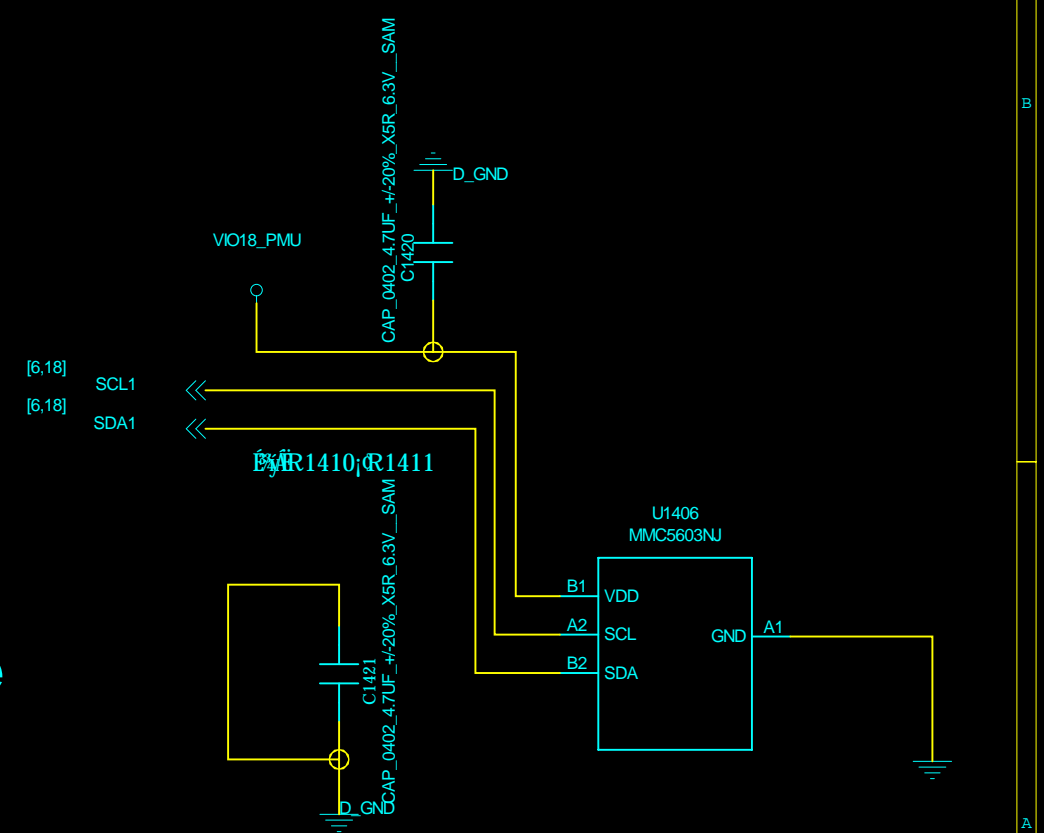


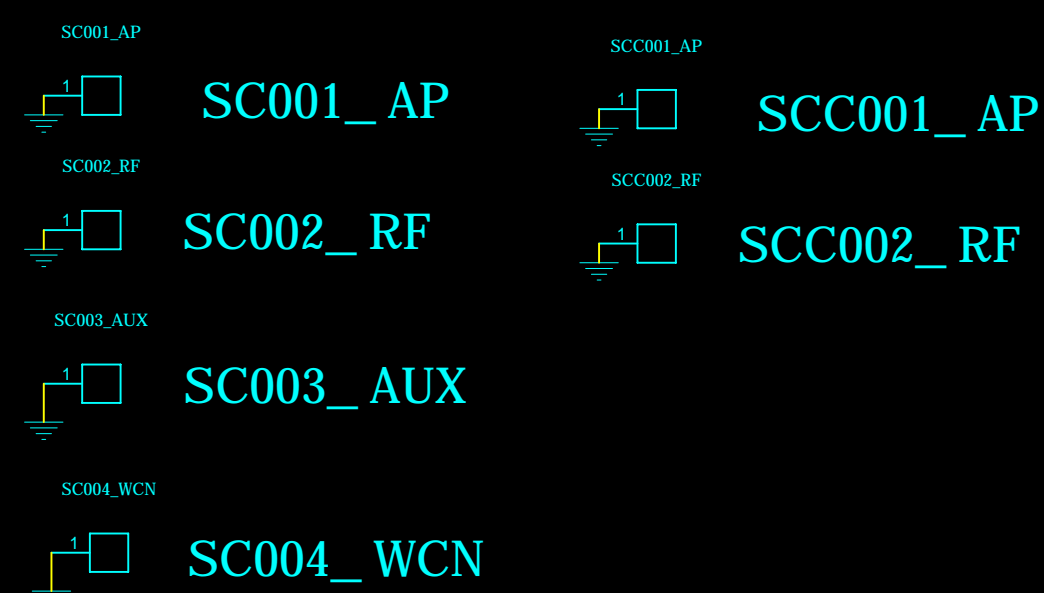
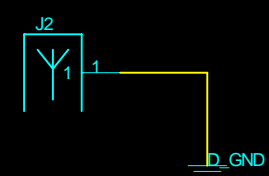
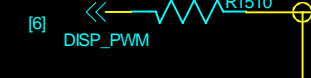
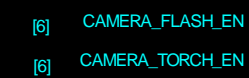
Thermistor / To sense board level temperature



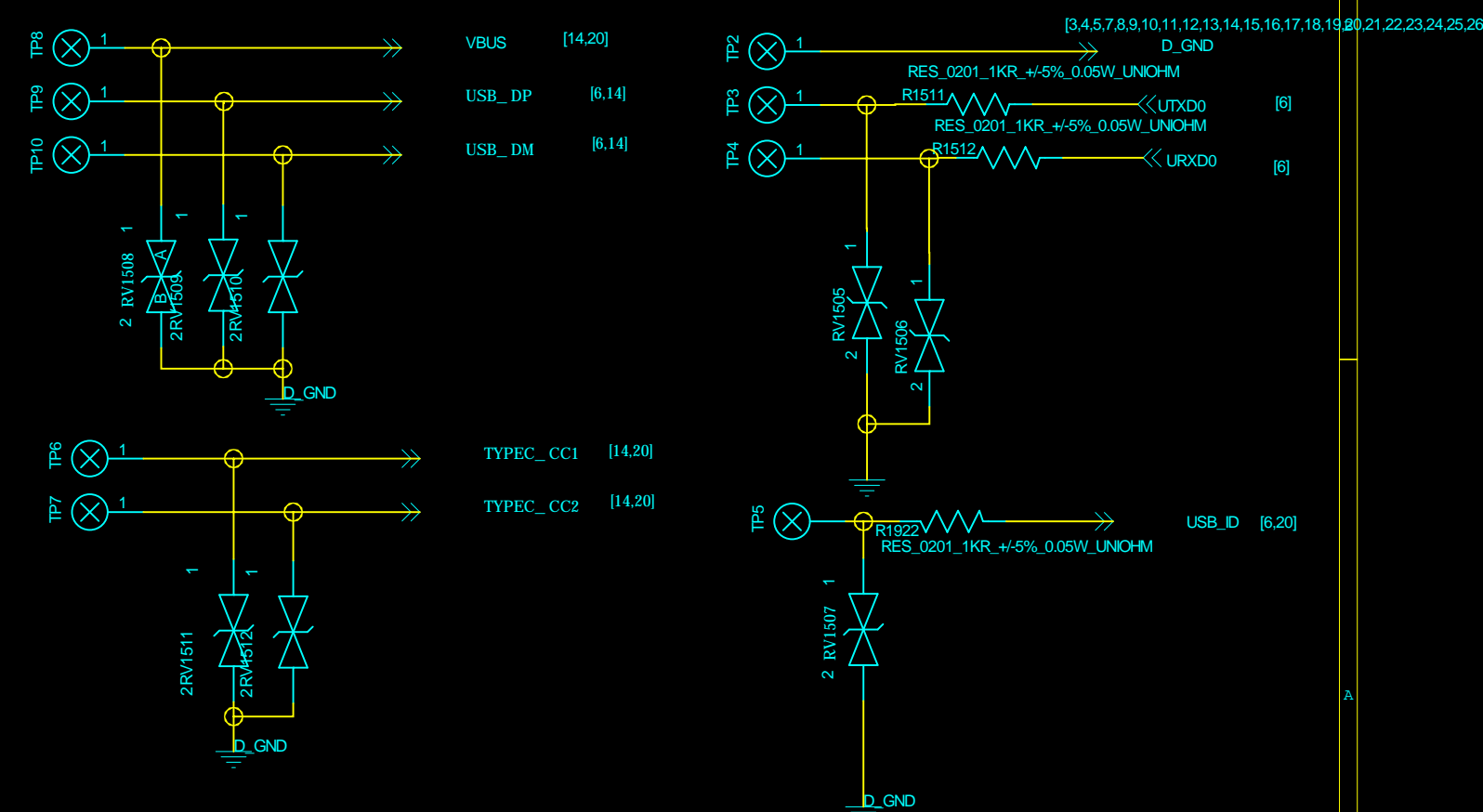
Distance to AP is 5~7mm and away from other heat resource 10mm~12mm

M Sensor





TESTPOINT



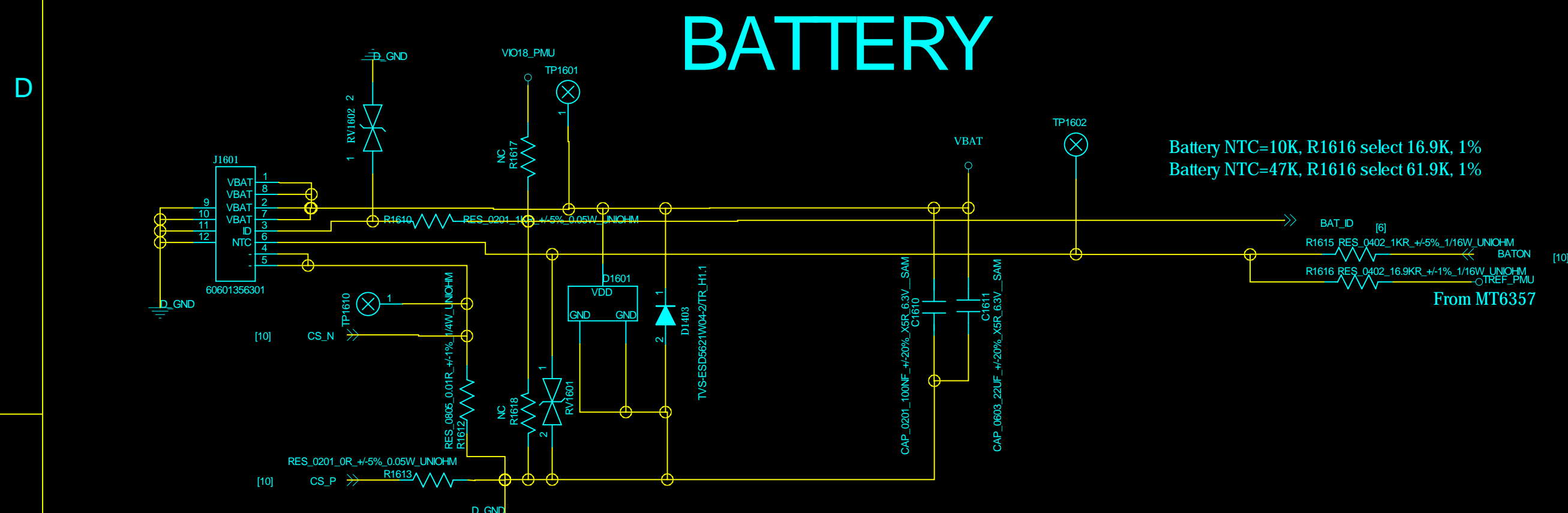
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D

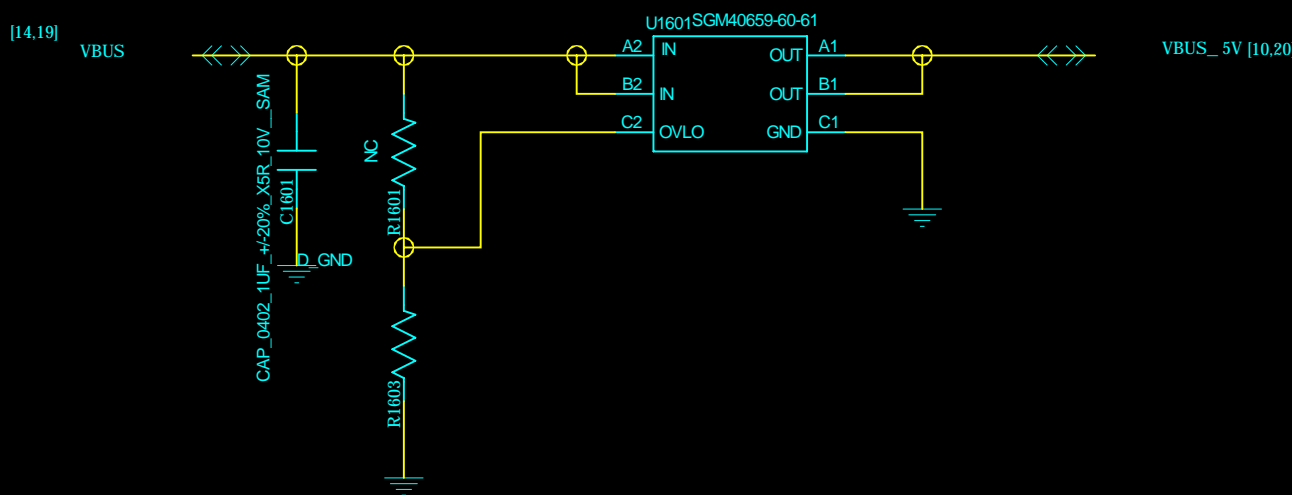
C

B

A

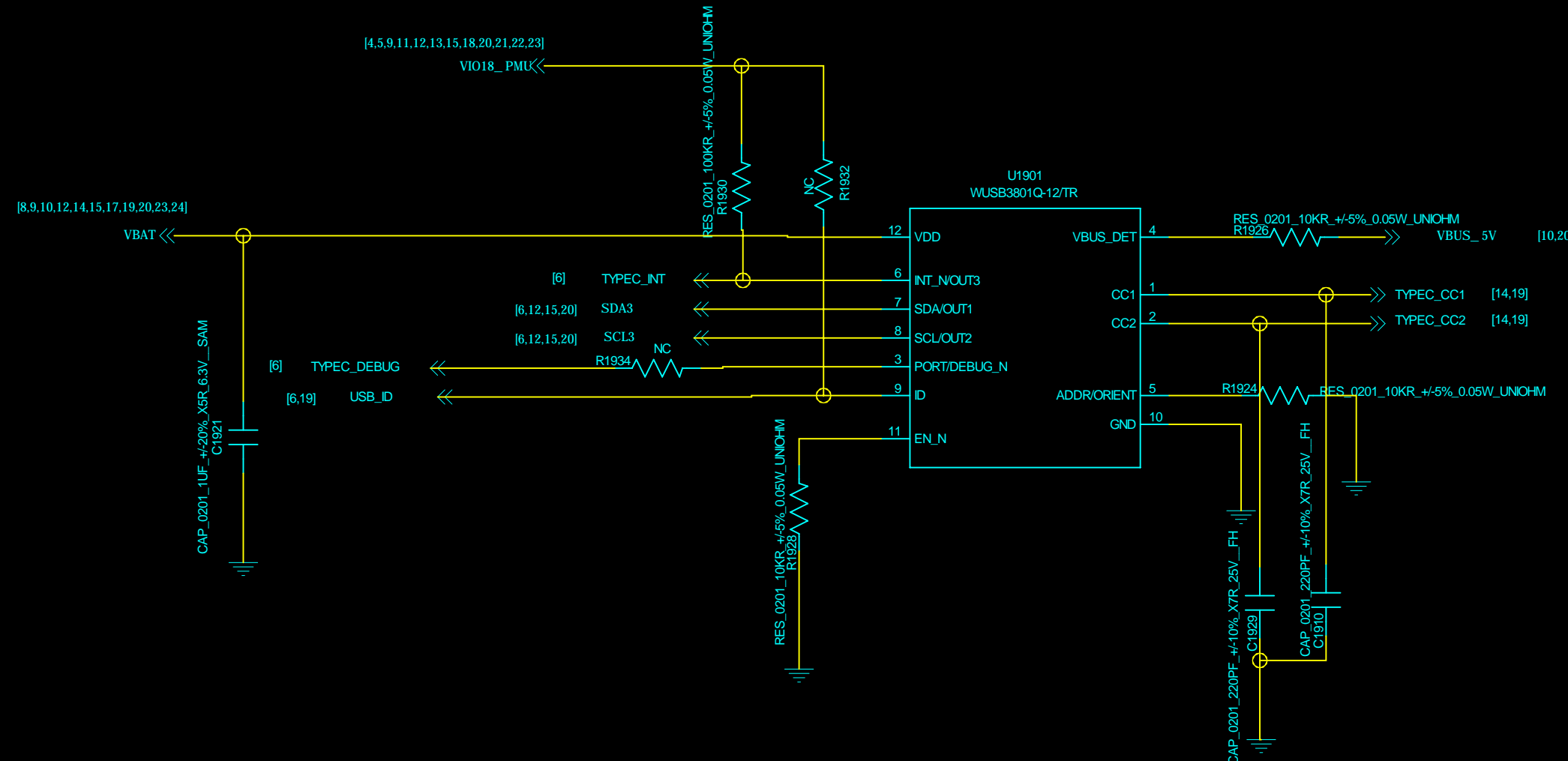
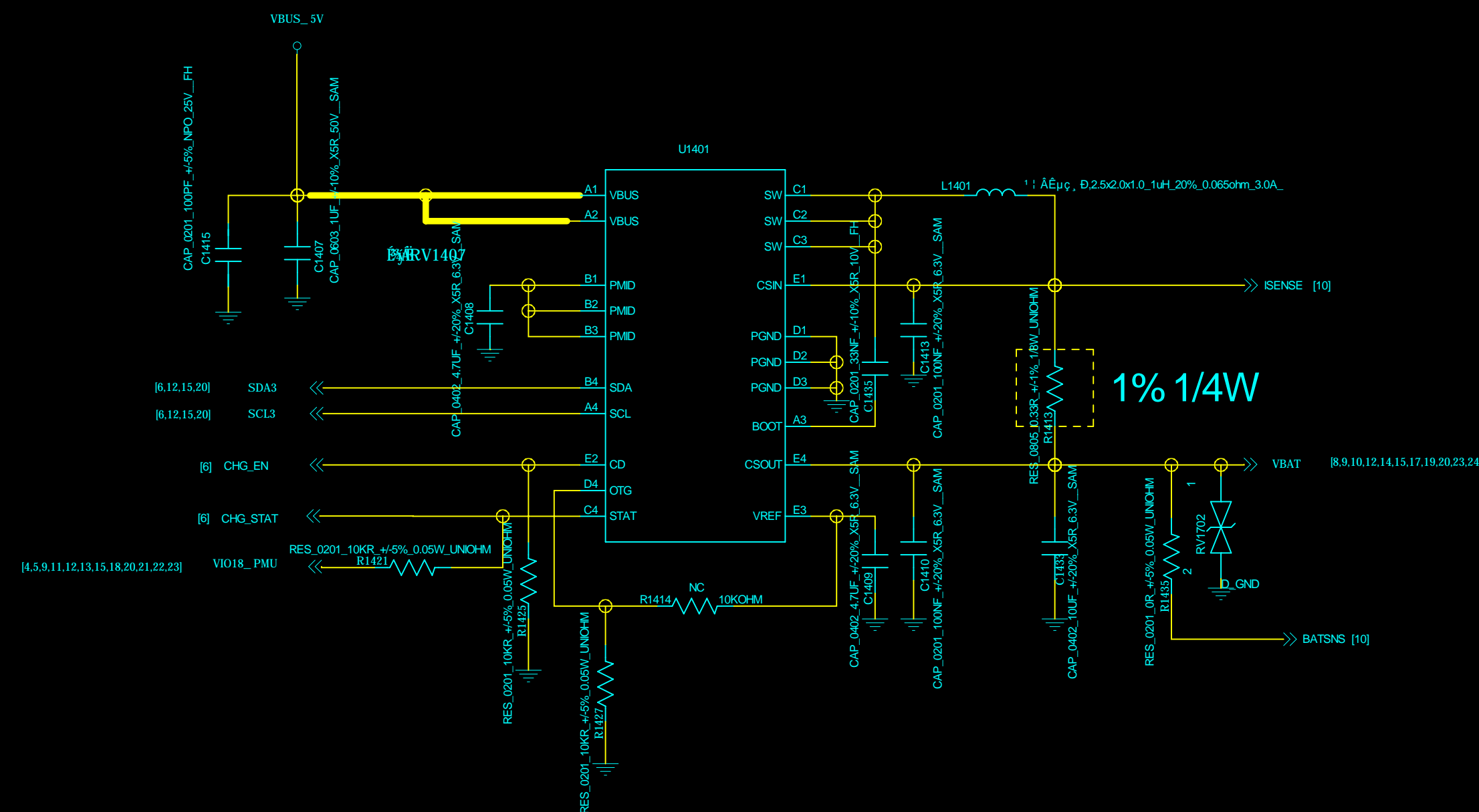


OVP



SGM41511&HL7026 CHARGER WITH POWER PATH

should afford 1.45A current



D

C

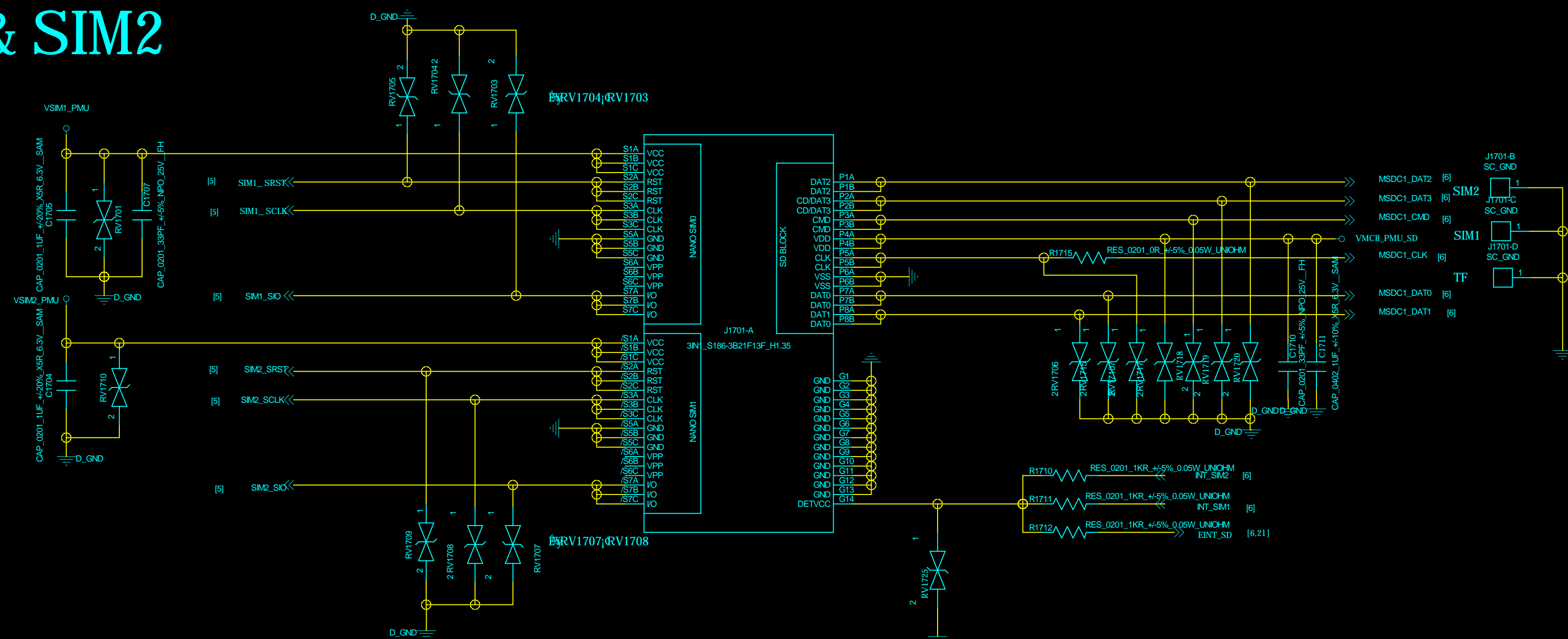
B

A

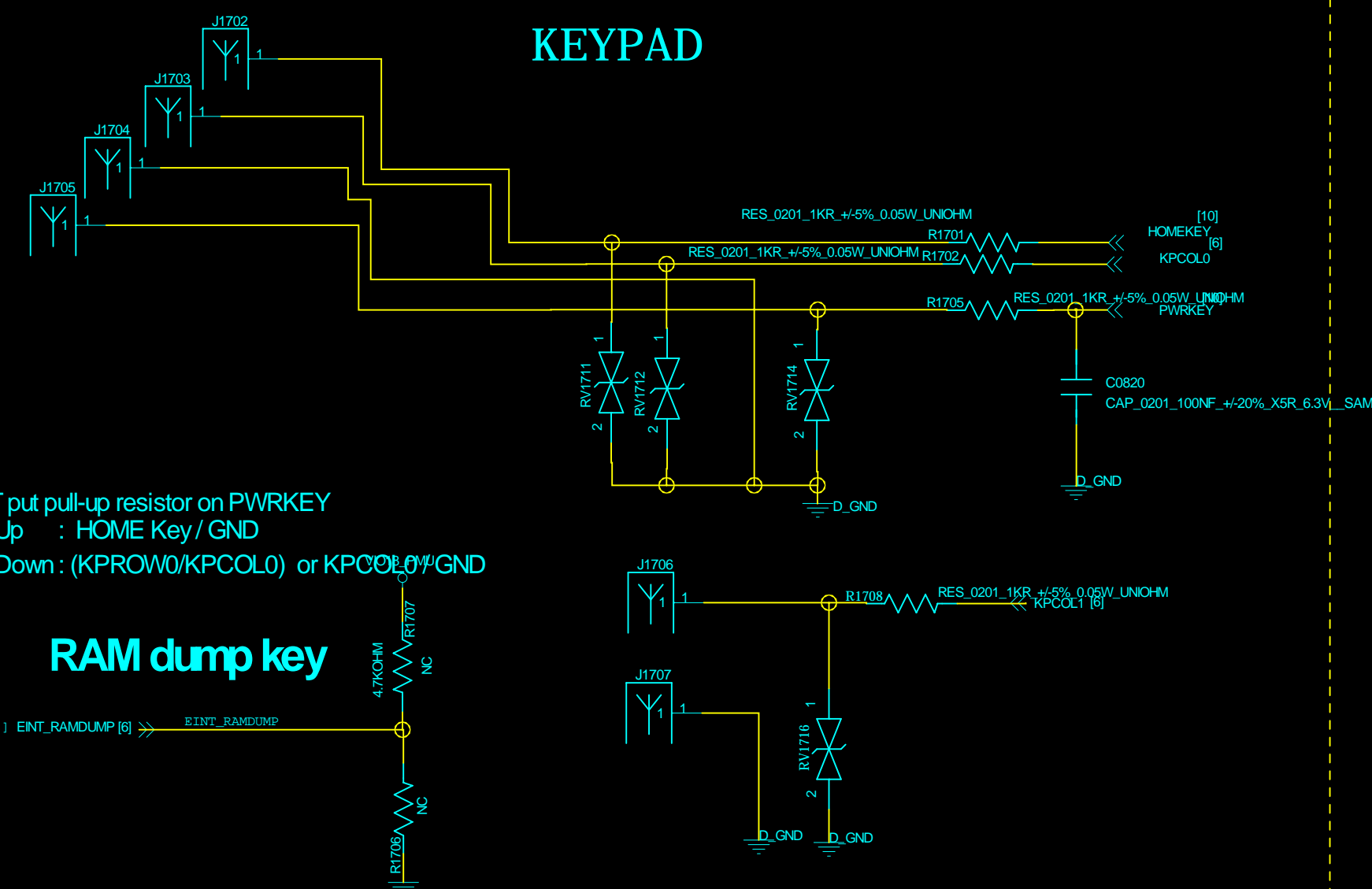
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SHEET: 60 29			

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CHECKED: <Checked By>	DATED: <Checked Date>
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RELEASED: <Released By>	DATED: <Release Date>

SIM1 & SIM2

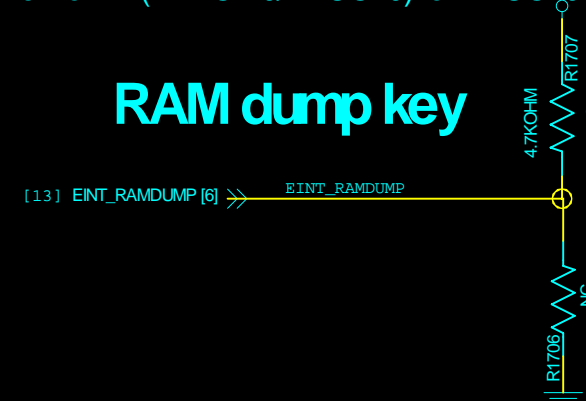


KEYPAD



DO NOT put pull-up resistor on PWRKEY
Volume Up : HOME Key / GND
Volume Down: (KPROW0/KPCOL0) or KPCOL0 / GND

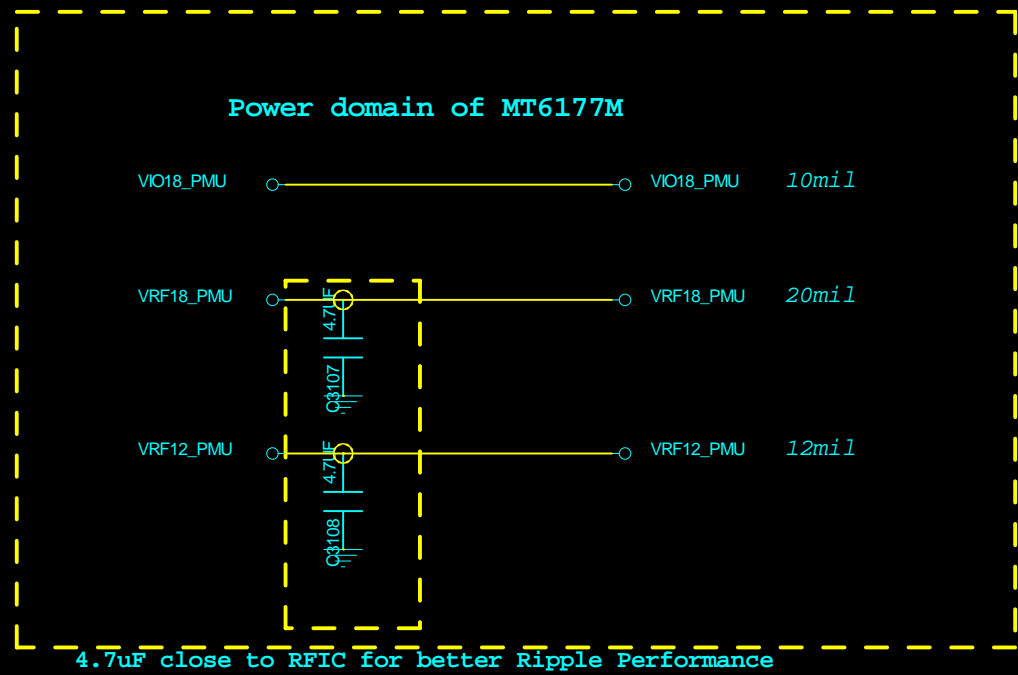
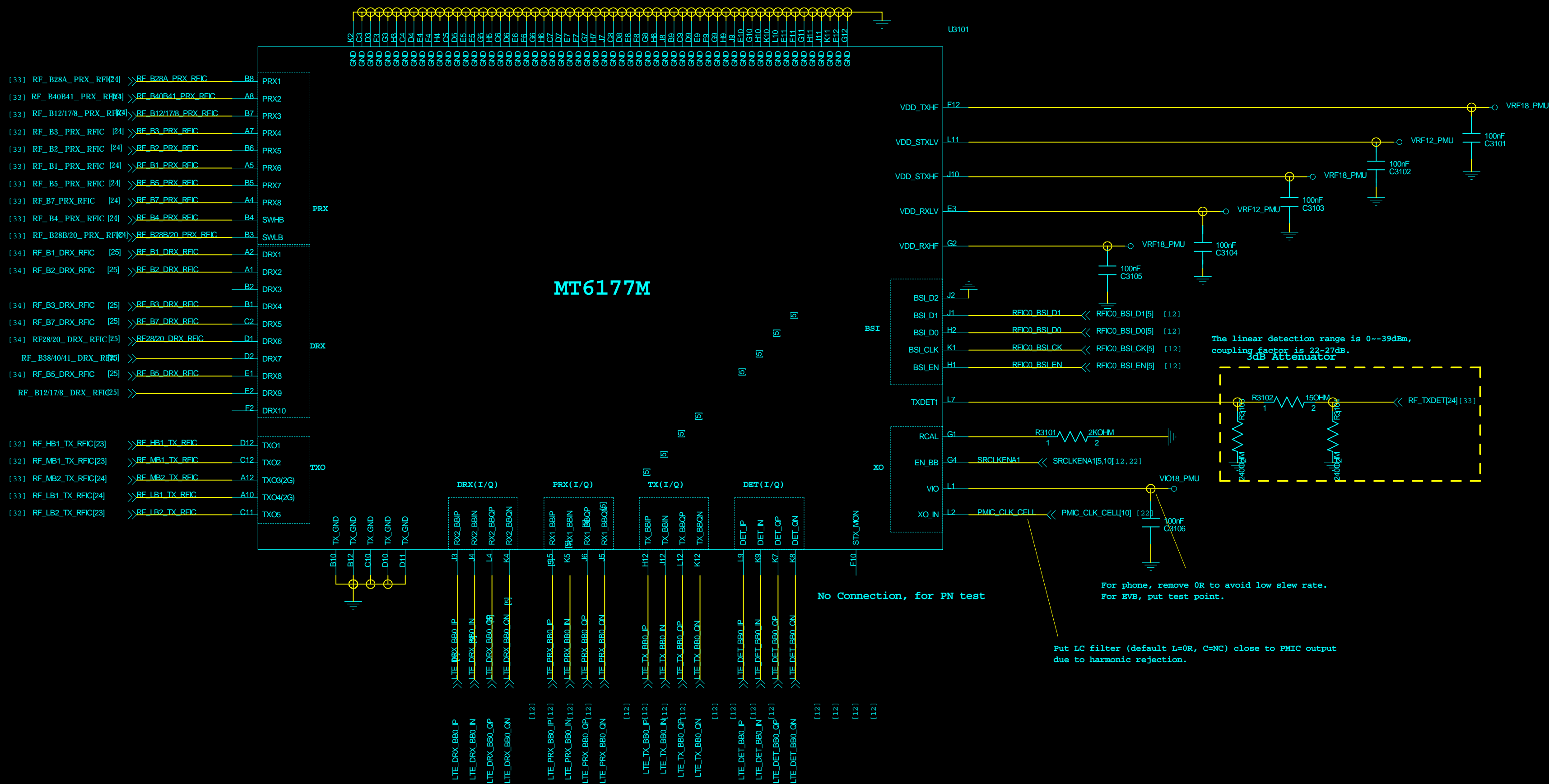
RAM dump key



Schematic design notice of "46_MEMORY_SD Card" page.

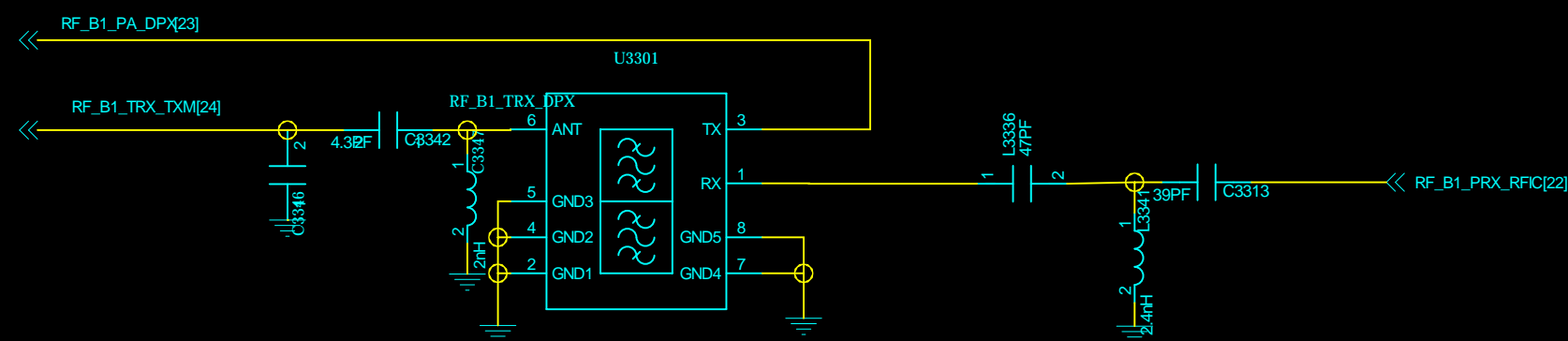
Note 46-1: For better ESD performance, please select suitable components for system protection.

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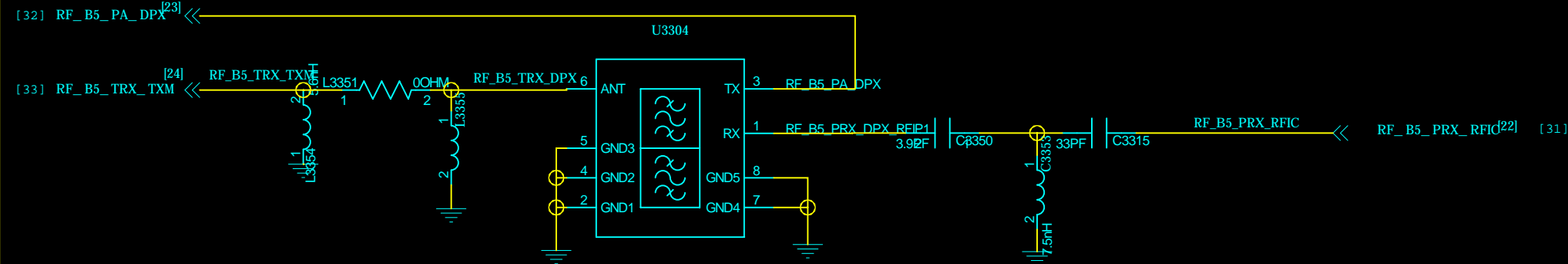


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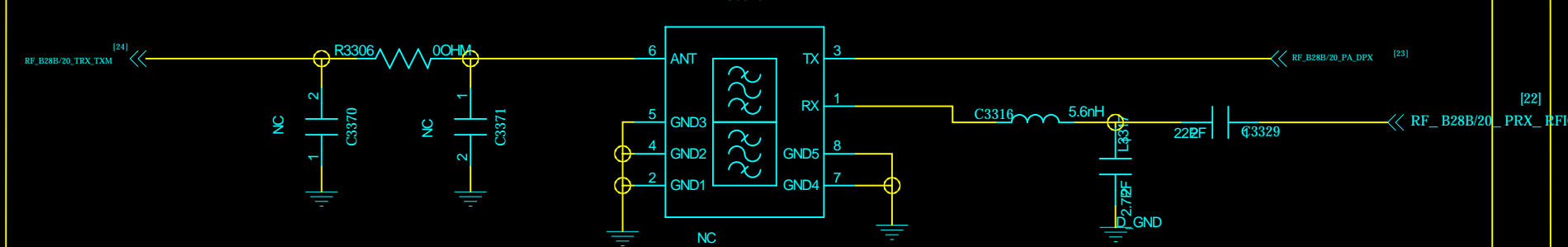
Primary-ANT



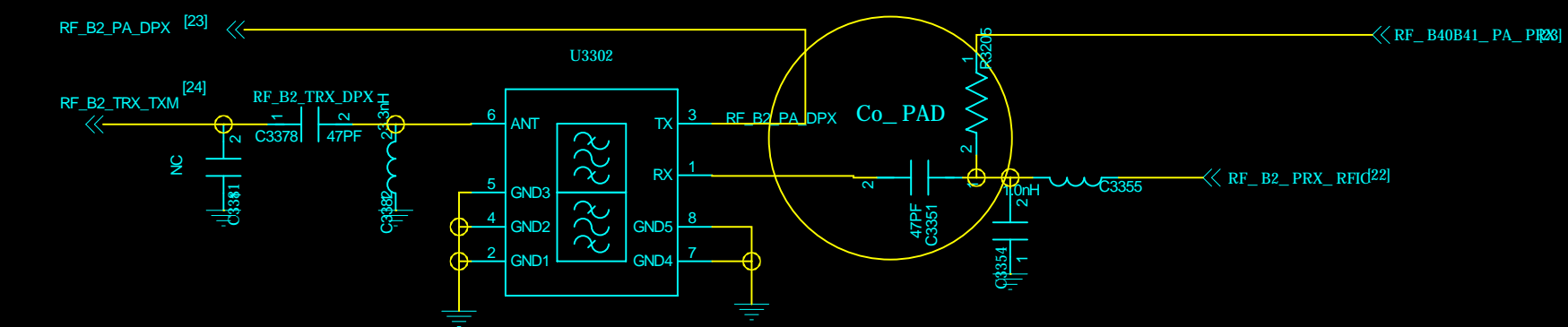
B5 TRX



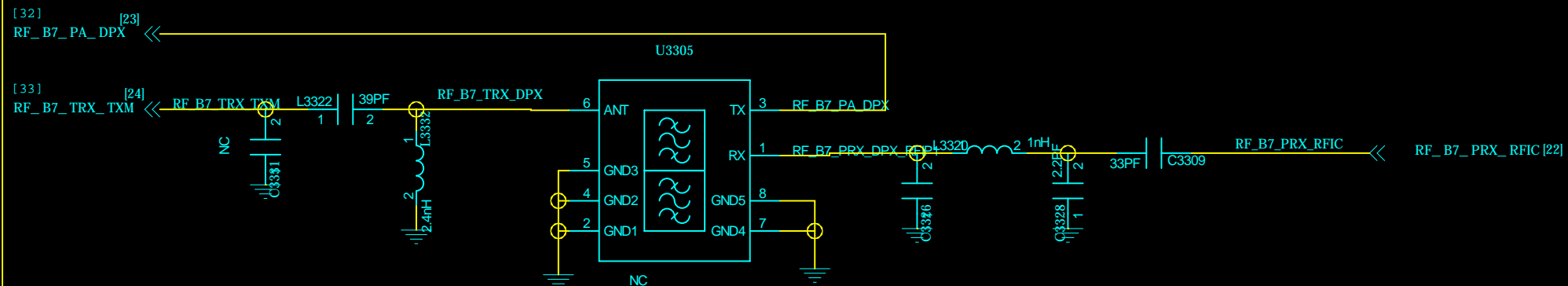
B28B/20 TRX



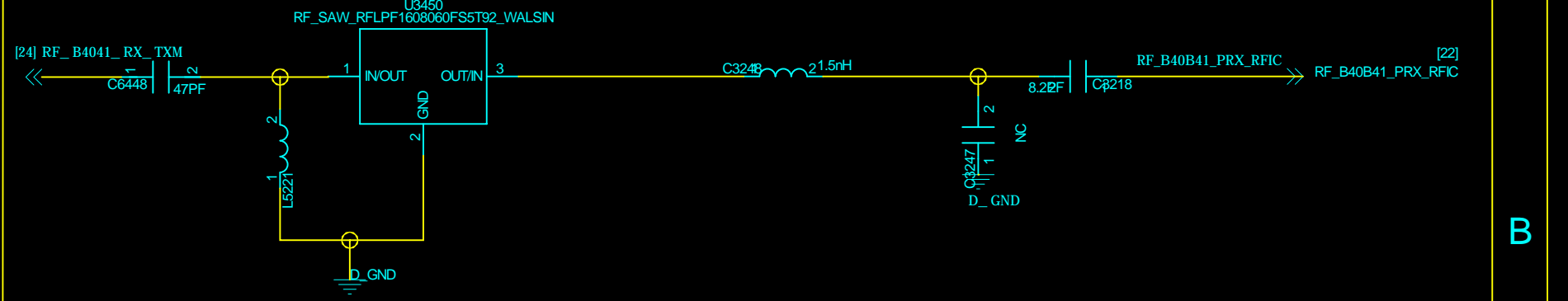
B2 TRX



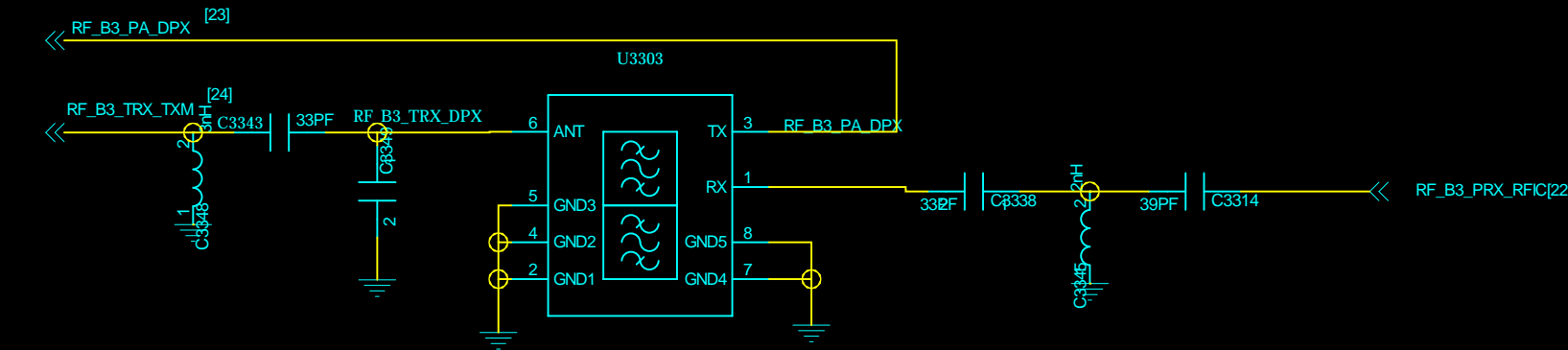
B7 TRX



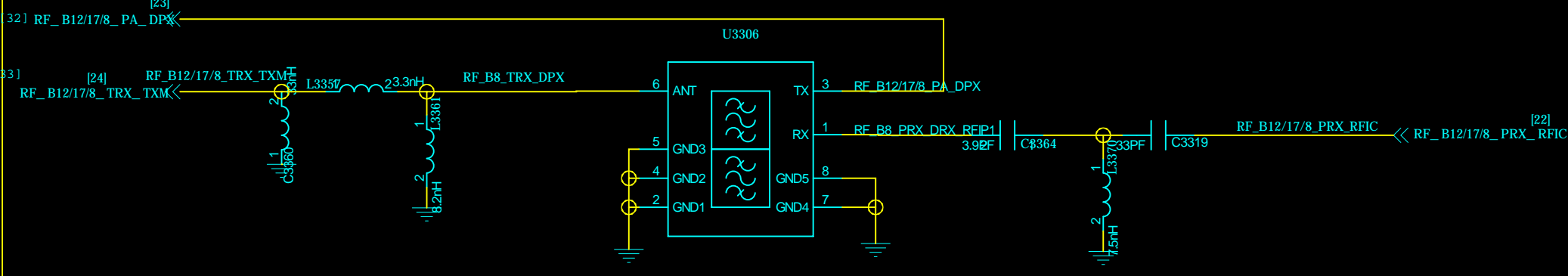
B4041 RX



B3 TRX



B12/17/8 TRX

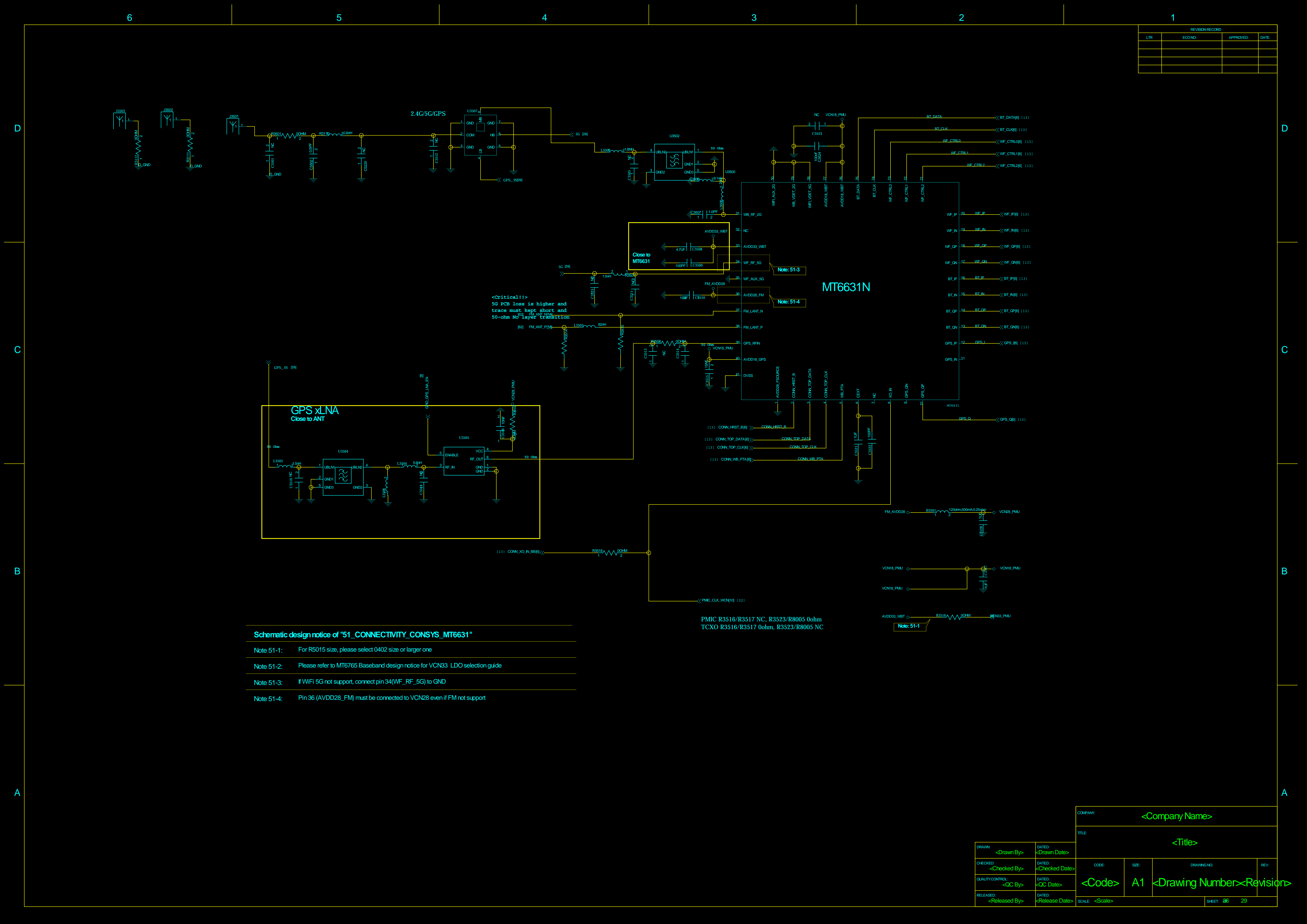


B4 TRX

B28A TRX

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RELEASED: <Released By>	DATED: <Released Date>	SCALE: <Scale>			SHEET: 04 29



Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"	
Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin.36 (AVDD28_FM) must be connected to VCN28 even if FM not support

PMIC R3516/R3517 NC, R3523/R8005 0ohm
TCXO R3516/R3517 0ohm, R3523/R8005 NC

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE

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