

Memory

A collection of storage cells to allow users to read and write information.

Stores information in binary form of a group of bits called **words**.

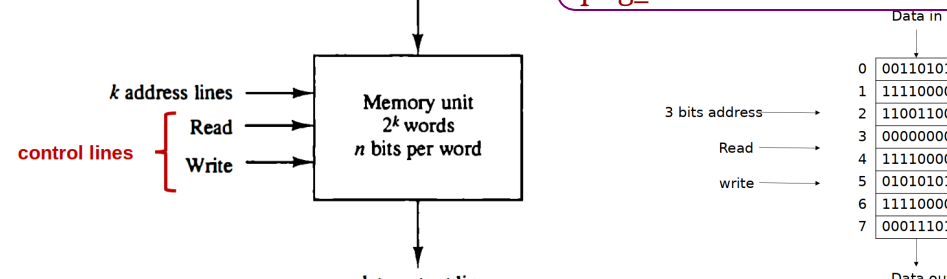
A word can represent a number, a character, an instruction...

Memory capacities is computed using the amount of **bytes** they can hold.

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2^k Locations to store words in

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RAM

Random Access Memory

Main memory of any computer system

Allows access to any word in the memory with the **same** time delay, unlike magnetic disks (hard disks) for example.

Volatile: as long as power is switched off, RAM loses the data inside.

To access a specific word, we must have its **address** (location) in the memory, hence we need **address lines**.

address line = where are you in the ram

Read-only memory

Memory unit that performs the read operation only;

Rom

it does not have a write capability.

This implies that the binary information stored in a ROM is made permanent during the hardware production of the unit and cannot be altered by writing different words into it.

Found in BIOS chips (basic input/output system)

used to start computers, in calculators, and embedded systems.

Memory Read

To read a word from memory and transfer it to a register DR (Data register)

$$DR \leftarrow M[AR]$$

Memory Write

$$M[AR] \leftarrow DR$$

Arithmetic MacroOps

Complements

1's complement of 1010 is = 0101

2's complement of 1010 is adding 1 to its complement, so 0101+1 = 0110

How to Read a two's complement number ?

(1 2)ⁿ + (Decimal of the remaining n bits)

read 1110 (-2ⁿ⁻³ + 6)

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R3 ← R1 + R2
R2 ← R1 - R2
R2 ← R2
R2 ← R2 + 1
R3 ← R1 + R2 + 1
R1 ← R1 + 1
R1 ← R1 - 1

Contents of R1 plus R2 transferred to R3
Contents of R1 minus R2 transferred to R3
Complement the contents of R2 (1's complement)
2's complement the contents of R2 (negate)
R1 plus the 2's complement of R2 (addition)
Increment the contents of R1 by one
Decrement the contents of R1 by one

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full adders

1-bit

half adders

Full adder

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Half adder

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Ripple Carry

MSB position

LSB position

Adder/Subtractor

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4-bit Arithmetic Circuit

Adder

Incrementer

Subtractor

Decrementer

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Select

Input

Output

Microoperation

0 0 0 0 B D = A + B Add

0 0 0 1 B D = A + B + 1 Add with carry

0 1 0 0 B D = A + B - 1 Subtract with borrow

0 1 1 0 B D = A + B - 1 Subtract

1 0 0 0 D = A Transfer A

1 0 1 0 D = A + 1 Increment A

1 1 0 0 D = A - 1 Decrement A

1 1 1 0 D = A Transfer A

1 1 1 1 D = A Transfer A

Logic Microops

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F₀ = 0

F₁ = xy

F₂ = xy'

F₃ = x

F₄ = x'y

F₅ = y

F₆ = x ⊕ y

F₇ = x + y

F ← 0

F ← A ∧ B

F ← A ∧ B̄

F ← A

F ← Ā ∧ B

F ← Ā

F ← B

F ← A ⊕ B

F ← A ∨ B

Clear

AND

Transfer A

Transfer B

Exclusive-OR

OR

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F₈ = (x + y)'

F₉ = (x ⊕ y)'

F₁₀ = y'

F₁₁ = x + y'

F₁₂ = x'

F₁₃ = x' + y

F₁₄ = (xy)'

F₁₅ = 1

NOR

Exclusive-NOR

Complement B

Complement A

NAND

Set to all 1's

Selection and Masking operations

Selective Set

Logic OR

Complement in A when you see 1 in B

Selective Complement

Logic XOR

Set 0 in A when you see 1 in B

Selective Clear

Logic A ∧ B'

Only keep in A when you see 1 in B

Masking

Logic AND

mask first then oring

Inserting

Example

Insert value 1001 in the most significant part.

Masking

Setting

Shifting

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Right Shift

Left Shift

the serial input is always a "0" either from left or right.

Logical Shift

Symbol: shl for shift left and shr for shift right

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R1 ← shl R1

R2 ← shr R2

Circular Shift

rotate shift

Symbol: cil and cir

Example 00001101 cir 10000110

Arithmetic Shift

Arithmetic shift right: shift using the MSB

multiply by 2

divide by 2

Arithmetic shift left: shift using 0

There's a problem in this shift when the two MSB aren't the same

the problem is that the sign is reversed

When they are the same no problem arises

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V_n = R_{n-1} ⊕ R_{n-2}

if the XOR = 1 there's a problem

Implementation

Sequential using flip flops

using Muxes

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Combinational

A is the input

H is the output

Select line decides whether to shift up or down.

Two serial inputs (left or right) # controlled by another control unit depending on what category of shift we want)

Try:

A = 0100

Shift left logical

Select must be set to '1' then

the ALU

combining all circuits in one

Arithmetic Logic Unit

ALU is a vital part inside any processor (CPU) and is responsible of carrying all computations.

ALU inputs should be connected to the registers as well as the ALU output should be also connected to the registers to write the results back.

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One stage Arithmetic Circuit

One stage Logic Circuit

Select

0 4 x 1 MUX

1

2

3

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1-bit stage for addition/subtraction, increment/decrement

from slide 4

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1-bit stage shifter

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1-bit stage logic operations

You need to replicate this stage n times for n-bit ALU.

Of course a special care has to be taken for first and last stages for the Cin, cout, and the shift elements.

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Operation select						Operation	Function
S ₃	S ₂	S ₁	S ₀	C _{in}	C _{out}		
0	0	0	0	0	0	F = A	Transfer A
0	0	0	0	1	0	F = A + 1	Increment A
0	0	0	1	0	0	F = A + B	Addition
0	0	0	1	1	0	F = A + B + 1	Add with carry
0	0	1	0	0	0	F = A + B̄	Subtraction with borrow
0	0	1	0	1	0	F = A + B̄ + 1	Subtraction
0	0	1	1	0	0	F = A - 1	Decrement A
0	0	1	1	1	0	F = A	Transfer A
0	1	0	0	×	×	F = A ∧ B	AND
0	1	0	1	×	×	F = A ∨ B	OR
0	1	1	0	×	×	F = A ⊕ B	XOR
0	1	1	1	×	×	F = Ā	Complement A
1	0	×	×	×	×	F = shr A	Shift right A into F
1	1	×	×	×	×	F = shl A	Shift left A into F