Four-Quadrant CMOS Analog Multiplier

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***Abstract*—A Four Quadrant CMOS Analog Multiplier based on the Gilbert Gain Cell is presented. The input signal range has been increased by employing attenuators to reduce the signal amplitude given to the Gilbert Cell Circuit.**

I. CIRCUIT DETAILS

Bipolar version of the Gilbert cell [1] has been successfully used for many years in the form of analog multipliers. Replacing the Bipolar Junction Transistors with MOSFETs heavily limits the range of the differential input signals. This is because the output current of the MOS differential pair depends non-linearly on the tail bias current and the input signal. The MOS analog multiplier is however an extremely useful circuit in integrated VLSI systems. In this paper an attempt has been made to increase the input range of the signal swing by employing attenuating stages which reduce the input signal levels before giving the input into the Gilbert cell stage.

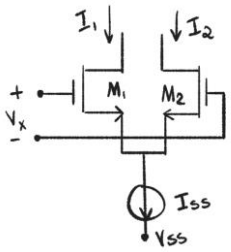

Fig. 1. NMOS Differential Pair

The differential current is given by the equation (where symbols have their usual definitions):

$$I_1 - I_2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) V_x \sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\left(\frac{W}{L}\right)} - V_x^2}$$

$$\text{FOR } |V_x| \leq \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}$$

The Gilbert cell (*Fig. 2*) uses Three of these differential pairs and two inputs to steer tail currents depending on the two inputs.

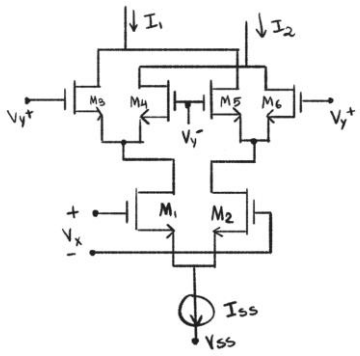

Fig. 2. MOS Gilbert Cell

II. CIRCUIT DESIGN AND WAVEFORMS

The Circuit [2] shown in *Fig. 3* has been simulated using LTSpice.

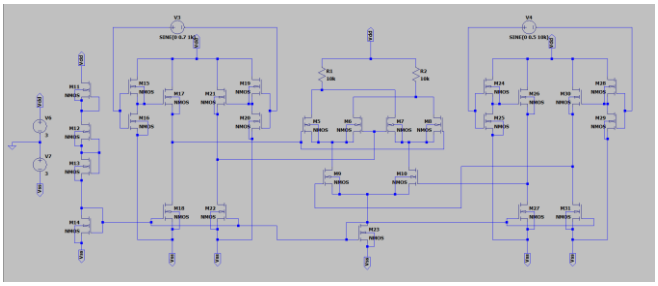

Fig. 3. Circuit Implementation in LTSpice

The DSB-SC signal obtained after simulation is shown in *Fig. 4* and the transfer characteristics of the circuit are shown in *Fig. 5*.

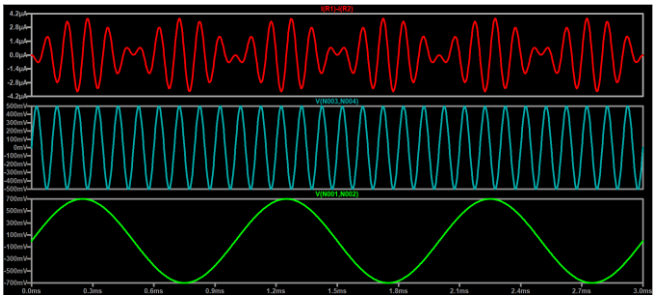

Fig. 4. Multiplication of two sine waves of different frequencies (DSBSC)

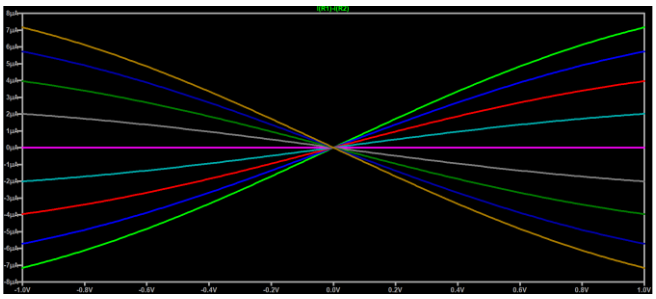

Fig. 5. Transfer characteristics of the designed MOS multiplier.

REFERENCES

[1] B. Gilbert, "A high-performance monolithic multiplier using active feedback," IEEE J. Solid-State Circuits, vol. SC-9, pp. 364-373, Dec. 1974

[2] SHI-CAI QIN ANDRANDY L. GEIGER, A +-5-V CMOS Analog Multiplier, IEEE Journal of Solid State Circuits, vol SC-22, pp.1143–1146, Dec. 1987

[3] Razavi, Behzad. 2001. *Design of analog CMOS integrated circuits*. Boston, MA: McGraw-Hill.