Manual

Camera - Control

This manual describes the operation and service for the Cam Control which implies the Double Line Cameras (DL) and the optional 4 channel Photo Diode Integrator (I).

Type

PDA(I)xx and

FFT(I)xx and

IR(I)xx

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ENV 50140
ENV 50204 / ENV 50140
ENV 50141
EN 61000-4-4

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Berlin, den 1.9.2009

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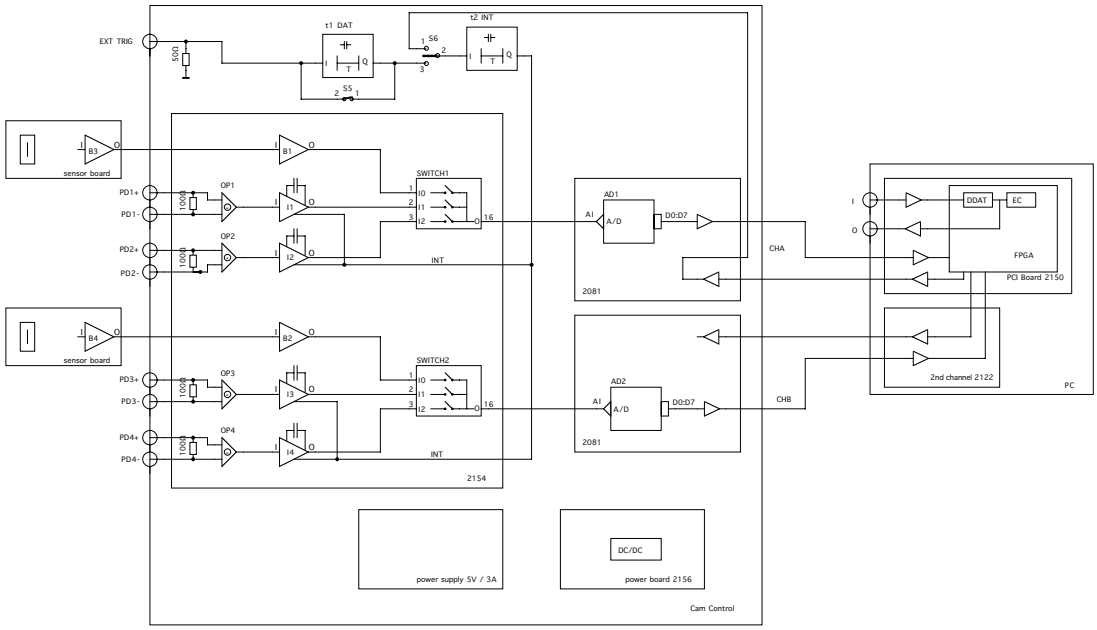
1 Overview

The Double Line Camera (DL) is intended for I/I0 Spectrometer Systems, where 2 spectres are sampled simultaneously with high repetition rates. Both lines are sampled exactly at the same time, as the lines are clocked with one master clock. The line rates can be better 1 kHz (better 1000 spectres per second): The read time is the same for 1 or 2 sensors.

The complete camera electronic and the A/D converter is mounted inside the control. So additional analog signals can be switched to the A/D converters input. The picture-1.1 shows the block diagram of the electronic.

picture-1.1: Block schematic of the Cam Control



The integrator cycle can be started with different modes. After the adjustable integration time the values of the 4 channels are hold until they are switched to the output, when all active camera pixel have been read. So these values appear as additional pixel values at the end of the data stream (see picture-2.1).

1.1 Versions

The Cam Control can be ordered with 4 external photo diode inputs. These values are inserted in the video stream at the end of the line. Here an integrator (I-version) can be used or just a simple voltage input (without hold).

The Cam Control is also available for single line systems and can be delivered with or without the integrator function.

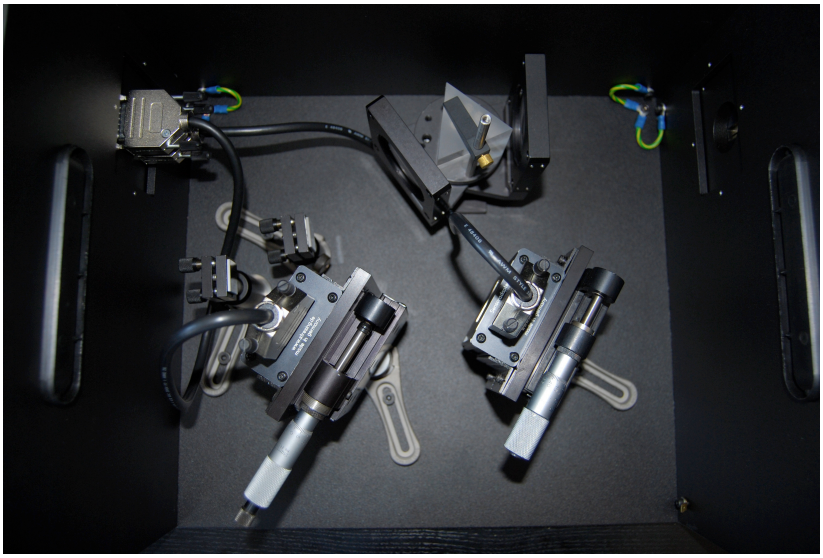
The sensor boards are different for different sensor types, as there are PDAs, FFTs (‚full frame transfer' CCDs) or IR sensors. Also switchable versions are possible, where one Camera Control can be used for vis sensor boards or in another setup for ir sensor boards.

The possible sensors are:

FFT	S7030-x
PDA	S390x
IR	G11608

picture-1.2: CamControl with IR/FFT switch and PD power supply

picture-1.3: Prism spectrometer with 2 single line sensor boards.



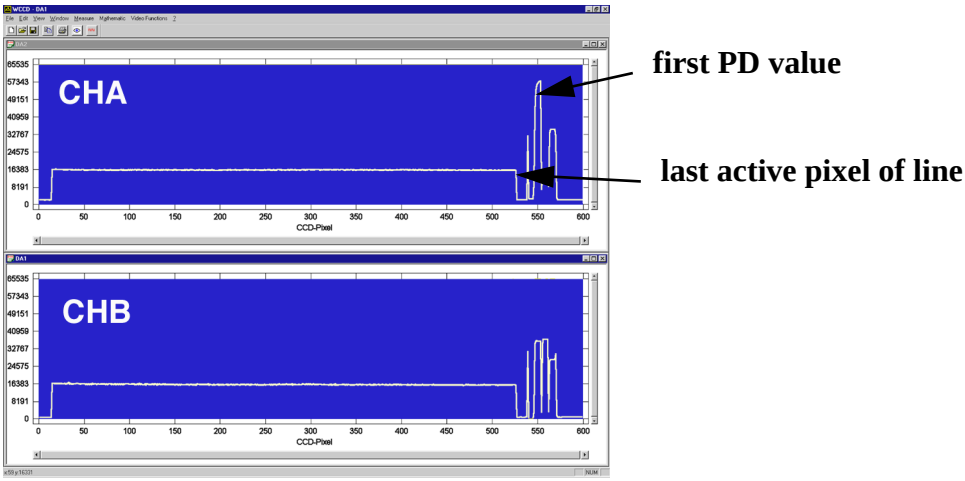
Here two laser beams are sent trough one prism (higher beam and lower beam with 30mm distance). The signals are reflected on 2 different sensor boards.

2 Software

2.1 Data Signal

The external PDA- signals occurs at the of the data array. In picture-2.1 the data stream is shown. First displayed are the values of the line camera (here pixel 20 to 532), then is a gap of non valid pixel. After that the 3 photo diode signals are shown (6 channel version) and a rest of non valid pixel values.

picture-2.1: Display of 2 channel data stream



Every PD signal consists of 8 or 16 pixel values (the A/D converter samples the integrator voltage 8 times - could vary depending on sensor type). In case of a full scale value, an asymptotic slope can be seen at the first 4 values. As the switch is not fast enough (A/D converts with 1 or 2 MHz) the first 4 values should not be taken. The last values are stable and can be used. For additional noise improvements averaging of several values is recommended.

2.2 Data Structure

As seen in picture-1.1 the control has 2 parallel working channels. These are clocked by the same clock, but have their own A/D converter and an own data path to the PCI Interface board. In the interface the 32bit PCI bus system is used in a special way: the lowest 8bit transfers the channel A with 16bit values in a low byte/high byte order. The next higher byte of the PCI bus transfers the 16bit values in a low byte/high byte order of channel B (CHB). The higher word of the PCI bus is not used. For that hardware dependant reason the data array has its special structure. In unit board @ function CallIORead these values are resorted to a standard structure, that other compilers can handle these values more easily. For a deeper understanding a look at the source code of BOARD should be taken.

2.3 WCCD Software

The software WCCD can be used to test the camera system.
The software is deeper explained in the camera manual chapter 2.
Be aware: this software has a max. repition rate which is shown in the lower window frame. For highest speed the labview examples LoopSelFF and GetRing2cam must be used.
Here is a short briefing whats different for the double line system.

2.3.1 WCCD Setup

In the setup menu (only acessable if all data windows are closed)
some flags have to be set for the right sensors:

a) the HA FFT Sensor S703x
the flag IS_FFT must be checked
FFT: lines = 64 (for 0906,1006)
FFT: vfeq = 12 (for 3µs vclk)

b) the HA PDA Sensor S390x
the flag IS_PDA must be checked
FFT: lines = 0
FFT: vfeq = don‘t care

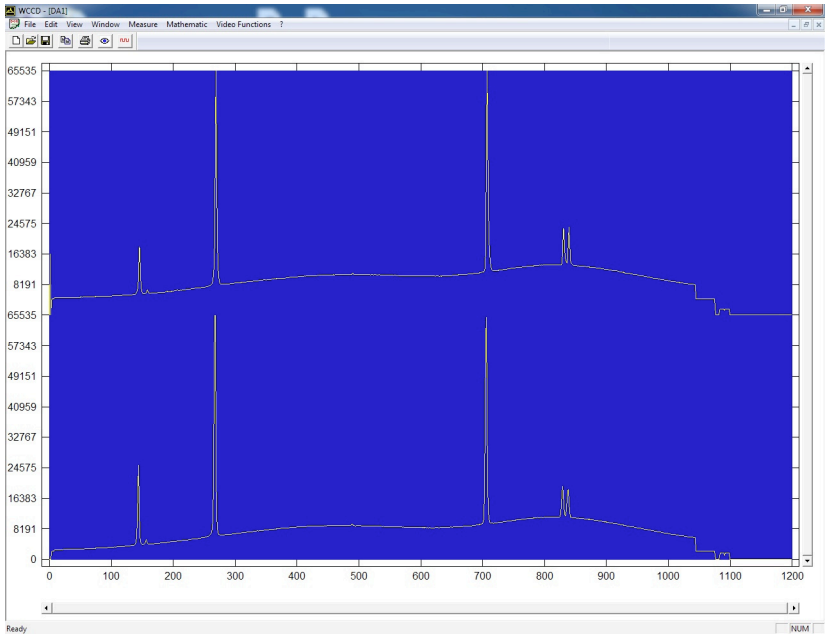
c) the HA IR Sensor G11608
same setting as b) PDA

c) the HA IR Sensor G920x
same setting as b) PDA
WCCD must be especially compiled with the flags
_HA_IR = TRUE
_HA_IRSingleCH=TRUE if 256 pixel sensor
_RESORT=TRUE

2.3.2 WCCD feature

in the view setup menu
when the button „2 cams simultan“ is checked, both camera signals are displayed in one window DA1.
If the button is not checked, DA1 can display camera1 data and DA2 the camera2 data.
It is not possible to refresh the display for both cameras at once.

picture-2.2: WCCD with double line signal



2.4 Labview Setup

To adopt the software to the different sensor types and the Double Line System, some flags and sub vis must be set accordingly. The DLL had to be compiled with the Flag _HWCH2=TRUE (see in propertys: 2cam version).

a) the HA FFT Sensor S703x
the sub vi IS_FFT must be called
and the vclk register has to be set to
lines = 64 (for 0906,1006)
vfeq = 12 (for 3µs vclk)

b) the HA PDA Sensor S390x
the sub vi IS_PDA must be called
and the vclk register has to be set to
lines = 0
vfeq = don‘t care

c) the HA IR Sensor G11608
same setting as b) PDA

c) the HA IR Sensor G920x
same setting as b) PDA
and the DLL must be especially compiled with the flags
_HA_IR = TRUE
_HA_IRSingleCH=TRUE if 256 pixel sensor
_RESORT=TRUE

2.5 Labview Examples

There are 2 main examples to show the calls of the DLL.

GetRing2cam

GETRing2cam shows how to read 2 cameras parallel with a background thread. The main read thread reads the FIFO data to main Ram. This part is executed in higher priority. The display thread runs with normal priority and displays one of the last scans, which was copied by the main thread to an additional display buffer if it was requested by Flag FetchActLine This Flag must be set once by calling DLLStartFetchRingBuf to start the cycle. With a 2nd Flag: DispBufValid both threads are syncronized. These Flags are global in the DLL (BOARD.C).
In the call of SRingStartThread the priority is set to 15 - thats standard max. priority. For high speed cameras and heavy computing systems this value could be set to a max. val. of 31(timecritical). In that case one core is exclusively used.
this example uses just one memory array for both lines(length=1 line) with data sorted as: word array CHA word array CHB resort of hardware data is done in BOARD.C -> CallIORead resort of arrays is done in the read loop of labview.
also implemented is a ring buffer of size RingBufDepth=20 Could be used much bigger if needed. Here it is used for demonstration only.

LoopSelFF

LoopselFF implements a very constant measure loop outside labview reads a complete block of nos scans during block read, the thread is highest only for single core systems -> should run modal and disable mouse if needed: set _PS2KEYBOARD TRUE and recompile
after read the slider can select the scan which is displayed first hit run, then hit arm/clear and then read. For a new block of scans press stop then arm and then read again.

for more infos and comments, please have a look to the DLL sources LWLSCDLL

3 Electronics

The Cam Control can run up to 2 camera boards and 4 photo diodes. The power supply is also implemented here. As seen in picture-1.1 there are 2 inputs possible for the external trigger input. These are explained deeper in chapter-3.3.

3.1 Double Line (DL) Function

The DL control has 2 complete channels with 2 parallel working A/D converter. Here 2 sensors can be sampled absolutely parallel in high speed. So an easy way of simultaneous reading is accomplished, where the signals can be further calculated afterwards (i.e.: divided for I/I0 measurements). The sensors can be located close together behind one spectrometer (if they have a small case that they fit there) or they can be located behind 2 separated spectrometers (if their case is too big). Usually the distance between the 2 spectra may not be more then 10mm.

3.1.1 Double Line Board

The 2 sensors can be located on one double line sensor board as shown in picture-3.1 mounted behind one spectrometer ().
Advantage: both rays use the same optical components.

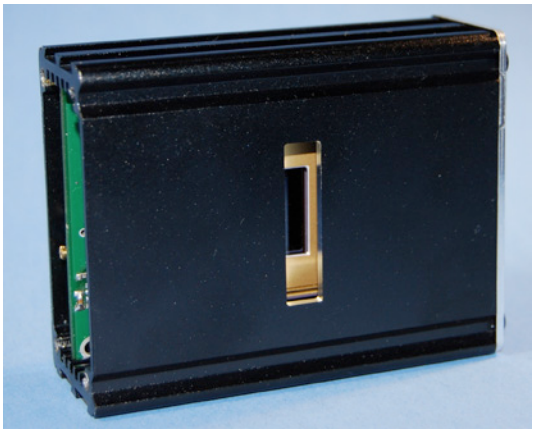
picture-3.1: Double Line Sensor

picture-3.2: Setup with one Spectrometer

3.1.2 Two separated Single Line Boards

It is also possible to mount 2 single line sensor boards (picture-3.3) behind 2 separated spectrometers, if the case of the sensor is too big to place them beneath each other.

picture-3.3: Single Line Sensor Board



picture-3.4: Setup with two Spectrometer

here two Jobin-Yvon spectrometers are shown with standard cameras, but they can be used with two sensor boards and one CamControl as well. If cooled cameras are needed, the CamControl cannot be used. Here only two separate cooled cameras can be used.

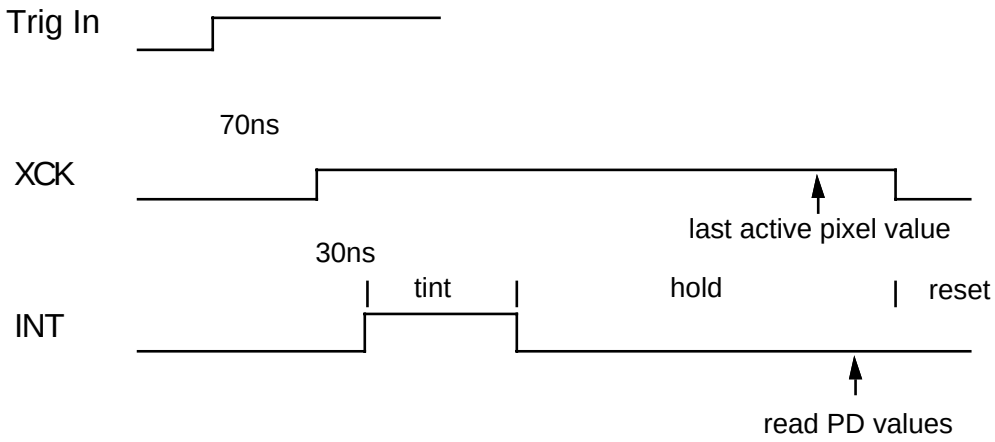
3.2 Photo Diode Integrator I- Function

The Camera Control can be equipped with 4 additional channels for external photo diodes. Every channel has an own integrator which is started at the beginning of the read sequence. The 4 integrated signals are held and switched to the data stream at the end of the read sequence after the sensor line was clocked out.

3.2.1 Integrator Timing

The Cam Control has an trigger input to start the integrate function with a very short and exact analog delay.

picture-3.5: Integrator Timing



The duration for the integration tint of the photo diode signals can be set with P5 (picture-5.4) of the Cam Control (default = 20µs). P6 can insert an additional DAT (delay after trigger) if S5 is ON.

When tint goes low, the values are hold until they are switched to the A/D converter after the last active pixel of the sensor was transferred (usually after pixel*hclk, i.e. 600*1µs = 600µs). When XCK goes low the integrators capacitor is hold reset until the next trigger occurs.
The signals XCK and INT can be monitored by the BNC plugs on the rear.

3.2.2 Integrator Calibration

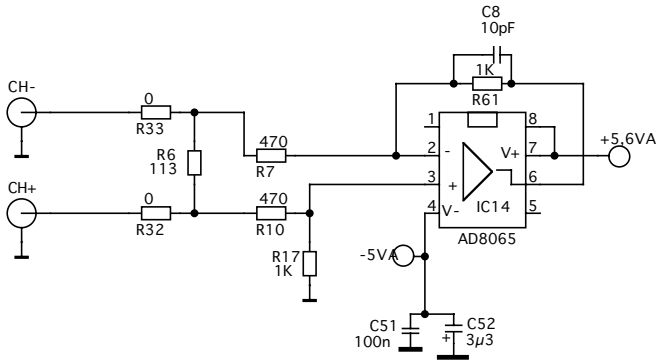
The full scale of the integrator is aligned for an input signal of 2V and tint= 20µs.

Alignment:
Apply a 2V constant Voltage at the + Input and connect - Input to GND (=case).
The BNC PD plug on the rear should now show a constant 4V signal.
Adjust int timer (P5 on picture-5.4) to 20µs (control with the int BNC on the rear).
Now P10, P11, P12 and P13 are adjusted for maximum signal gain of the PD values (picture-2.1). The zero values are adjusted by P3 and P4 as a group, or by the front panel potentiometers individual. After changing the gain, the zero values must be realigned again.

3.2.3 Photo Diode Integrator Input

The 4 channels use differential signaling for better noise immunity. For ease of use standard BNC cables are used. Every signal has a pair of cables which should be twisted around each other and **must have the same length**! The input resistor is 100Ω.

picture-3.6: PD Input schematic



The standard input voltage range is 2,5V±1V. This signal is amplificated before it connects to the integrator. A single ended output of the integrator input signal can easily be monitored on an oscilloscope with the PD1..4 BNC plugs on the rear. Here a 4V span shows that the signal is not overdriven (internal amplification = *2).

If needed the channel can also be made unidirectional by connecting the PD- input to GND. The input resistor is still 100 Ω in that case. For correct 50Ω input, a parallel resistor of 100Ω should be connected parallel to the +input.

The low resistive input is not intended for direct use of a photo diode. Here an additional amplifier must be used (see chapter-4.1).
If an own PD amplifier is used, the signal must be adopted, so that the PD output monitors a 0 to 4V maximum signal (0..2V on 50Ω). The peak width maximum is about 25µs (10µs for a square wave signal) which saturates the integrator. If the laser pulse is shorter, the signal should be stretched (Capacitor parallel to the photo diode).

3.3 Trigger function

The Cam Control can be triggered in 3 different modes.
Default mode is the internal mode. The analog delay uses 2 monoflops which are build into the Cam Control (ADAT=P6 and INT=P5). The digital delay trigger uses 2 registers of the PCI Interface (DDAT= delay after trigger and EC= exposure control). The internal mode is for free running without using additional delays.
The setup of the trigger modes is different and explained in the following chapters.

Inside the Cam Control are 2 switches for choosing some options (see picture-5.1).

SW2*-S5 ON:	analog DAT on (here is a min delay of 700ns)
SW2*-S5 OFF:	analog DAT off (here is a min delay of 100ns)
SW2*-S6 ON:	integrate is started by trigger input of Cam control
SW2*-S6 OFF:	integrate is started by XCK goes high (internal mode).

*SW1 if one channel version as 2nd board is missing here.

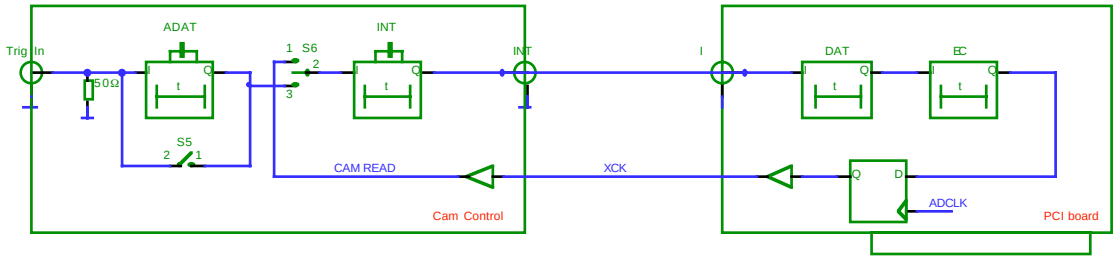
3.3.1 Analog Delay

The analog delay can be used to start the integrate before the camera read starts or when very short and accurate delay after trigger is needed. This is the default setup.

For very short delay the ADAT(P6) can be switched off by SW2*-S5 (picture-5.1).
With S5=OFF the analog delay after trigger (ADAT) of the Cam Control is disabled.
There is still a minimal delay of 100ns coming from the input filter.

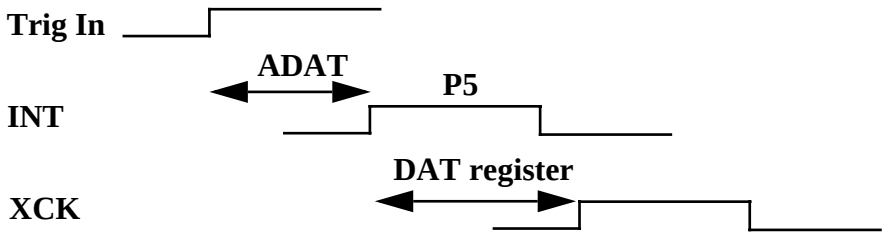
Setup for analog delay
setup a cable from INT to PCI boards „I“ connector or use the ext. trigger directly.
Cam Control:
Trigger In of Cam Control starts sequence
SW2*-S5 ON/OFF: analog ADAT if needed.
SW2*-S6 ON: integrate is started by trigger input of Cam control
DAT register sets additional delay for starting XCK (camera read) if needed.

picture-3.7: Setup for analog delay



ADAT = P6, INT = P5, DAT and EC are registers of the PCI board (see camera manual).
The Software must be set to external trigger.

picture-3.8: Timing with analog delay



selecting the pos. slope for the software trigger sets read to start of INT, selecting the neg. slope sets software trigger to end of INT.
With DAT and EC the start of XCK can be set to occur after INT is ready.
The INT Jitter is very low, the XCK Jitter is the ADCLK. The XCK Jitter does not matter much here, as the laser pulse is already gone.

Alternativ: the PCI Trigger Input (I) can also be connected directly to the trigger source.

* SW1 if 0ne channel version.

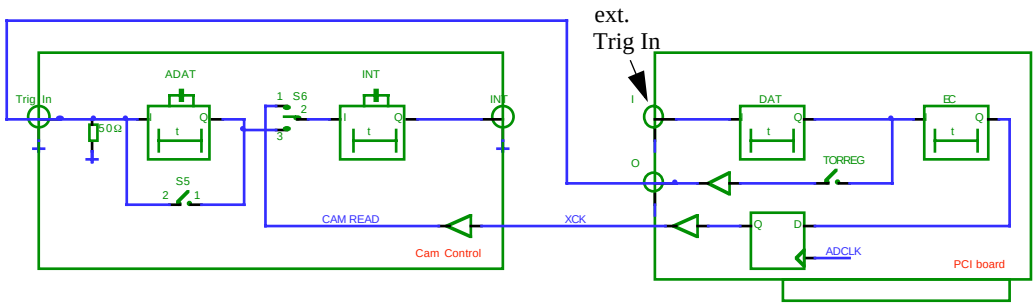
3.3.2 Digital Delay

Here the Trigger input is the BNC/Cinch plug marked I on the PCI Interface board. The trigger starts the camera read as explained in the camera manual. The DAT register can be used to delay the trigger before the integrator starts.
The duration of the integration is set by P5 of the Cam Control (picture-5.4). When all pixel values are sampled the additional 4 photo diode channels are switched to the A/D converter. The camera read can be delayed independant from the integration with the EC register to start after integrate is ready. All signals should be monitored with a scope during adjustment. The Softwaretrigger can be set to external or internal.

Setup for digital delay
PCI board:
if external: ext. Trig In „I“ of PCI board starts sequence
DAT register sets the delay after trigger for starting INT
EC register sets the start of the camera read (XCK) -> should be set >1
TOR register bit EC=1 must be set to = 0x40 -> trigger O is EC signal (see cam manual)
setup a cable from PCI connector O to the trigger input of Cam Control
Cam Control:

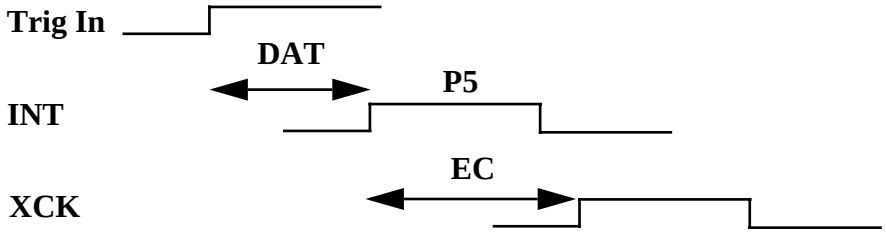
SW2*-S5 OFF:	analog DAT not needed.
SW2*-S6 ON:	integrate is started by trigger input of Cam control
P5	sets the duration of integrate INT

picture-3.9: Setup for digital delay



ADAT = P6, INT = P5, DAT and EC are registers of the PCI board (see camera manual).

picture-3.10: Timing with digital delay



The XCK Jitter is the ADCLK (1µs), Jitter of INT is 1/1000 of duration.

* SW1 if 0ne channel version.

3.3.3 Internal mode

In internal mode the frequence generator of the PCI board is used to control the timing. It can be used for testing the system without external trigger, or if possible to trigger the laser by the Cam Control. Here the trigger output „O“ of the PCI board can be used.

Here the XCK signal is connected back to the Cam Control inside the camera cable (picture-3.9 with S6 connecting 1 to 2).
SW1-S6 OFF:integrate is started by XCK goes high.
The duration of the integration is set again by P5 of the Cam Control (picture-5.4).
The Software must be set to internal or external trigger. Every read now starts the integrator at the beginning of the read sequence.

3.4 Power Supply

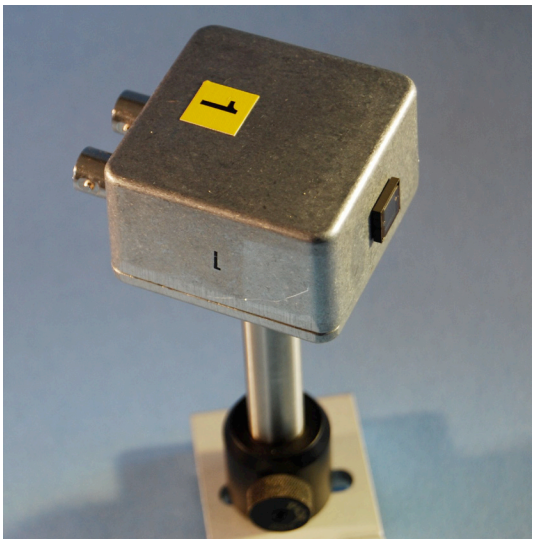
The main power switch is on the rear panel.
The power unit is a switching power supply with an input range of 110 - 240 V / 50-60 Hz with a voltage of 5V and 3A or 5A. All other voltages are derived by additional DC/DC - converters from these 5V. The power consumption is max. 10W.
The main fuses are beneath the power plug on the rear panel (2 items T1A). It can be reached after unplugging the cord and lifting the lid of the power connector.

4 Accessory

4.1 Photo diode (PD) Amplifier

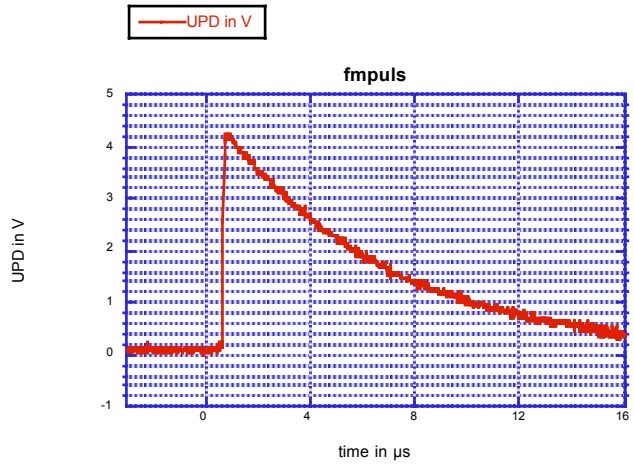
We offer a well suited active photo diode amplifier for the Cam Control. Here the amplitude and the duration is optimized for the integrators input. The diode is especially a slow type with high capacity, to stretch the pulse to a time scale the integrator can handle. The power (6,8V) is supplied by the CamControl (no battery needed).

picture-4.1: PD Amplifier



Our PD amplifier supplies the signal which is best suited for the Integrators input (see chapter-3.2.3). The monitor BNC plug on the rear can be used to control the signal of each channel. The amplitude should not go beyond 4V and should be attenuated by optical filters if needed.

picture-4.2: femto second monitor pulse of PD amplifier



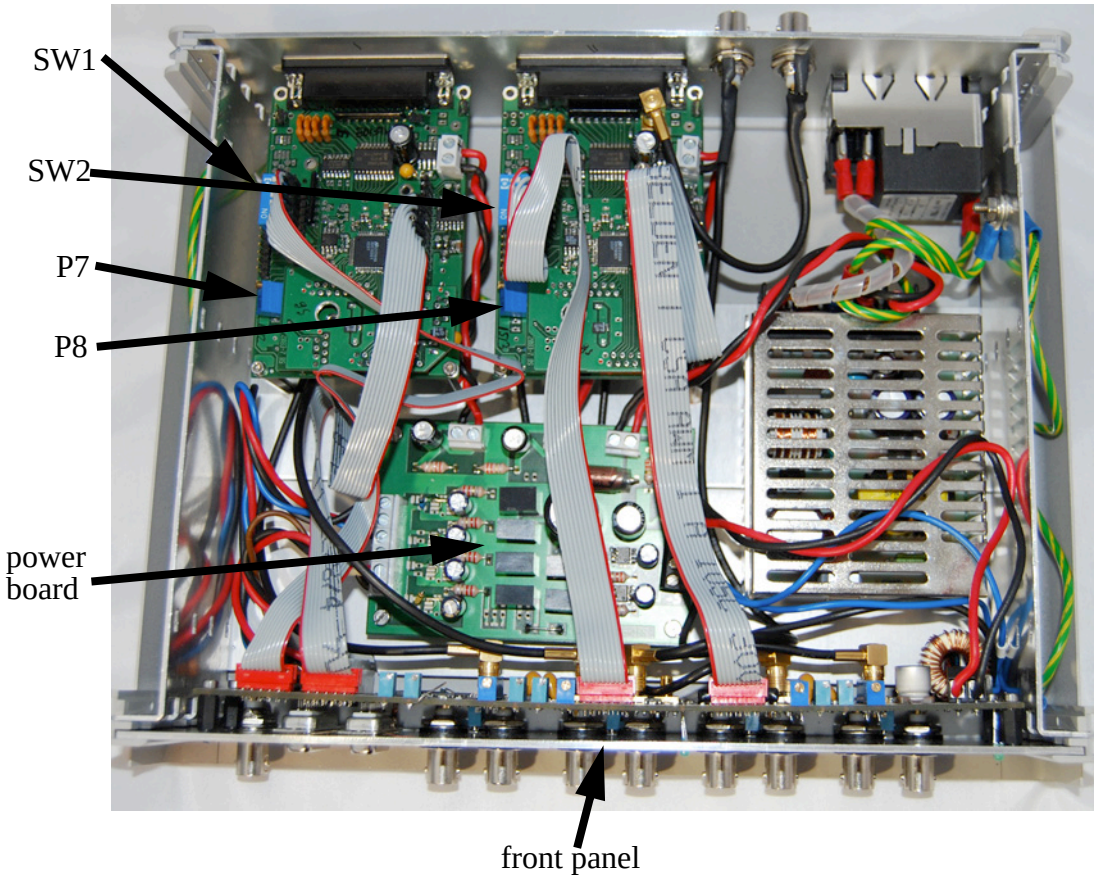
5 Maintenance

5.1 Adjustments

The Cam Control is completely aligned in the factory. Beside that especially the zero line levels can change over time and temperature. In that case they can be realigned as described here. The full scale levels do not change much, so they should not be altered.

The following picture shows the components of the Cam Control.

picture-5.1: opened Control unit



The potentiometers of the Control unit:

P7: full scale of camera signal CHA
P8: full scale of camera signal CHB
SW1: switch for CHA
SW2: switch for CHB

The power board supplies the voltages:

left connector	right connector
+7V	5,6V
+23V	-5V
-9V	-15V
+7V	

5.2 Front Panel

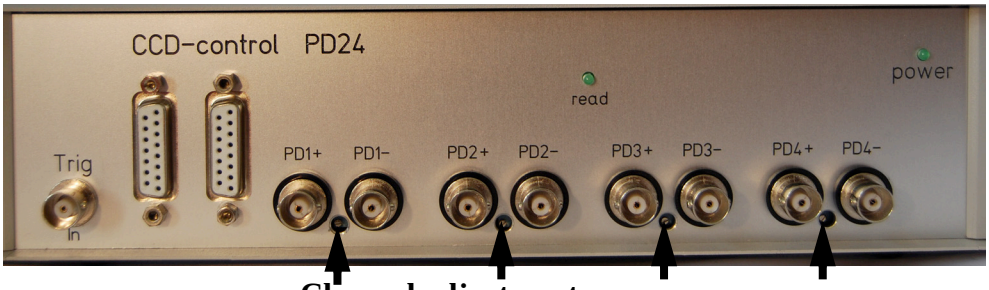
5.2.1 Channel Adjustment potentiometers

With P3 and P4 in picture-5.4 both signals of the PDA can be adjusted in relation to the camera signal level. This general level should be around 1000 counts. After that the individual channels must be setup.

The individual channel zero offset is used for adding a slight DC offset to the integrator. Also channel differences can be aligned here. It should be adjusted somewhere above the lowest possible point where it does not go lower.
Be shure to have a valid INT signal (like 20µs) during adjustment procedure. Both inputs should be connected to ground.

5.2.1.1 Front side version

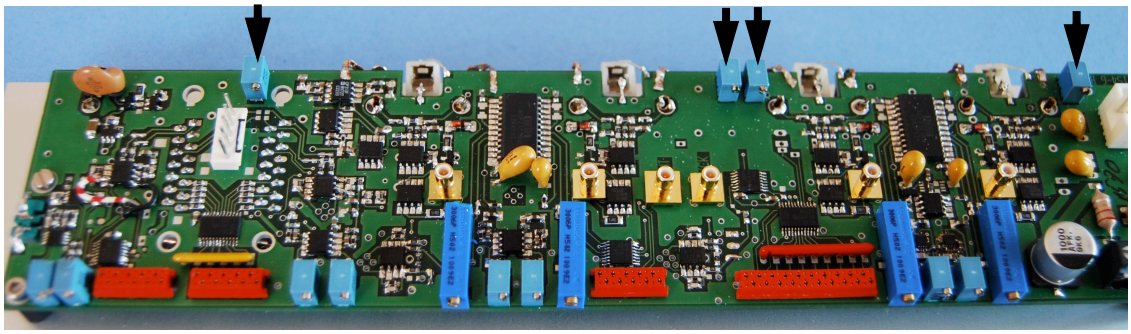
On the front side version the potentiometers are located under the BNC plugs.
picture-5.2: Front Panel version



Channel adjustment

5.2.1.2 PCB version

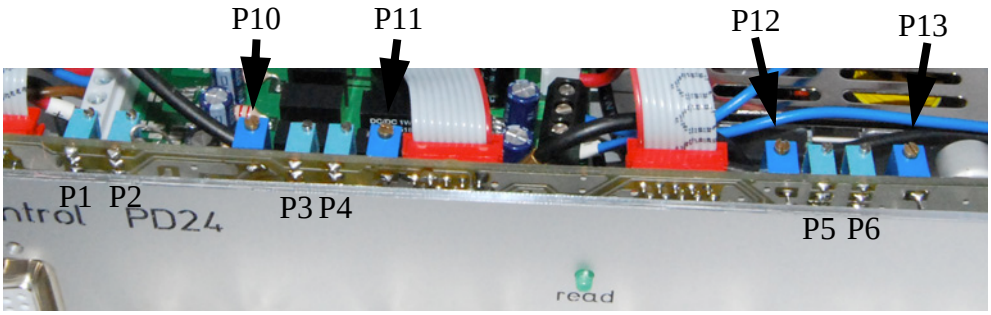
Versions with external power supply for the photo diode amplifiers have the dc plug located on the front side. In that case the potentiometers can be reached from inside the Cam Control.
picture-5.3: PCB version



5.2.2 Top side PCB Potentiometers

Located on the front panel are the potentiometers for the alignment of the signal levels. They could be reached after opening the case.

picture-5.4: Locations of the potentiometer of front panel



P1: Zero offset of camera signal CH1 (0C)
P2: Zero offset of camera signal CH2
P3: Zero offset of integrator signal CH1 (0P)
P4: Zero offset of integrator signal CH2
P5: tint = integration time : when high, the integrator is active, low = hold
P6: dat = delay after trigger - only for Cam Control trigger input
P10: full scale of integrator signal PD CH1
P11: full scale of integrator signal PD CH2
P12: full scale of integrator signal PD CH3
P13: full scale of integrator signal PD CH4

With the specific potentiometers each signal could be aligned.

After the zero levels are all set, the full scale integrators should be set.
Apply a 2V DC level to the ±inputs. Check that the PD output signal has now a constant 4V level. With an INT signal of 20µs the Pixel values of the tested channel should have a little less then the maximum value. This is aligned with P10 to P13.

5.3 Changing the analogue range of DAT and INT

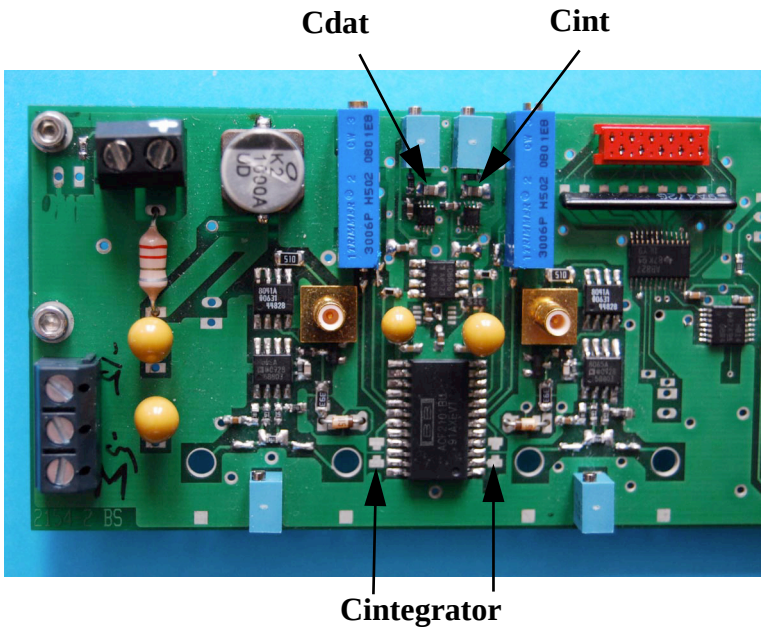
The monostable multi vibrator which sets the delay after trigger (DAT) and the integrating window (CINT) can be changed if necessary. The timing value is t = R * Cint. R is the potentiometer with 20kΩ + 1kΩ resistor and Cint is default 4.7nF. With these values the range is given:

default:
if Cint=4n7 delay range = 6-100µs

if Cint=22n the range is 8-450µs
if Cint=1n5 the range is 2-30µs

The SMD capacitor is mounted at the pcb as shown in picture-5.5. The Cs are mounted directly on the surface to guarantee very low Jitter. If they need to be replaced, a person with experience should do that, as the neighbor parts should not be damaged.

picture-5.5: Location of timing Capacitors



5.4 Changing the photo diode integrators range

It is also possible to change the range of the build in integrator of type ACF2101 (BB/TI) These ICs have a build in capacitor of 100pF. In some cases it might be necessary to change that. In those cases the empty Cintegrator pads (see picture-5.5)can be used. If so, a small connection between pin #2 , #3 and #22 , #23 must be removed.

6 Technical data

weight DL control	2,2 kg
size	280 x 220 x 70 mm

6.1 Technical Data of the DL control

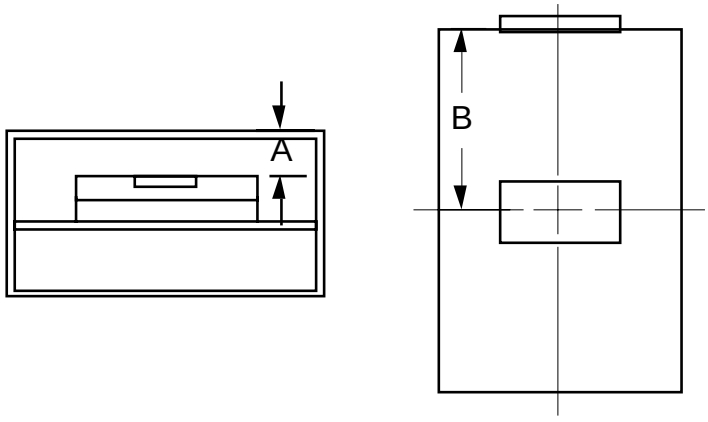
Power consumption FFT Type (max.):	9W (10 W)
Power consumption PDA Type (max.):	5W (7 W)
Input voltage	110-250V/50-60Hz
Fuse	T1A / 220V
Type of power supply	RS-25-5
version with external photo diode supply delivers (4x)	6,8V / 25mA max.
Jack plug (outer connector is gnd, inner is plus)	2.5mm

6.2 Integrator

int Trigger Sw2-S6=off (triggered by computer)	
delay after XCK goes high	80ns
Integrator signal - INT (P5) Cint = 4n7	
int range =	6-100µs (default: 20µs)
ext Trigger S6=on (trigger on front panel)	
Sw2-S5=off no DAT, delay after trigger	70ns
Sw2-S5=on with DAT, delay after trigger	6-100µs
Integrator signal - INT (P5) Cint = 4n7	
int range =	6-100µs

6.3 Adapter Size

picture-6.1: Case Size of Adapter



6.4 Technical Data of the FFT single channel Adaptor - S7030

size with case	85x65x30 mm
pcb board size (2152)	78x55 mm

Sensor Distance A = 5.5 mm (+ inner sensor window <-> chip: 3.2mm),

B = center

6.5 Technical Data of the PDA double channel Adaptor

size with case	85x65x30 mm
pcb board size (2128)	78x55 mm

sensor distance A = 6.3mm (+ inner sensor window <-> chip: 1.3mm),

one sensor version
B = center

double line version
sensor one B = center, sensor two B = center + 13.0 mm

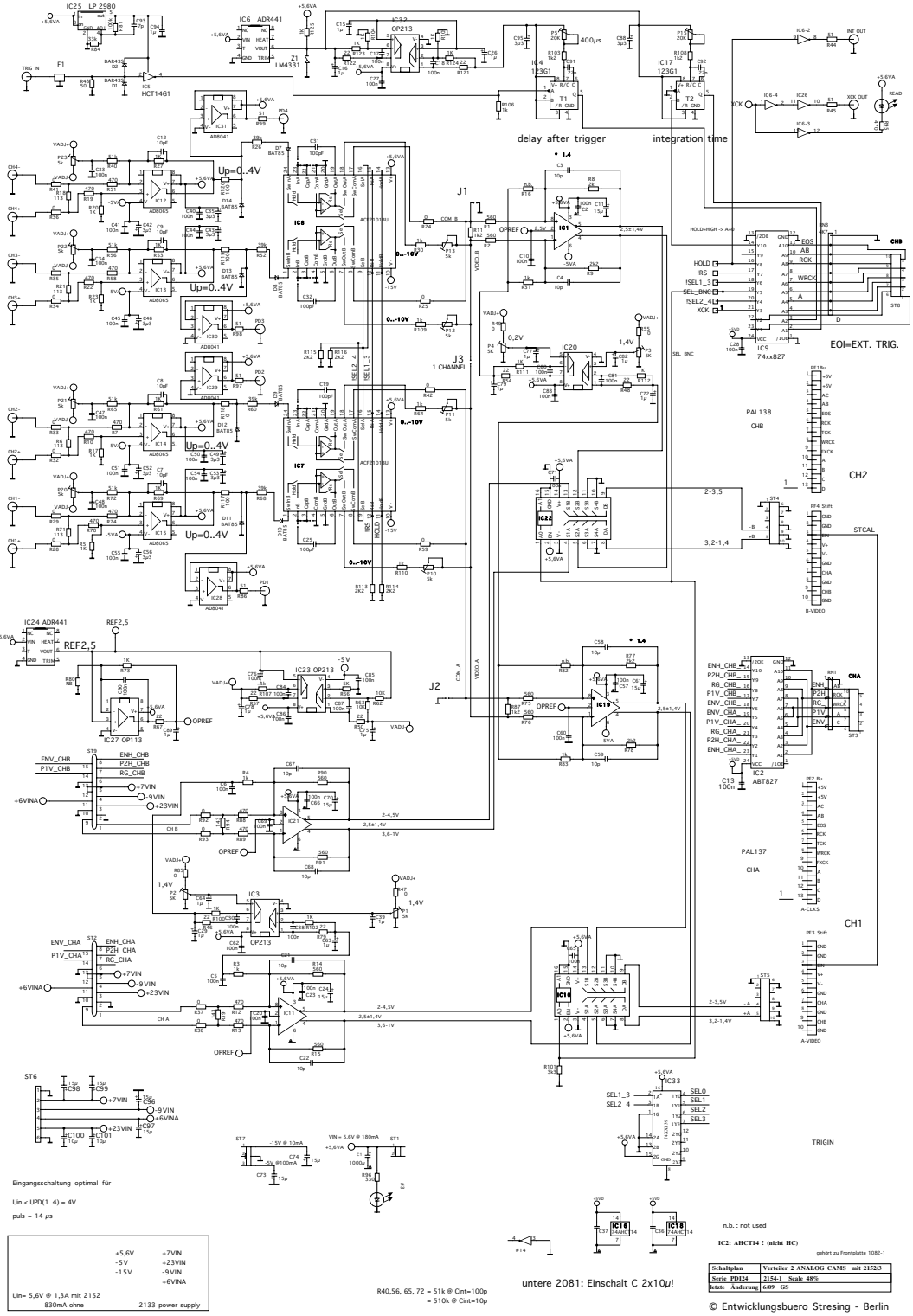
6.6 Technical Data of the FFT double channel - S9840

size with case	107x85x30 mm
pcb board size (2147)	99x77 mm

6.7 Technical Data of PD Amplifier

size	110x60x30 mm
Voltage (min.)	9V (6V)
Current	20mA

picture-6.2: Schematic of Cam Control



picture-6.3: Schematic of PD Amplifier