Faculty of Engineering
Cairo University

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Electronics project

Submitted to

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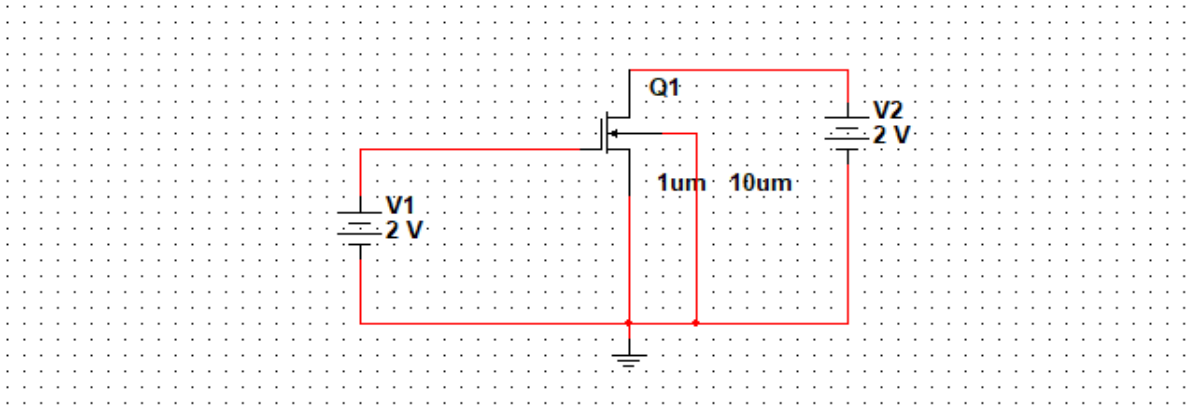
Note: يوجد جداول ملخص نتائج في نهاية كل مسألة للتسهيل

Q1.Transistor Characterization:

In this problem we need to determine the parameters for Mos like µcox & λ & VTH for both NMOS &PMOS and compare between results:

NMOS:

a) W=10um &L=1um



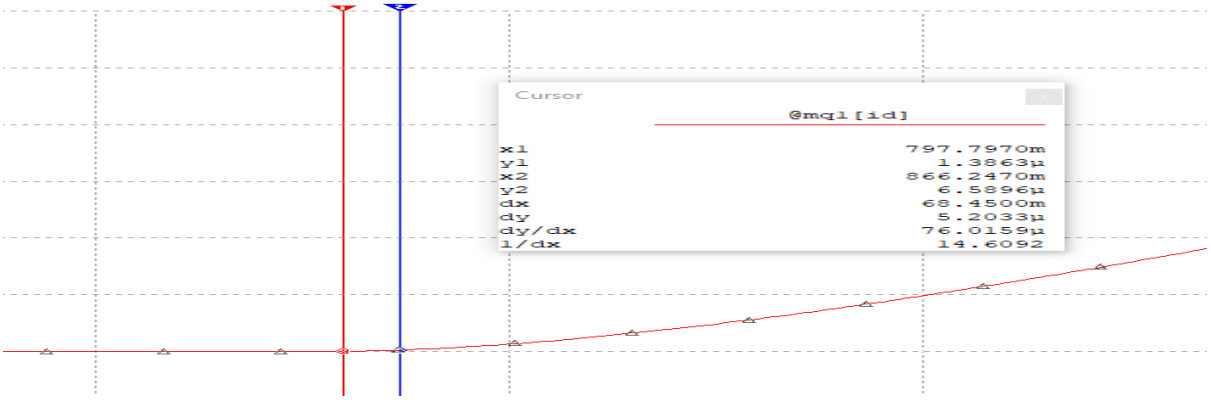
(1) Schematic diagram

Design Procedure & Simulation results:

Vin=VGS=, Vout=VDS (as VS is grounded) we also connect the substrate to the least voltage in circuit so we connect it to ground.

1.First case:

we will sweep Vin from (0 to 3V) while Vout=2V ,in this case we will study the variations of IDS with VGS so we can determine VTH, and this is the result of simulation:

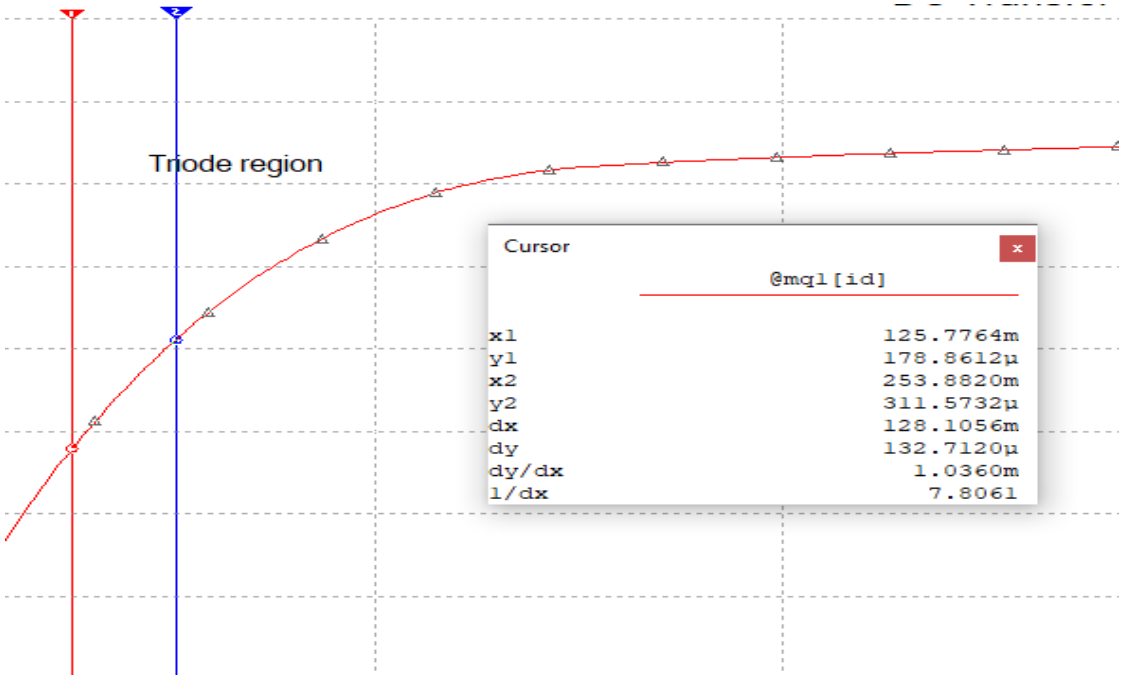


(2) "The relation between IDS&VGS"

From this curve we can determine VTH as it is the value for VGS to be a signficant value for Ids, from figure (2) we found that: VTH=0.798V

2.Second case:

we will sweep Vout from (0 t0 3V) while Vin=2V ,in this case we will study the variations of IDS with VDS so we can determine µnCox from the triode region and λ from the saturation region , and this is the result of simulation:



(3)"The relation between IDS &VDS in triode region"

From the equation of the current in Triode region:

IDS= µnCox (W/L) ((VGS-VTH) VDS –VDS^2 /2)

We can neglect the squaring term of VDS and then we can from this equation determine µnCox as the slope of figure(3) equals

µncox(W/L)(VGS-VTH)

We can obtain µncox:

µnCox=slope/((W/L) (VGS-VTH))

(W/L)=10 , VGS-VTH=2-0.798=1.202 V , slope=1.0360 mm

µnCox= $8.62x10^{-5}$

And we will calculate λ from the equation of current in saturation region:

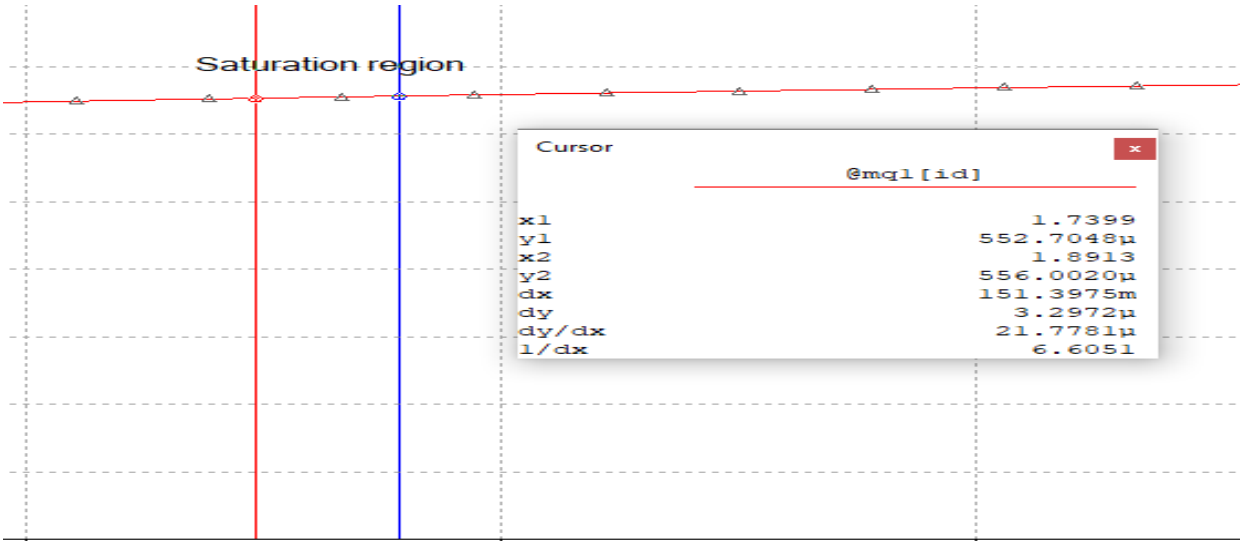
IDS= 0.5 µnCox (W/L) ((VGS-VTH)2(1+ λ VDS)

So we can get the slope of the curve in sat region then

λ = slope/RS

Where RS= 0.5 µncox(W/L)((VGS-VTH)2

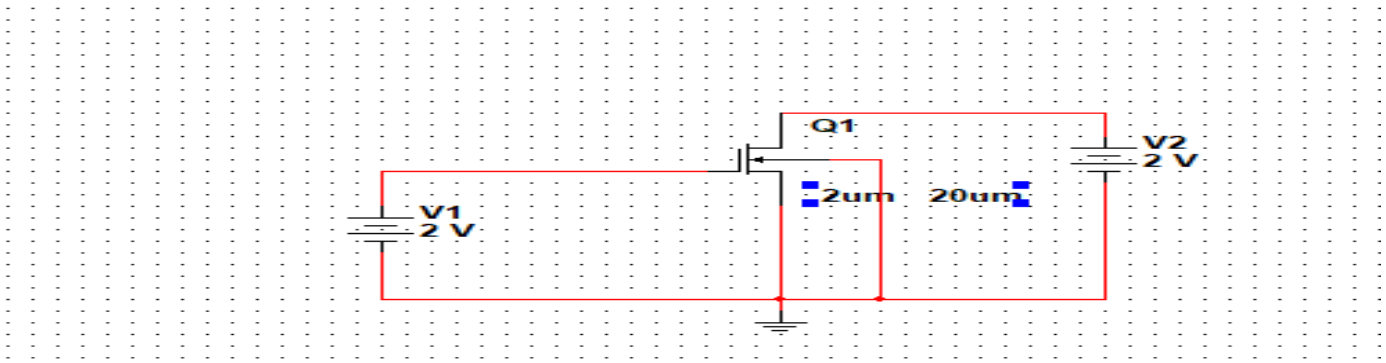
The slope from simulation results:



(4)"The relation between IDS &VDS in Sat region"

Slope=21.7781um then: λ =0.035

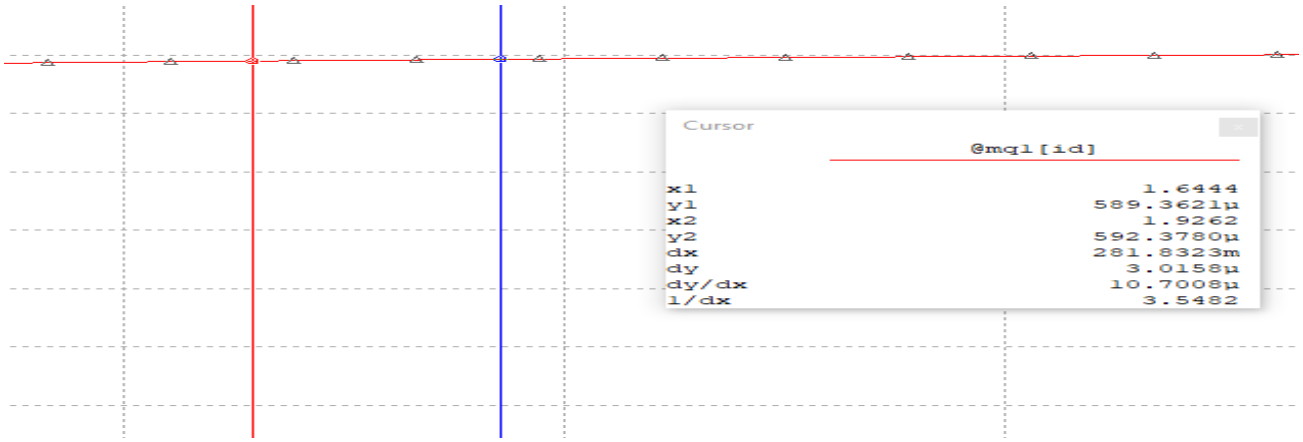
b) W=20um &L=2um



(5)schematic

DISSCUTION:

For the value of VTH it doesn't change as this value depends on the the temperature and the fabrication of the MOSEFT ,for µncox it also doesn't change as it depends also on another parameters not related to length and width of the MOSEFT and if, it depends on the ratio between them and in our case it is still the same the ratio between length and width, for λ it will change as λ depends on the length of the MOS (λ α (1/L)) so when L increase the λ will decrease and the curve in sat region will be more flatter as shown:



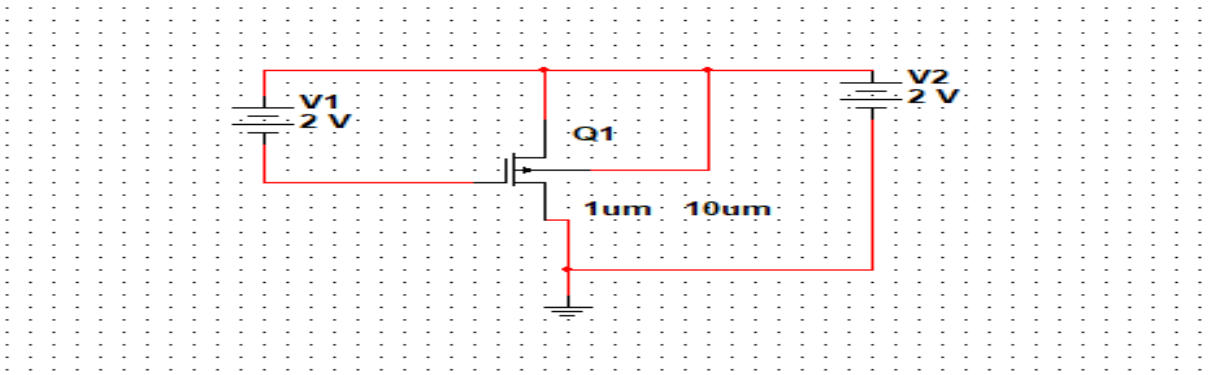
(6) "The relation between IDS &VDS in Sat region"

Slope=10.7um

So λ=0.017

PMOS:

a) W=10um &L=1um



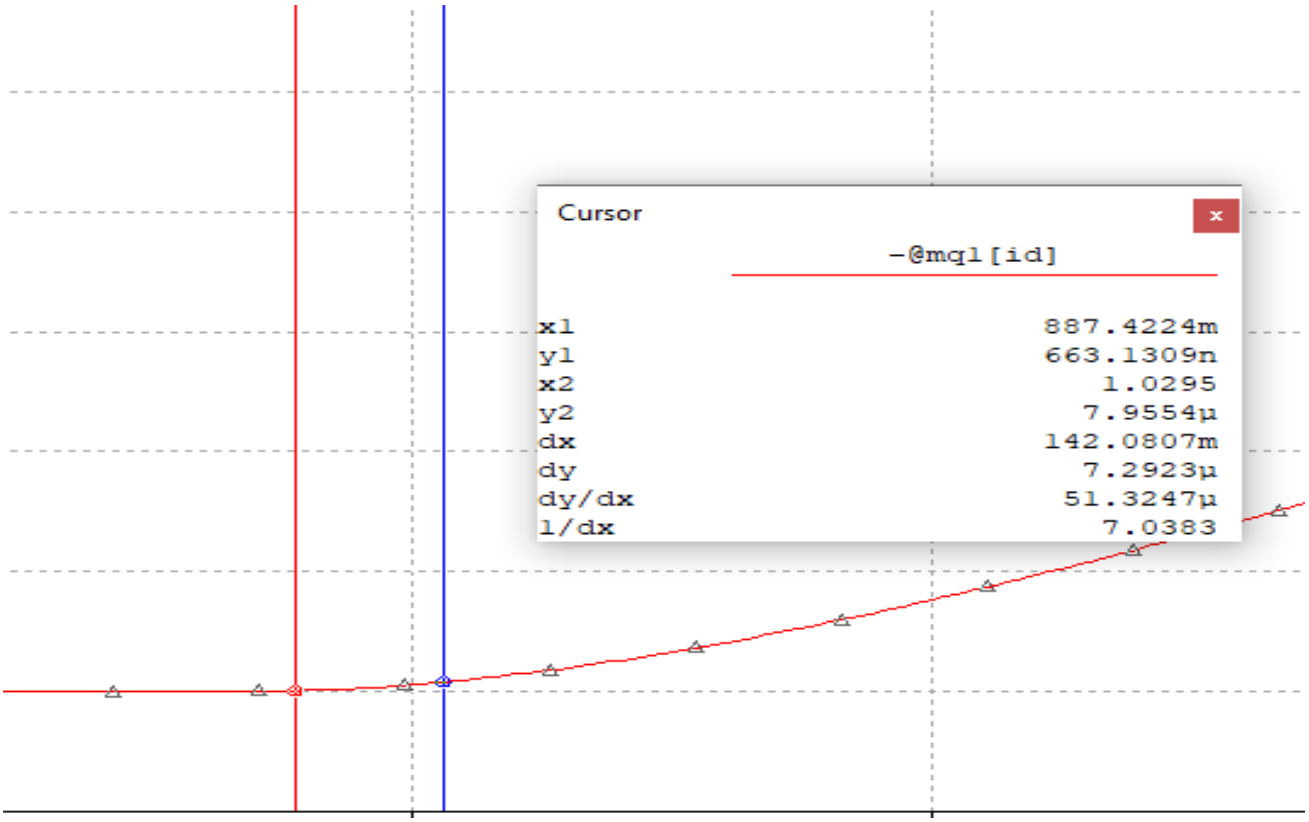
(7)pmos schematic

Design Procedure & Simulation results:

Vin=VSG=, Vout=VSD (as VD is grounded) we also connect the substrate to the most voltage in circuit.

1.First case:

We will do as we did in NMOS :

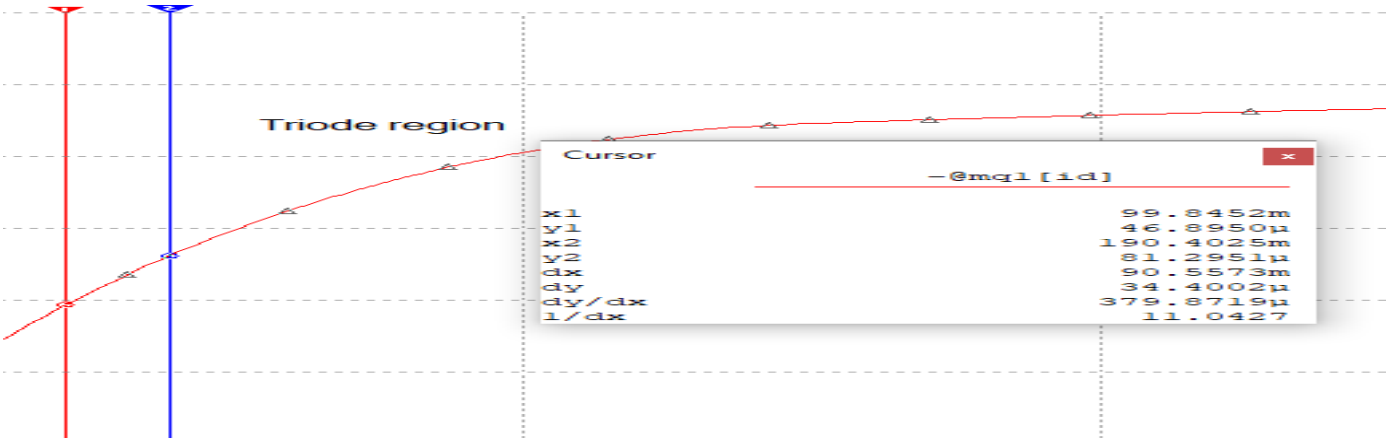


(8)"The relation between VSG&ISD"

From this curve we can determine VTHp as it is the value for VSG to be a signficant value for ISD, from figure (8) we found that: |VTHp|=0.887V

2.Second case:

We will do as we did in NMOS:



Figure(9) "The relation between ISD &VSD in triode region"

From the equation of the current in Triode region:

ISD= $\mu pcox(W/L)((VSG - |VTHp|)VSD - VSD^2/2)$

We can neglect the squaring term of VSD and then we can from this equation determine µpcox as the slope of figure(9) equals

µpcox(W/L)(VSG-|VTHp|)

We can obtain µpcox:

µpcox=$\frac{slope}{(W/L)(VSG-|VTHp|)}$

(W/L)=10 , vsg-|vthp|=2-0.887=1.113 V , slope=379.87 um

µpcox= 3.4x10^{-5}

And we will calculate λ from the equation of current in saturation region:

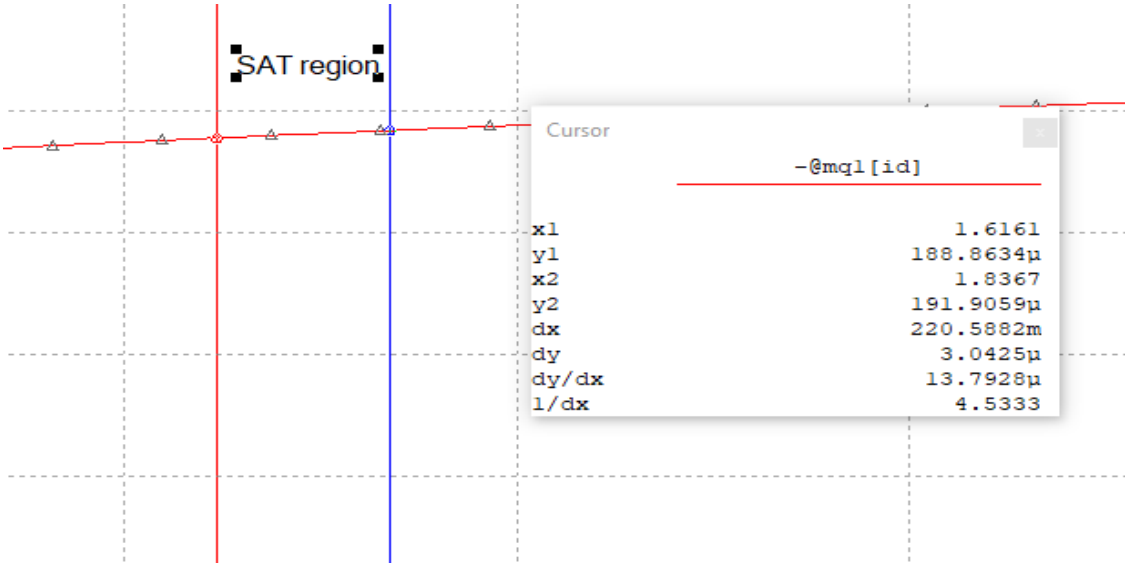
ISD= 0.5 µpcox(W/L)((VSG-|VTHp|)2(1+ λ VSD)

So we can get the slope of the curve in sat region then

λ = slope/RS

Where RS= 0.5 µpcox(W/L)((VSG-|VTHp|)2

The slope from simulation results:



Figure(10)"The relation between ISD &VSD in SAT region"

Slope=13.7938um then: λ =0.066

b) W=20um &L=2um

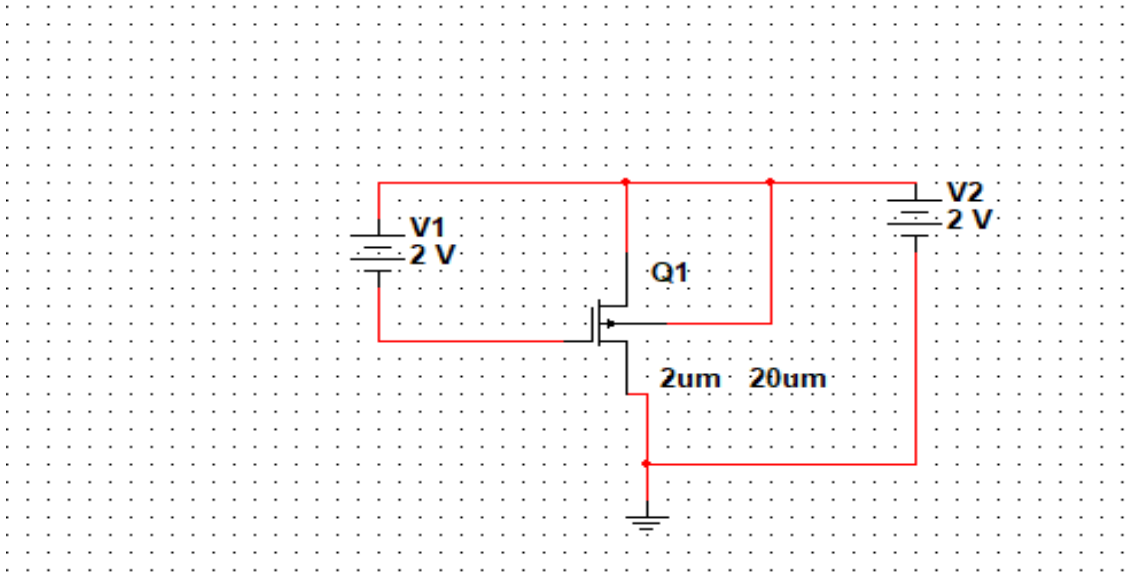
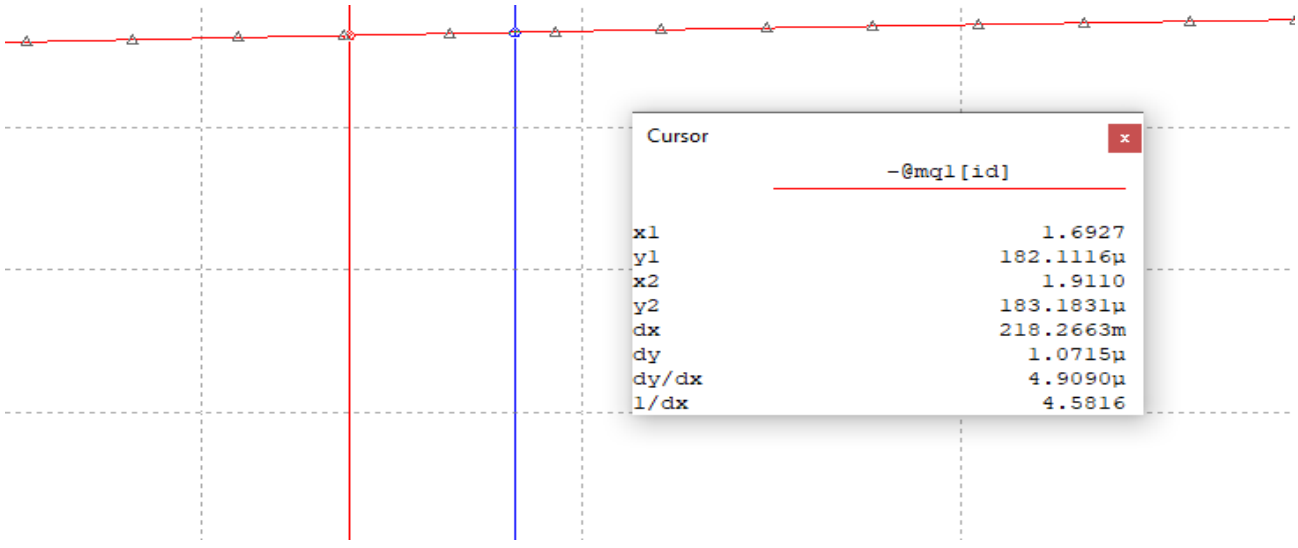


Figure (11)

DISSCUTION:

For the value of |VTHp| it doesn't change as this value depends on the the temperature and the fabrication of the MOSEFT ,for µpcox it also doesn't change as it depends also another parameters not related to length and width of the MOSEFT and if, it depends on the ratio between them and in our case it is still the same the ratio between length and width, for λ it will change as λ depends on the length of the MOS (λ α (1/L)) so when L increase the λ will decrease and the curve in sat region will be more flatter as shown:



Figure(12)

Slope=4.909um

So λ=0.023

SUMMARY&CONCLUSTIONS:

NMOS	VTH	μcox	λ
W=10um L=1um	0.798	$8.62x10^{-5}$	0.035
W=20um L=2um	0.798	$8.62x10^{-5}$	0.017
PMOS			
W=10um L=1um	0.887	$3.4x10^{-5}$	0.066
W=20um L=2um	0.887	$3.4x10^{-5}$	0.023

THE comparison between PMOS &NMOS:

1-VTH of PMOS is a little bit more than NMOS

2- μcox of NMOS is more than PMOS as the mobility of electrons is more than the mobility of holes

3-the channel length modulation of PMOS is more than NMOS and this cause in NMOS the curve of current in sat region is more flatter as it has a small λ

And this decrease the percentage error for example in current mirror

4-for both NMOS& PMOS when the length of MOS increase

Channel length modulation decrease and the error decrease but as we knew in current mirrors when we increase L that will effect on compliance voltage and these are the trades off design.

Q2.Current Mirrors:

a) Simple Current Mirror

1.First Case

we are given that:

Iin=100uA, Iout=200uA, Veff=0.25, L=1um for both

We need to determine the width of each transistor:

To operate these transistors as current mirrors they should be in sat

So by using the equation of current in saturation we can obtain W

For M1 :IDS|in= 0.5 µnCox (W/L) ((VGS-VTH)2

We have µnCox=8.62x10-5

Then W1=37um then from mirroring W2=74um

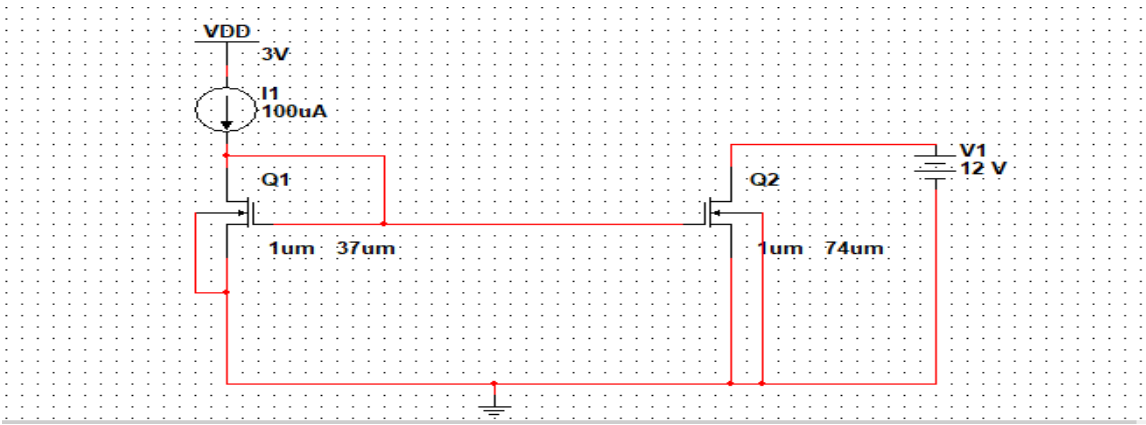
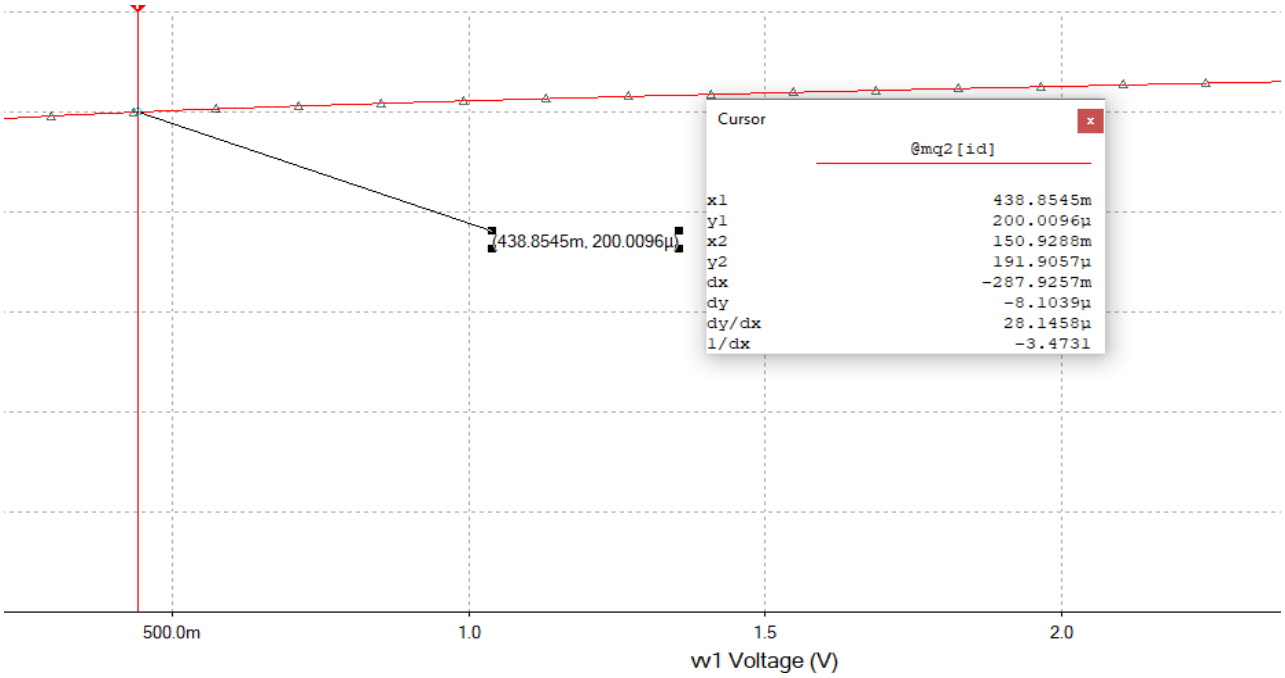


Figure (13)

Compliance voltage is the min value for Vout for the circuit to operate as a current mirror. In our case to operate M2 in SAT it needs as a min value VDS sat that equals Veff ,and in this problem Vout=VDS then Vout min=VDS sat=Veff.

Then Vcomp.=0.25 V this value we get it through hand calculations let us get by plotting

Iout and Vout and the value of vout thet we get the output current 200um it will be the compliance voltage and this is the simulation results:



Figure(14)

From the simulation result we can find that: Vcomp=0.44V this is the exact min value of vout to be a 200uA in M2 ,the compliance voltage that we get from hand calcluations will allow to be 197.38671 uA only in M2 and this is the simulation result of DC operating point when we put the vout =0.25 V that means M2 enters the SAT region.

	DC Operating Point	
1	@mq2[id]	197.38671 u

Figure(15)

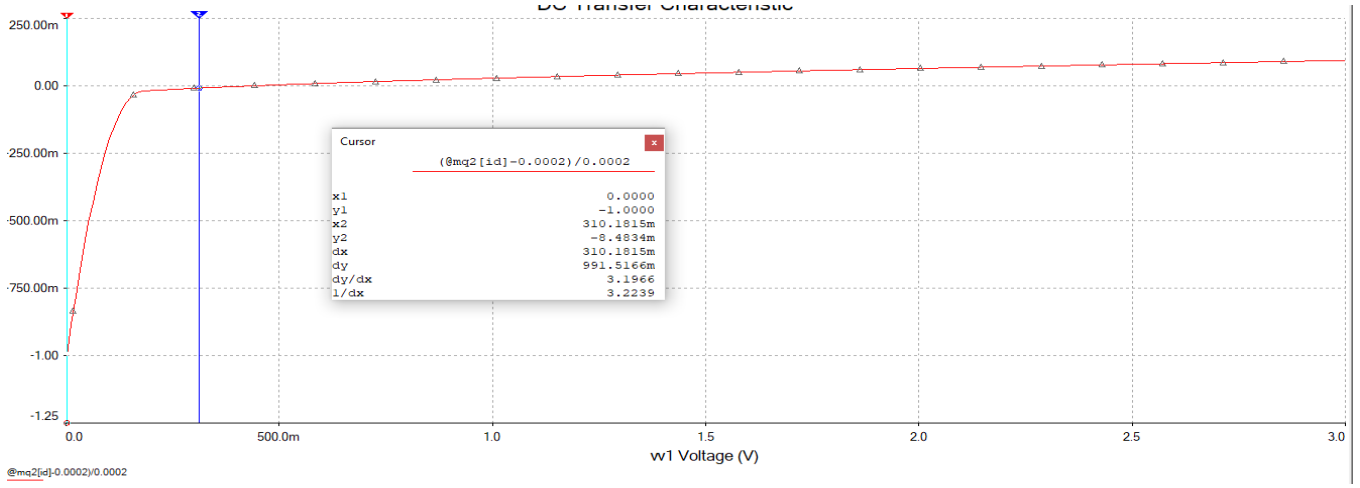
Then we can obtain the percentage error of the current relative to ideal current:

Error=((|I actual – I ideal|)/I ideal)x100

Error=((|197.38671-200)/200)x100

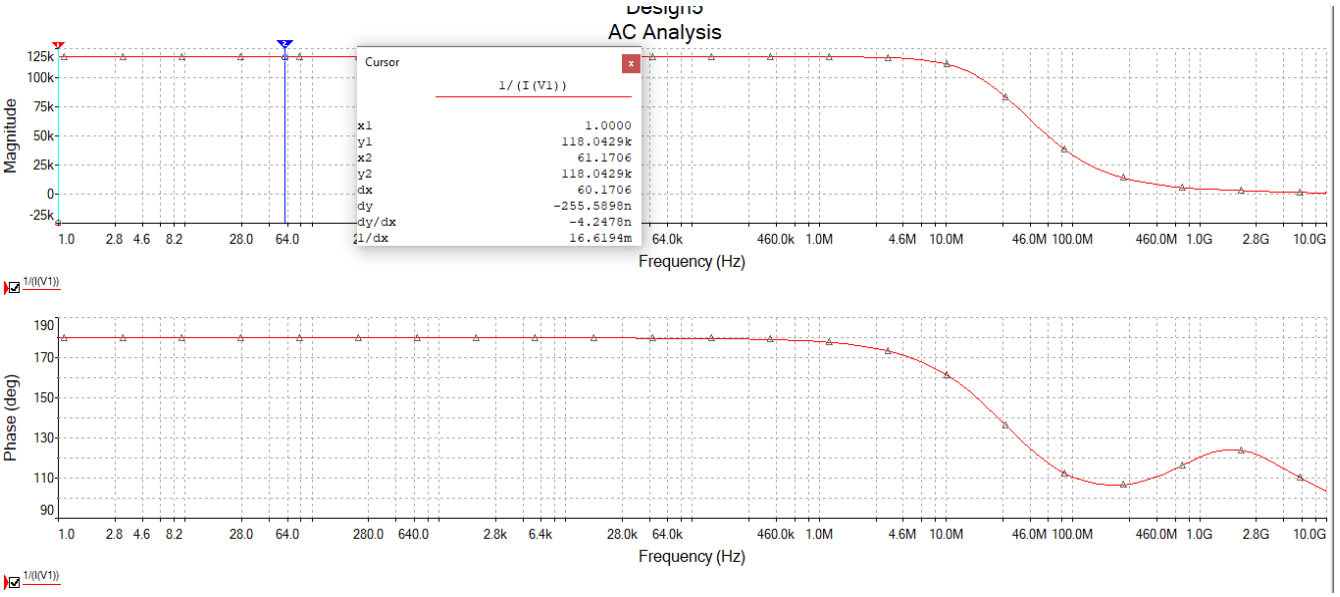
Error=1.3%

If we need to plot the percentage error with Vout ,this is the simulation result:



Figure(16)

We need to determine Rout then we will do AC anaylsis with AC voltage source that the voltage offset of it is more compliance voltage for example (1 V) and this the result simulation:



Figure(17)

From simulation result Rout=118KΩ

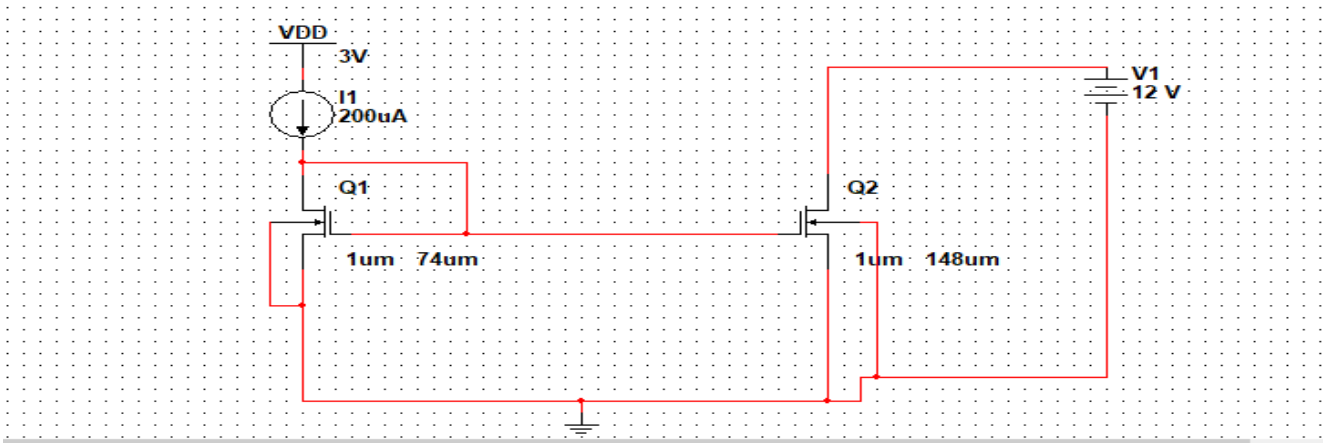
2.Second Case: I in=200uA & I out=400uA & veff=0.25 V & l=1um

We need also to determine W by using the equation of current in saturation we can obtain W

For M1 :IDS|in= 0.5 µnCox (W/L) ((VGS-VTH)2

We have µnCox=8.62x10-5

Then W1=74um then from mirroring W2=148um



Figure(18)

We will repeat what we did in first case:

For compliance voltage by hand caluclations remains the same Vcomp=0.25V

Let plot the relation between Iout& Vout to obtain the exact value for compliance voltage tha will be the value for vout at Iout=400uA and this the simulation result:

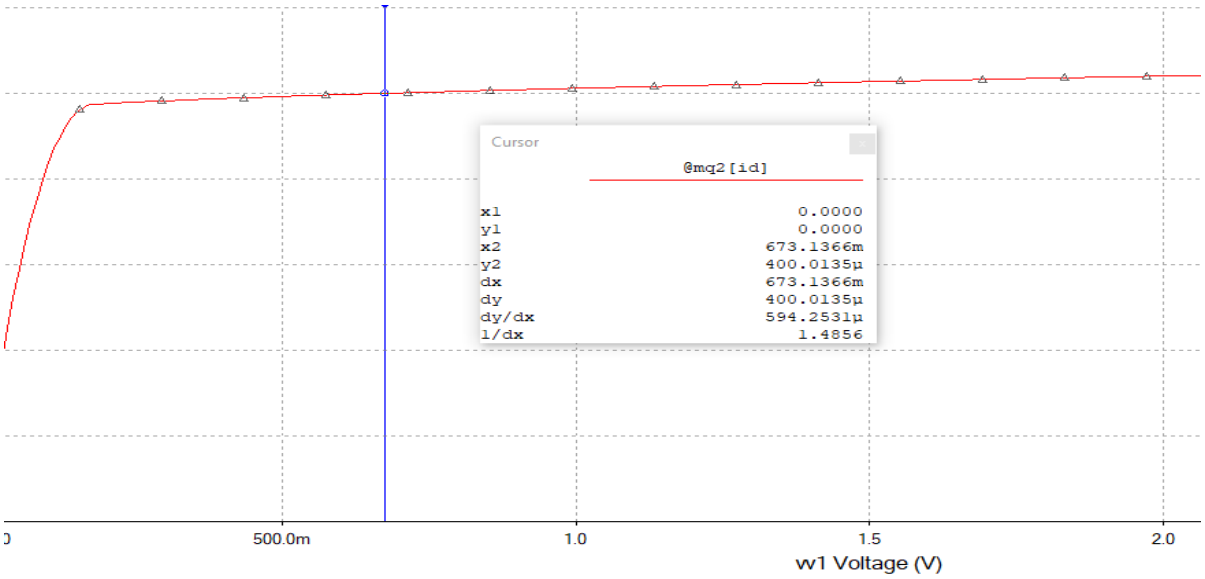


Figure (19)

We found that Vcomp=0.67V

If we need to know the actual current that Iout will be when M2 enters the sat we put the vout with 0.25 V and check DC operating point we found that:

	DC Operating Point	
1	@mq2[id]	389.75649 u

Figure(20)

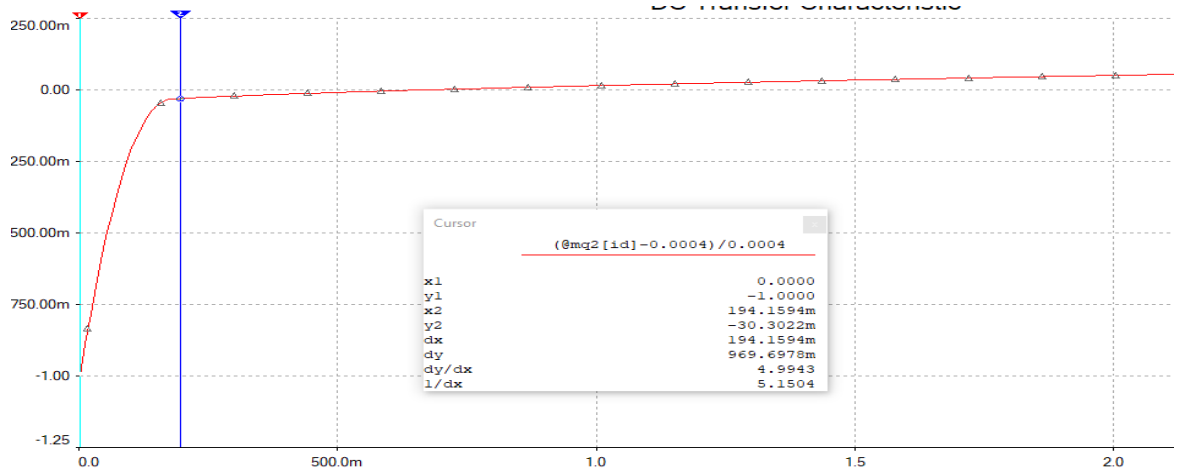
So we found that actual current will be Iactual=389.75649uA

Error=((|I actual – I ideal|)/I ideal)x100

Error=((|389.75649-400|/400)x100

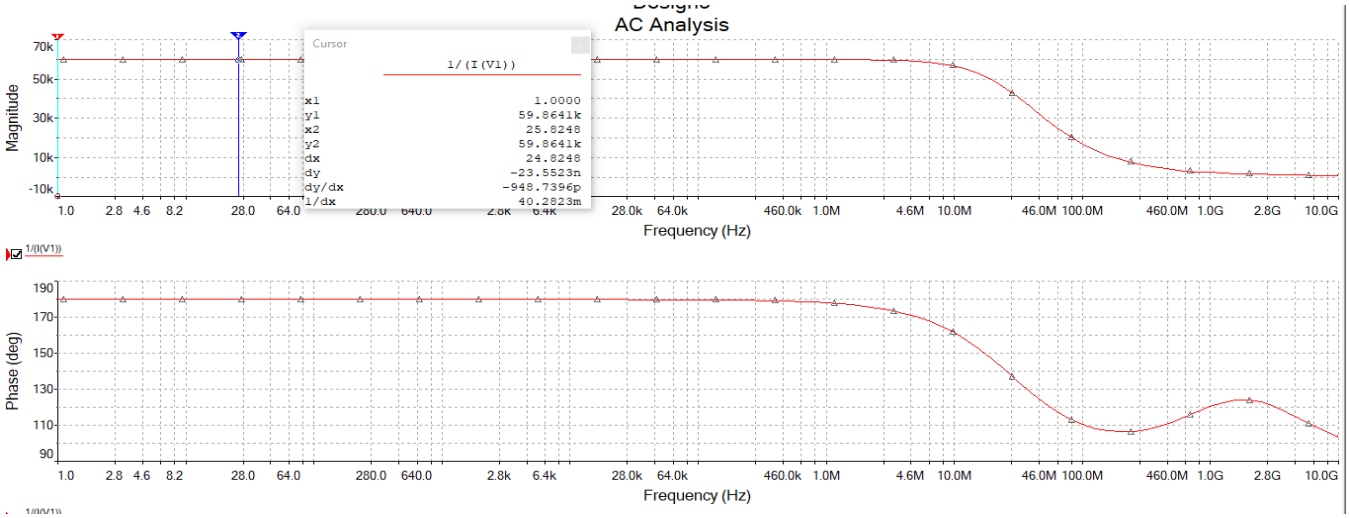
Error=2.56%

If we need to plot the percentage error with Vout ,this is the simulation result:



Figure(21)

We need to determine Rout then we will do AC anaylsis with AC voltage source that the voltage offset of it is more compliance voltage for example (1 V) and this the result simulation:



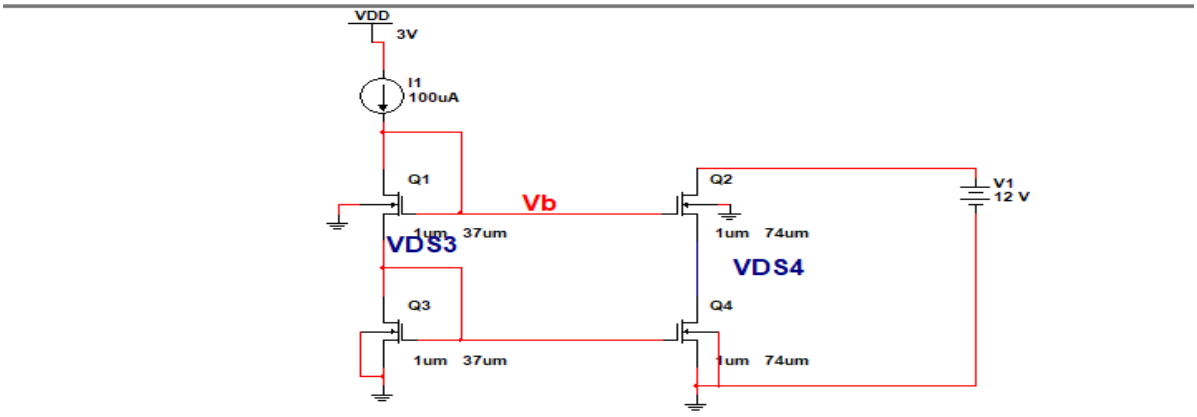
Figure(22)

From simulation result Rout=60KΩ

b)Cascode Current Mirror:

1.First Case:

Iin=100uA , Iout=200uA



Figure(23)

In simple current mirror we neglected the term of λ VDS and this cause error in mirroring we need to increase the accuracy of mirroring so we made a cascode current mirror to increase accuracy of mirroring but this how happens:

In simple current mirror we made VGS of two transistors are equal to take the term of λ VDS in consideration to increase accuracy of mirroring so we need that VDS3=VDS4 to reach high accuracy let's see that condition is satsifaied or not:

All transistors have the same VGS:

Vb=2VGS

VDS3=VGS

VDS4=Vb-VGS=VGS then VDS3=VDS4

Then we get high accuracy but we lose in compliance voltage

Let us obtain Vcomp:

We need M2 to be in sat then:VD4min=Vout min=VG-VTH

VG=Vb =2VGS

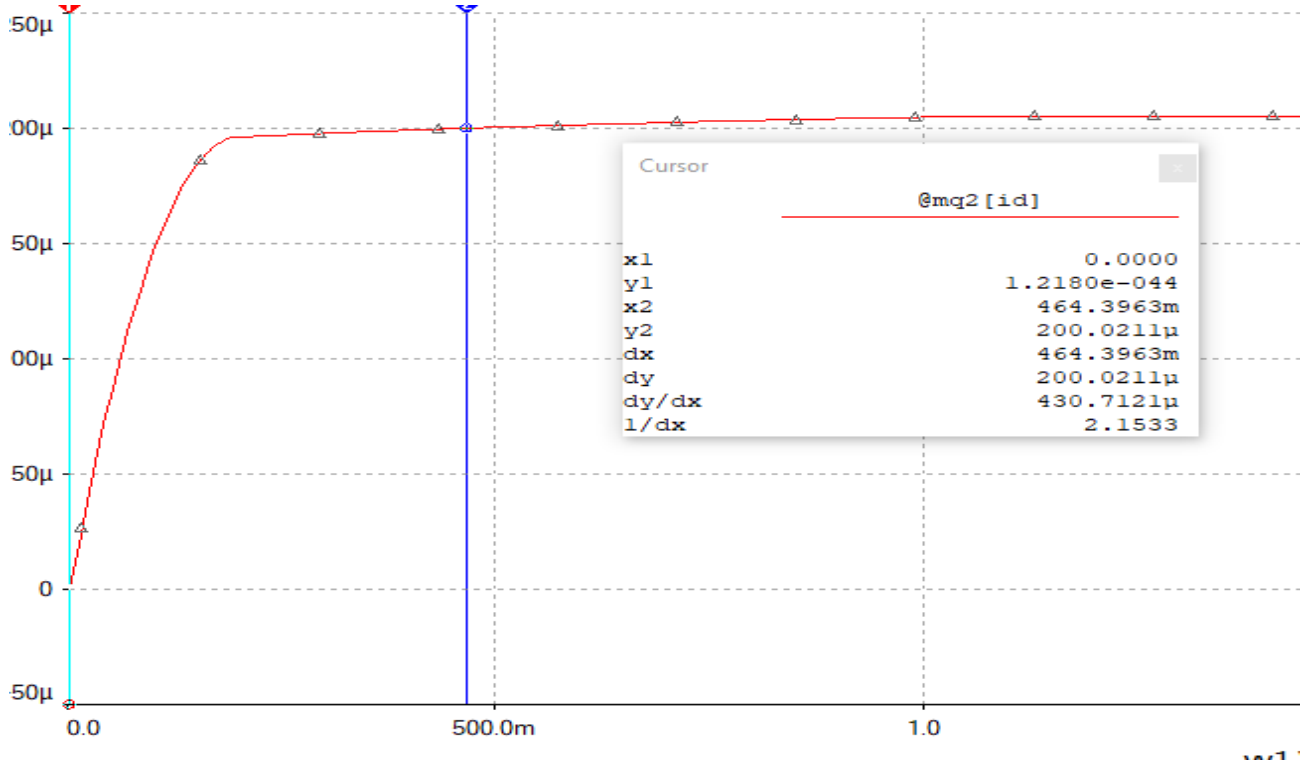
Then Vcomp=2VGS-VTH

Then Vcomp=2Veff+VTH

Vcomp=2*0.25+0.798

Vcomp=1.3V

Let plot the relation between Iout& Vout to obtain the exact value for compliance voltage tha will be the value for vout at Iout=200uA and this the simulation result:



Figure(24)

We found that :Vcomp=0.64V

If we need to know the actual current that Iout will be when M2 enters the sat we put the vout with 1.3 V and check DC operating point we found that:

	DC Operating Point	
1	@mq2[id]	205.29318 u

Figure(25)

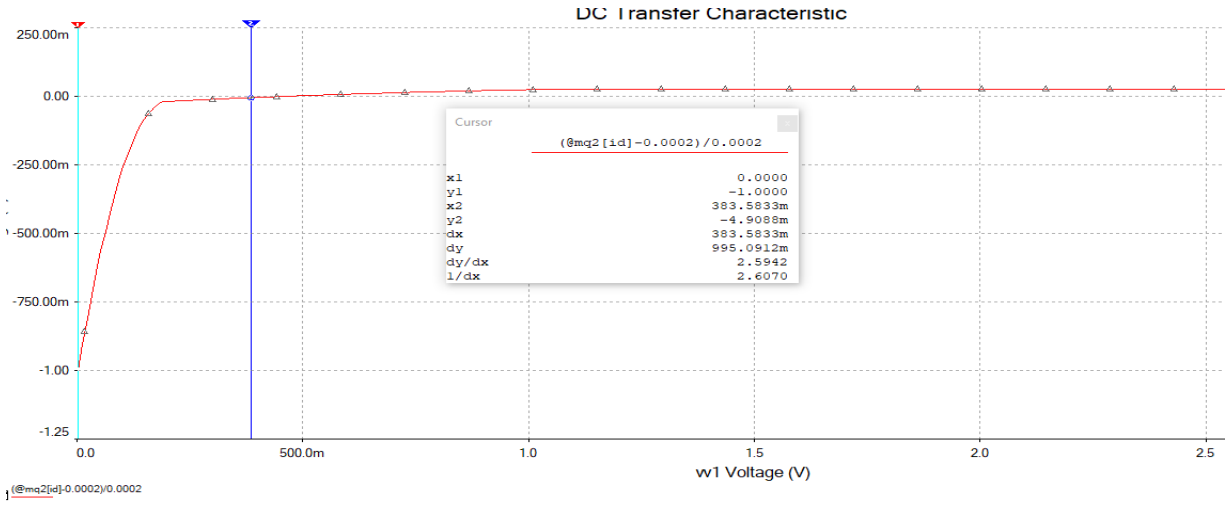
So we found that actual current will be Iactual=205.29318uA

Error=((|I actual – I ideal|)/I ideal)x100

Error=((|205.29318-200|/200)x100

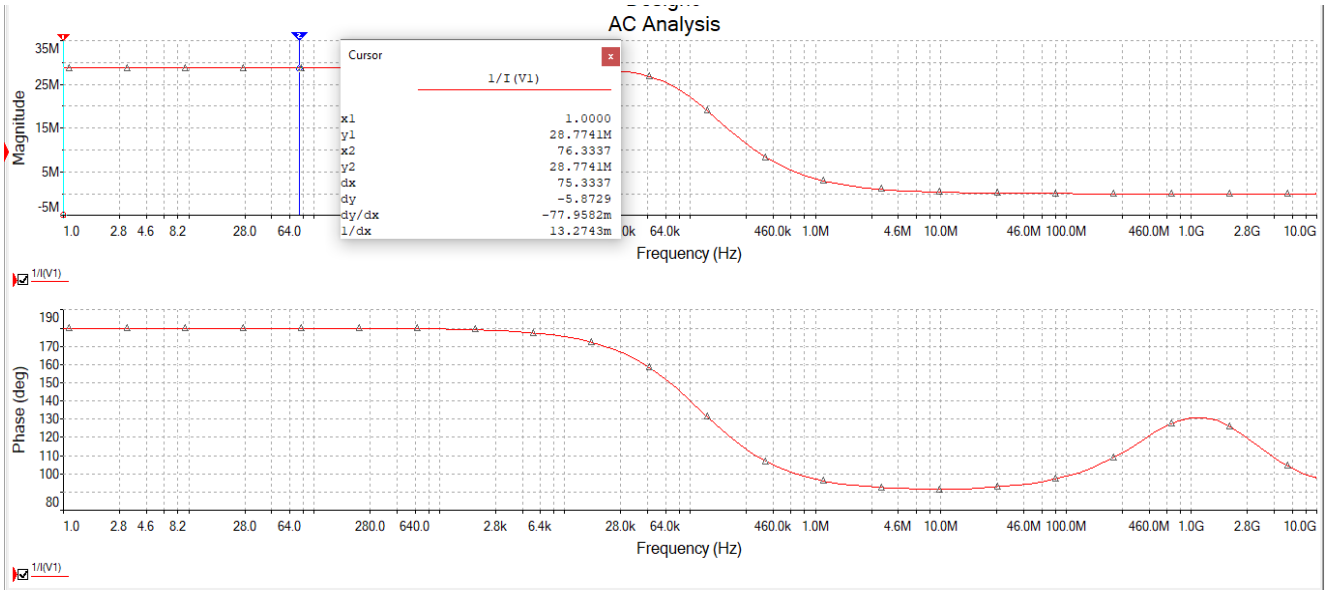
Error=2.65%

If we need to plot the percentage error with Vout ,this is the simulation result:



Figure(26)

We need to determine Rout then we will do AC anaylsis with AC voltage source that the voltage offset of it is more compliance voltage for example (2V) and this the result simulation:

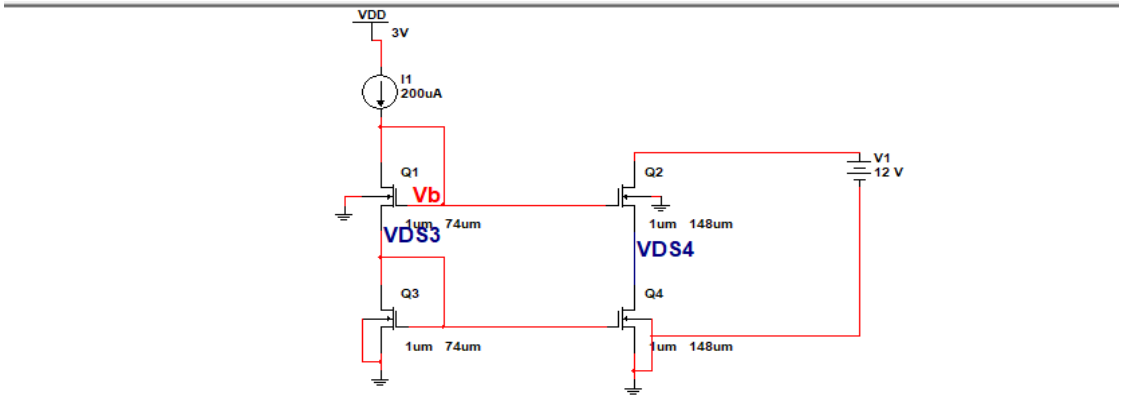


Figure(27)

From simulation result Rout=28.77MΩ

2.Second Case:

I in=200uA & I out=400uA & veff=0.25 V

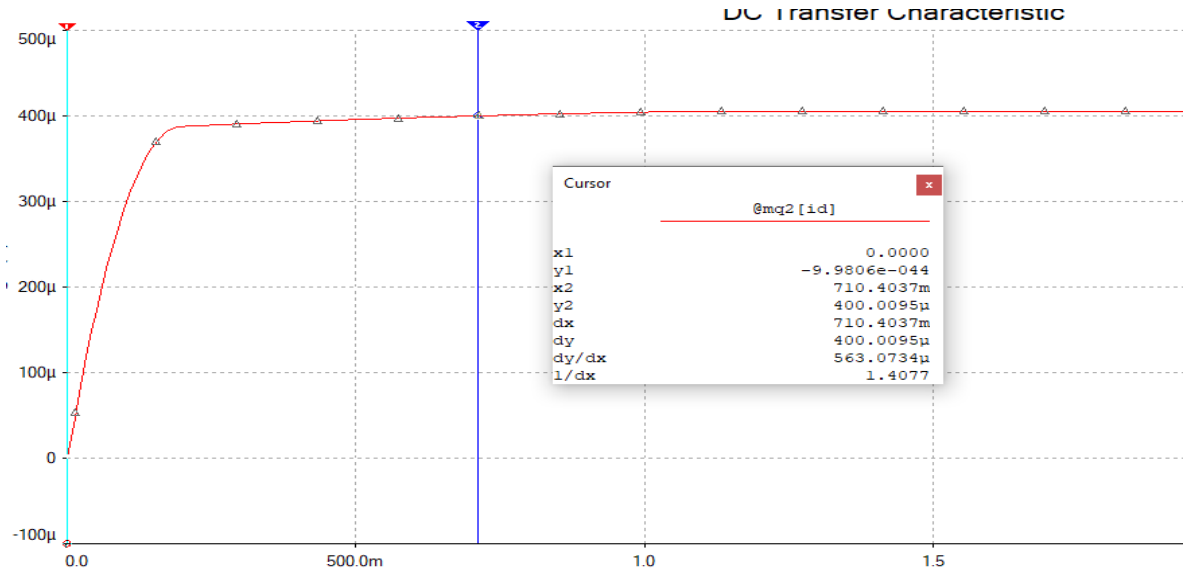


Figure(28)

We will repeat what we did in first case:

For compliance voltage by hand caluclations remains the same:Vcomp=1.3V

Let plot the relation between Iout& Vout to obtain the exact value for compliance voltage tha will be the value for vout at Iout=400uA and this the simulation result:



Figure(29)

We found that Vcomp=0.71V

If we need to know the actual current that Iout will be when M2 enters the sat we put the vout with 1.3V and check DC operating point we found that:

	DC Operating Point	
1	@mq2[id]	405.25000 u

Figure(30)

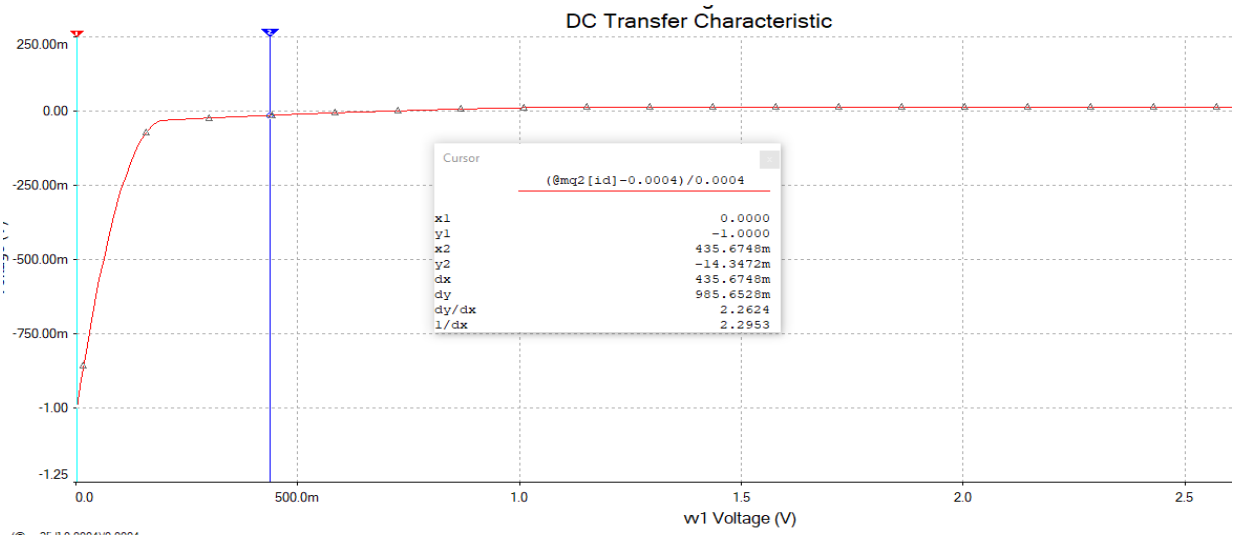
So we found that actual current will be :I actual=405.25000uA

Error=((|I actual – I ideal|)/I ideal)x100

Error=((|405.25000-400|/400)x100

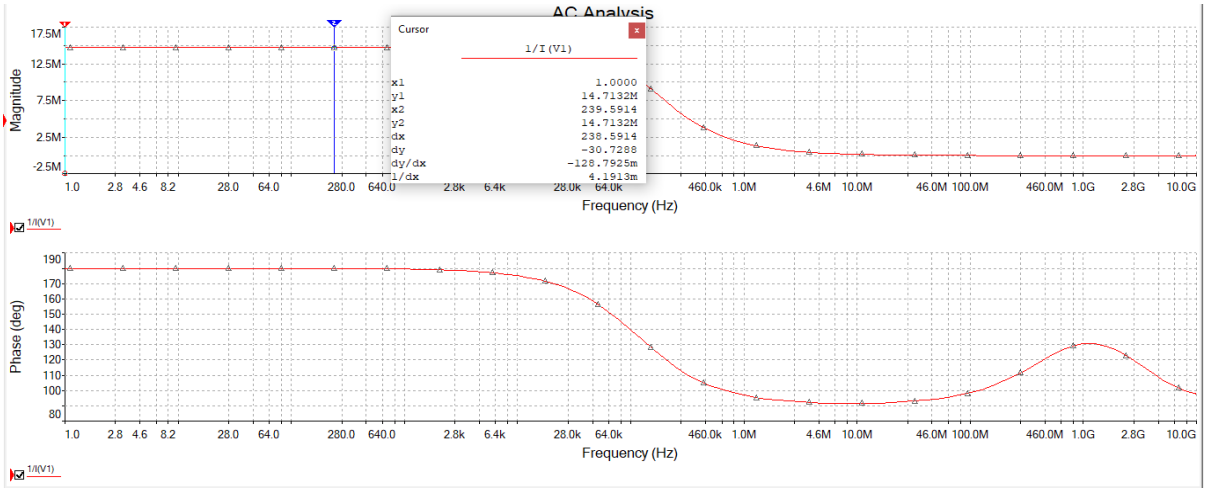
Error=1.3%

If we need to plot the percentage error with Vout ,this is the simulation result:



Figure(31)

We need to determine Rout then we will do AC anaylsis with AC voltage source that the voltage offset of it is more compliance voltage for example (2 V) and this the result simulation:



Figure(32)

From simulation result Rout=14.7MΩ

SUMMARY &CONCLUSTIONS:

1.For simple current mirror:

	Vcomp(hand)	Vcomp(simulation)	Error	Rout
First Case	**0.25 V**	**0.44 V**	**1.3%**	**118 KΩ**
Second Case	**0.25 V**	**0.67 V**	**2.56%**	**60 KΩ**

2.For Cascode Current Mirror:

	Vcomp(hand)	Vcomp(simulation)	Error	Rout
First Case	**1.3V**	**0.64 V**	**2.56%**	**28.7MΩ**
Second Case	**1.3V**	**0.71V**	**1.3%**	**14.7 MΩ**

Disscution of results:

1.In first case (simple current mirror) if we increase the output current the error increases and the Rout .

2.in second case (cascode current mirror) if we increase the output current the error decrease and the Rout.

Q3.differential pair:

Design hand analysis:

*Input linear range≥0.2v

vod=veff1= $\sqrt{(Is/k)}$ ≥0.2 , Is=200µ

We will take veff1=0.2

then k=5*10^{-3} knowing that µcox=3.4*10^{-5} and L=1µ

Then w=150µ

*ADM≥5

$ADM = gm * R \ \ and \ gm = k * veff1 = 1 * 10^{-3}$

So R≥5k

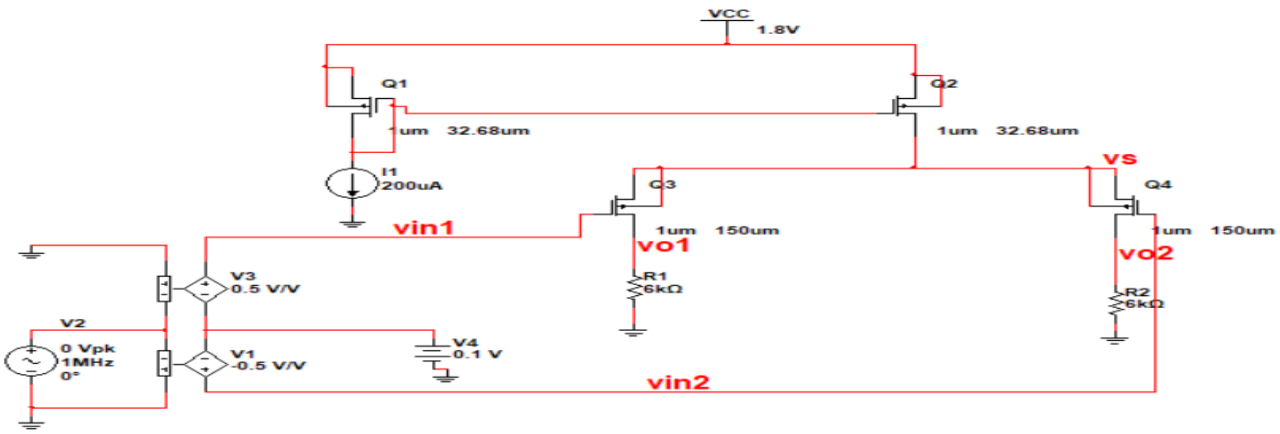
We will tak R=6k

*Differential output swing≥1 vpp

2*(vdd-veff1-veff2)≥1 knowing veff1=0.2v and vdd=1.8v

Veff2≤1.1v we will take it 0.6v

Then k2=1.111*10^{-3} if we let L=1µ then w=32.68µ



Figure(33)

We used a vcvs and gave them same Ac input(differential input) and changed the gain one is 0.5 and the other is -0.5 And the output is raised over DC source(DC common mode).

Input common mode range:

For maxmum value we should make sure that the current mirror is on (M2 in sat)

Vincm max=vdd-vsg1-veff2=1.8-(0.2+0.887)-0.6=0.113v

For minimum value we should make sure that (M1 in sat)

Vincm mini=0.5*Is*R-lvthpl=-0.287v

DC Q-point:

DC Operating Point

	DC Operating Point		
1	@mq3[id]	-94.37275 u	ID for m1
2	@mq1[id]	200.00000 u	ID for m2
3	@mq2[id]	-188.74551 u	ID for m2
4	@mq4[id]	-94.37275 u	ID for m1
5	V(vs)-V(vcc)	-687.69800 m	VDS2
6	V(vcc)-V(vg)-0.887	542.94963 m	Veff2
7	V(vo1)-V(vs)	-546.06548 m	VDS1
8	V(vs)-V(vin1)-0.887	125.30200 m	Veff1

Figure(34)

ID3=ID4=100µ from table 94.37µ

ID2=ID1=200µ from table 188.74µ

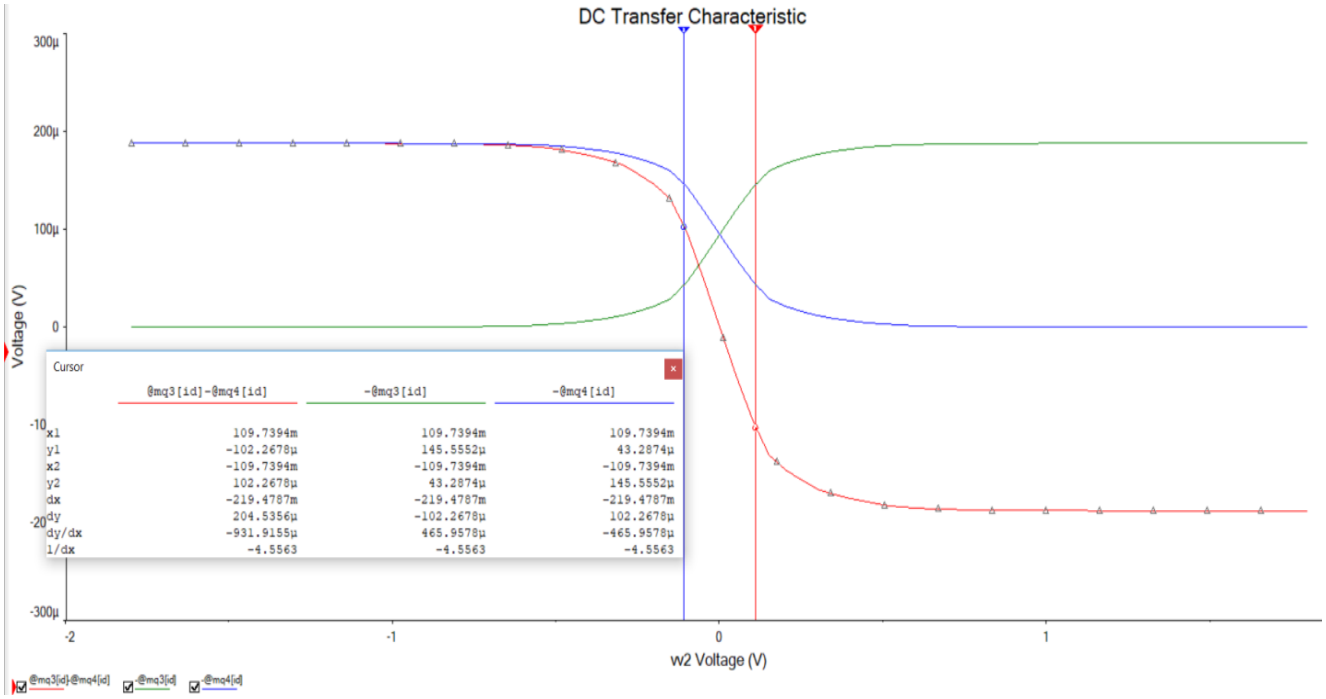
VDS2=VIN+VSG1-VDD=-0.613 from table 0.688

Veff2 from design 0.6 from table 0.543

VDS1=0.5IS*R-(VIN+VSG)=-0.687 from table -0.546

From design 0.2 from table 0.125 big error due to change in current and error in µcox calculation and model error too.

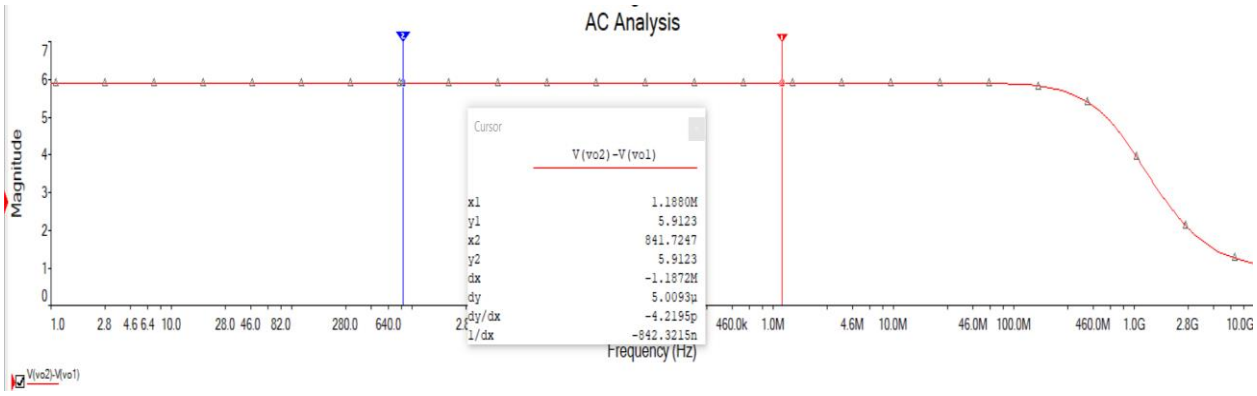
DC sweep for vid:



Figure(35)

We can see that linear input range is higher than 0.2v about 0.22v.

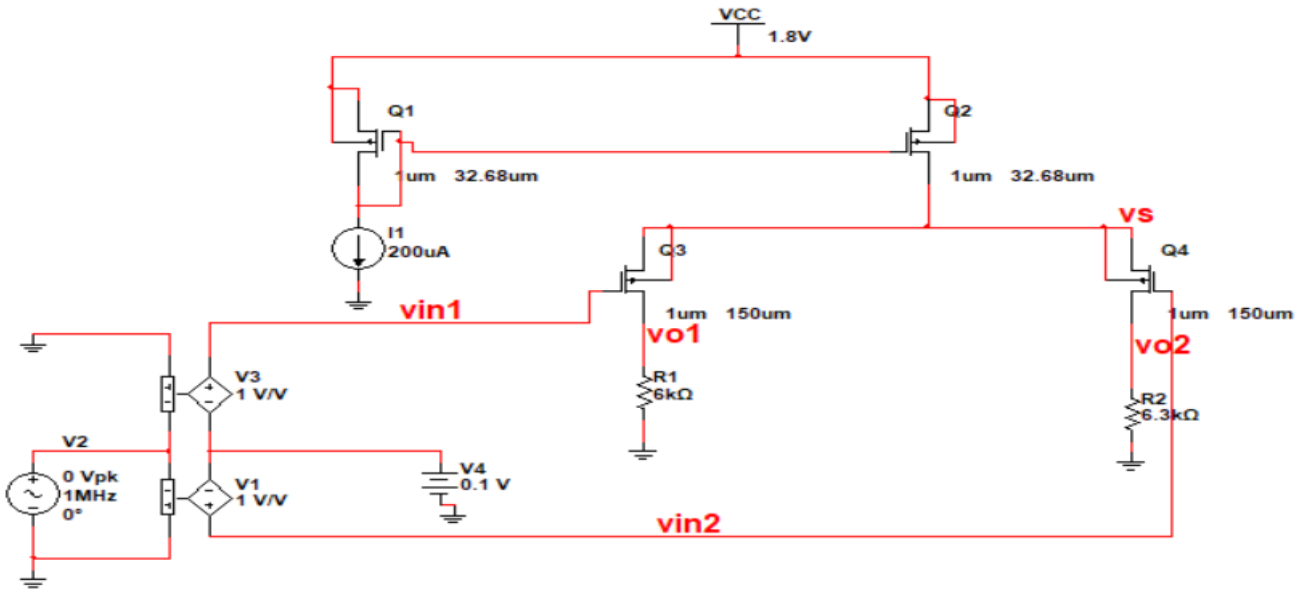
AC analysis for ADM:



Figure(36)

As we see ADM=5.9123 >5

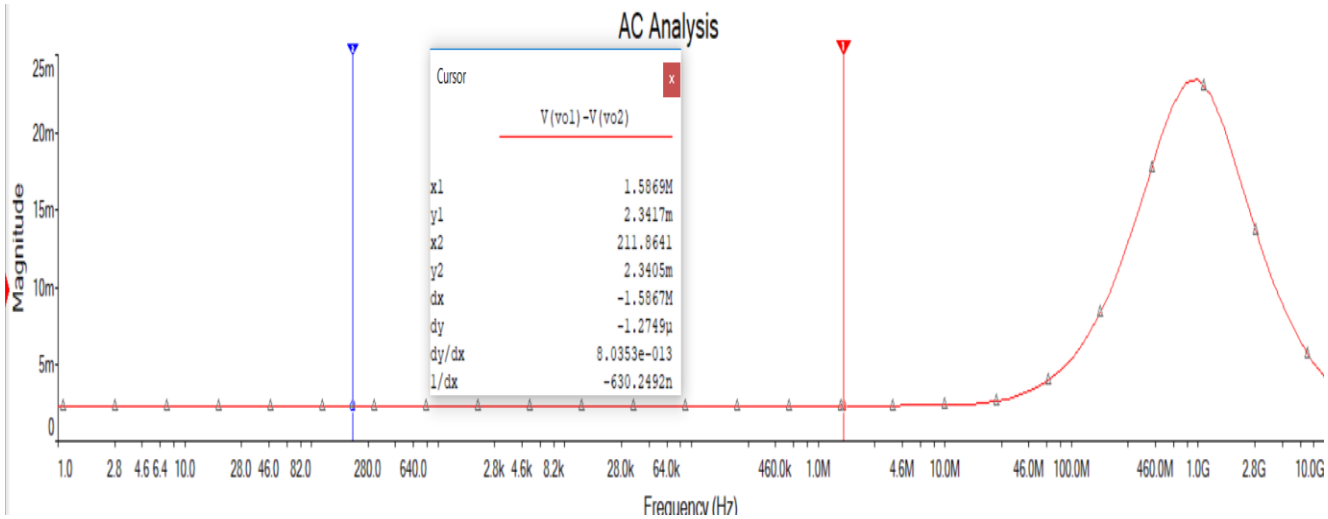
ACM-DM AC analysis:



Figure(37)

We changed the vcvs from (0.5 and -0.5) to(0.5 for both) to be common mode ,and on of the resistors R from 6k to 6.3k(+5%error).

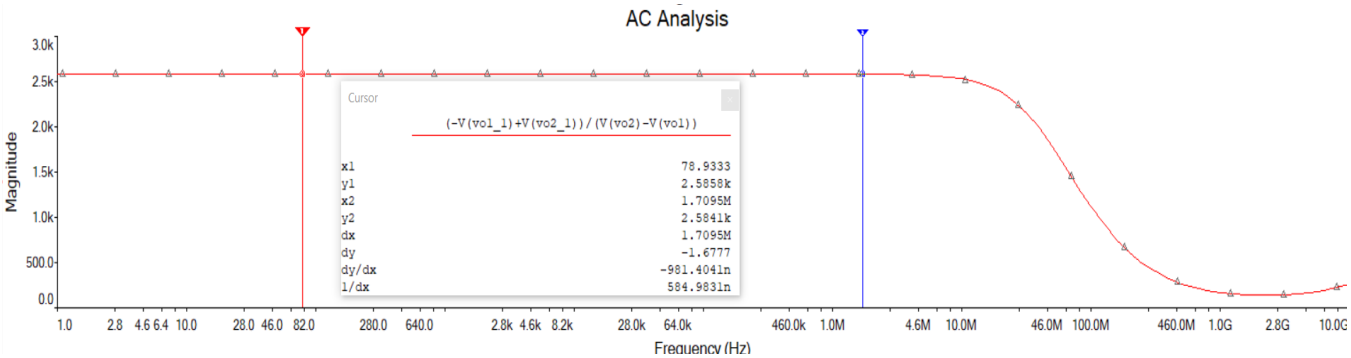
ACM-DM is should be so small=gm ΔR/(1+gm 2 ro2) approximatly equal ΔR/2ro2.



Figure(38)

We get ACM-DM=0.00234 which is small value as we expected.

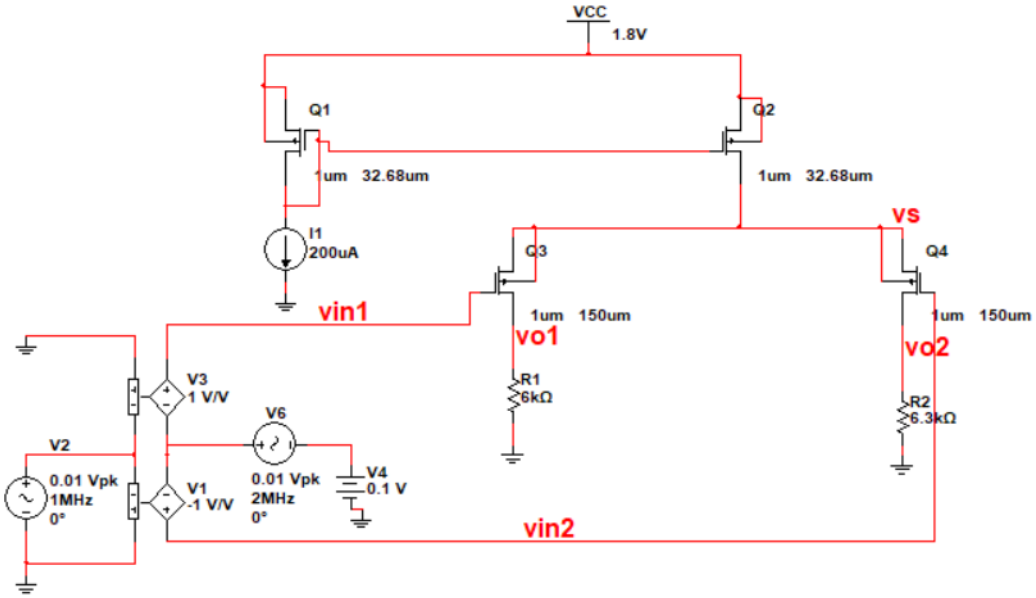
CMRR VS Frequency:



Figure(39)

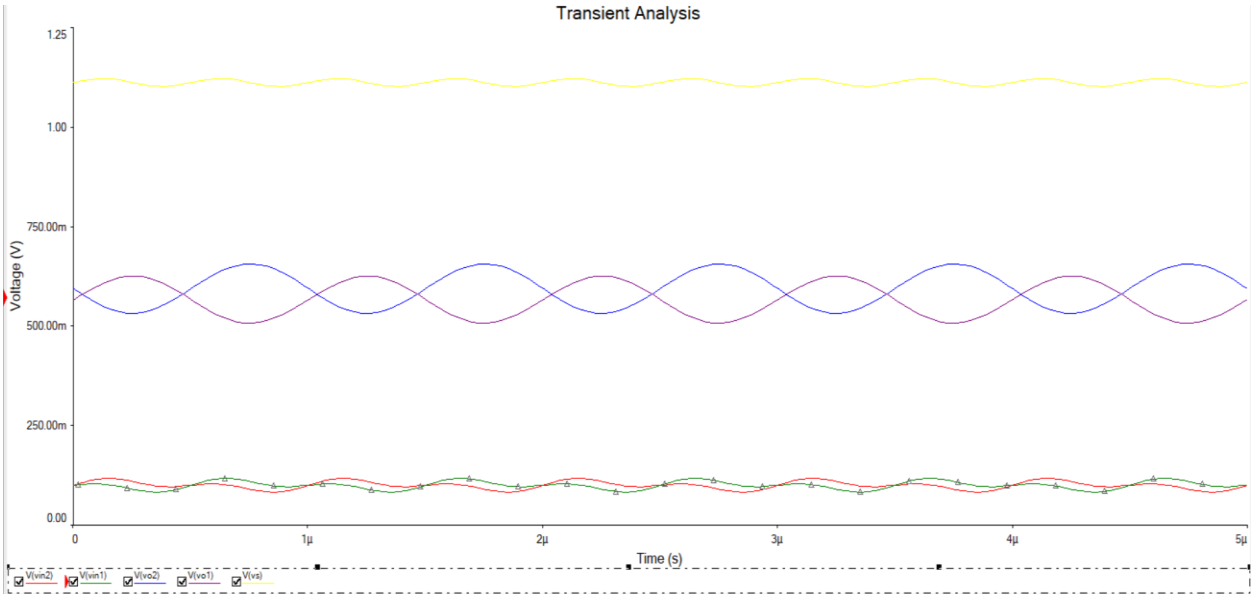
CMRR=ADM/ACM_DM=5.9123/0.00234=2527 near to the value we got and itis high ratio and that is good

Transient analysis:



Figure(40)

We changed vcvs to 1 and -1 and connected the input to as 0.01peak and 1MHZ as differential input and used anthor AC source with 0.01peak and 2MHZ as AC common mode input beside the battary with0.5v which is in range of input as we solved in a (0.115v and - 0.287v) and keep the 5% error in R.

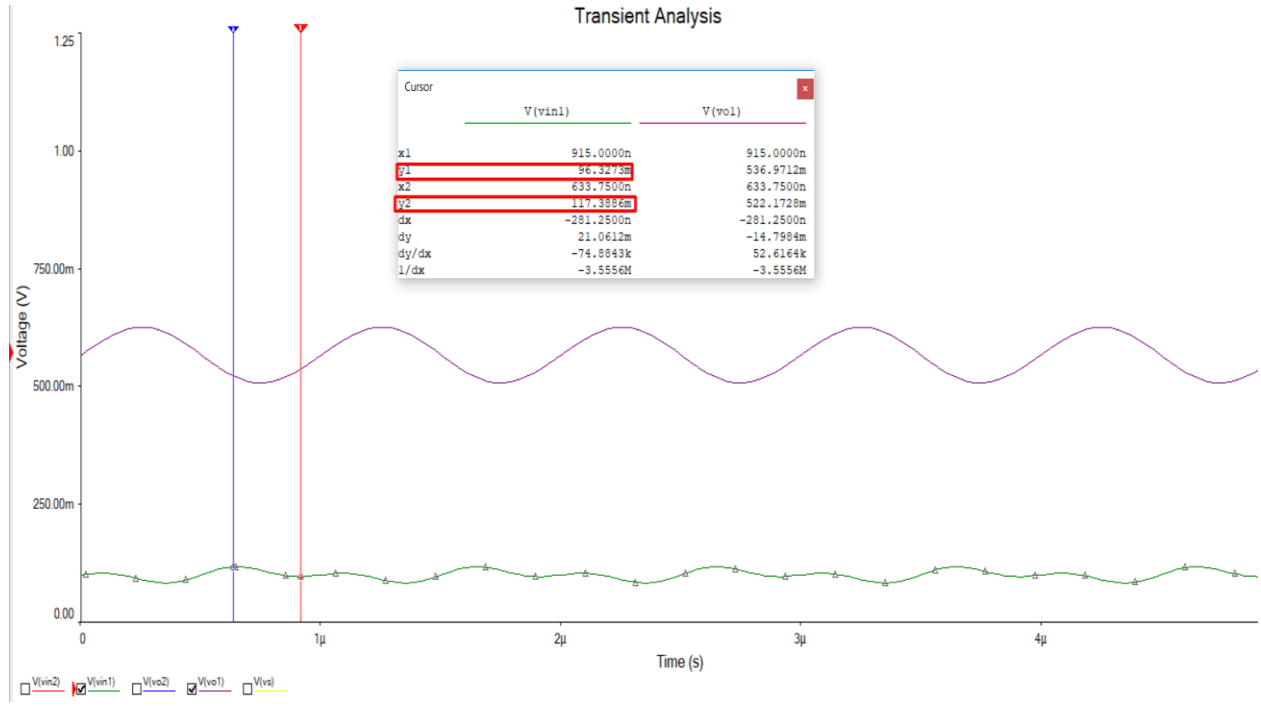


Figure(41)

Comments for transient:

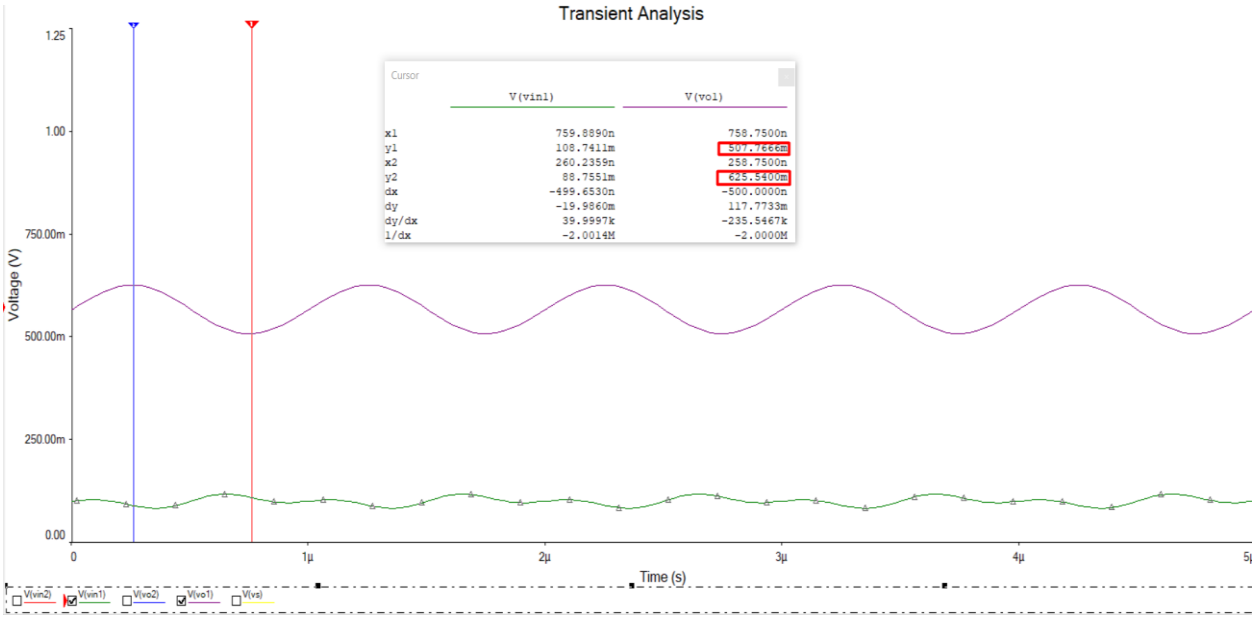
The input is 2 sins with different frequencies and coffients raised on proper dc value =0.1volt , and the output has different frequency from input and have no distortion too .

Gain of vout1/vin1:



Figure(42)

Vin1 amplitude=0.5(maxmum-minimum)=0.5(117.4-96.3)=10.55mv.



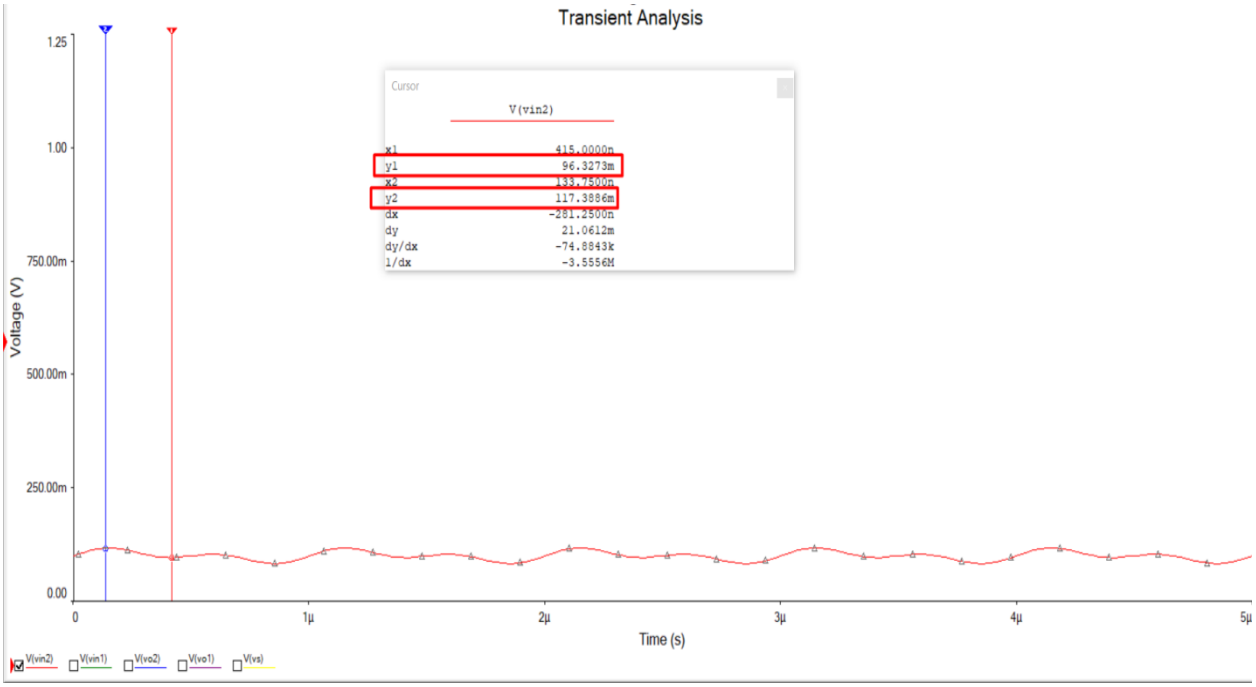
Figure(43)

Vout1 amplitude=0.5(625.5-507.8)=58.85mv

Gain=58.85/10.55=5.578>5

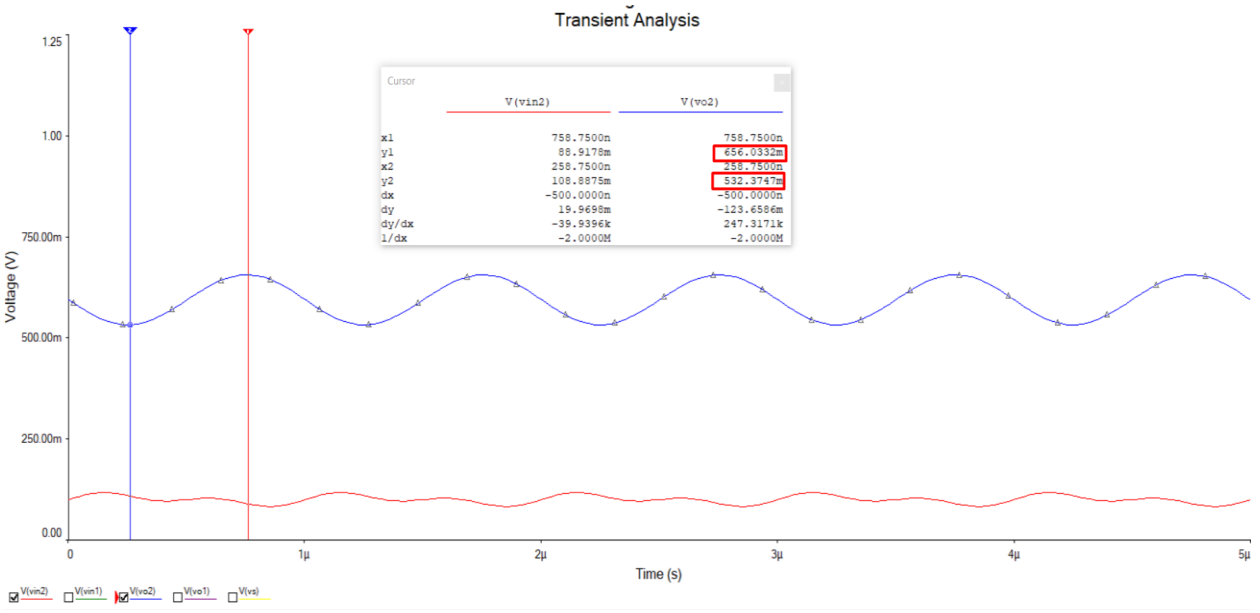
The gain is lower than diffrential gain due to asymmetric R and Acm-dm.

Gain of vout2/vin2:



Figure(44)

Vin amplitude=0.5(117.4-96.3)=10.35mv



Figure(45)

Vout amplitude=0.5(656-532.4)=61.8mv

Gain=61.8/10.35=5.971 higher than previous gain due to asymmetric in R

Vp :

Vp is high because it has DC value equal nearly vdd-veff2=1.2 approximatly and added to it the AC value

Summary of Result:

Design result:

Transistor	current	veff	W/L
M1	100µ	0.2	150
M2	200µ	0.6	32.7
R=6K			
Input common mode range (0.113 to -0.287)			

Simulation results:

Input linear range	0.22volt
ADM	5.97
ACM-DM	0.0023
CMRR	2530