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ELECTRONICS & ELECTRICAL
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CAIRO
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Electronics 201

Project

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Problem 1

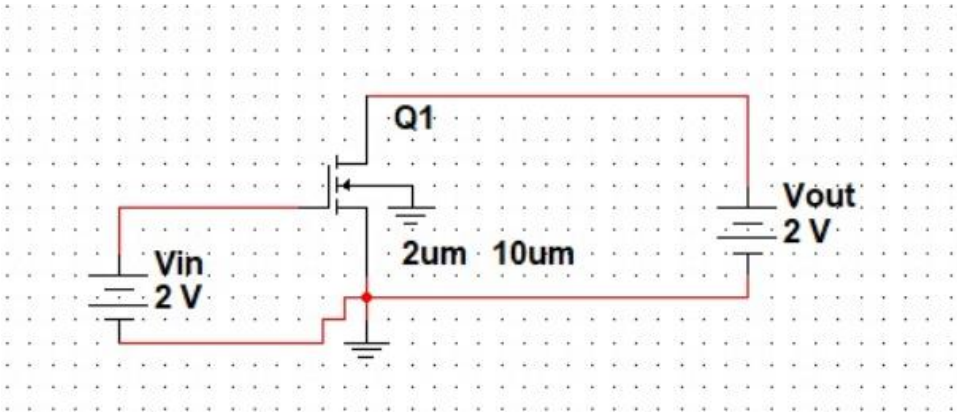


Fig 1.1

Design Procedure & Simulation results

The relation between Ids and Vgs

For the Enhancement MOSFET shown in figure (2.1), we let Vgs=Vin and Vds=Vout (we notice that Vs =0).By fixing the drain-to-source voltage (Vout) to 2v.Then by plotting the relation between Ids and Vin which is

$$I_{ds} = \mu_n C_{ox} \frac{w}{L}((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^{\ 2}}{2})$$

we get the curve in figure (2.2) Then we can easily get the threshold voltage Vth

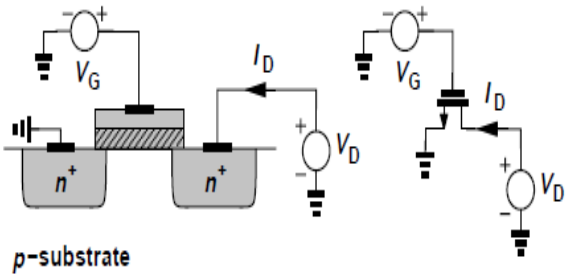


figure 2.1 NMOS transistor

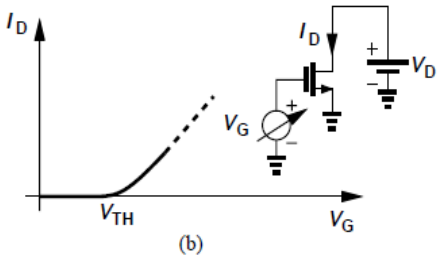
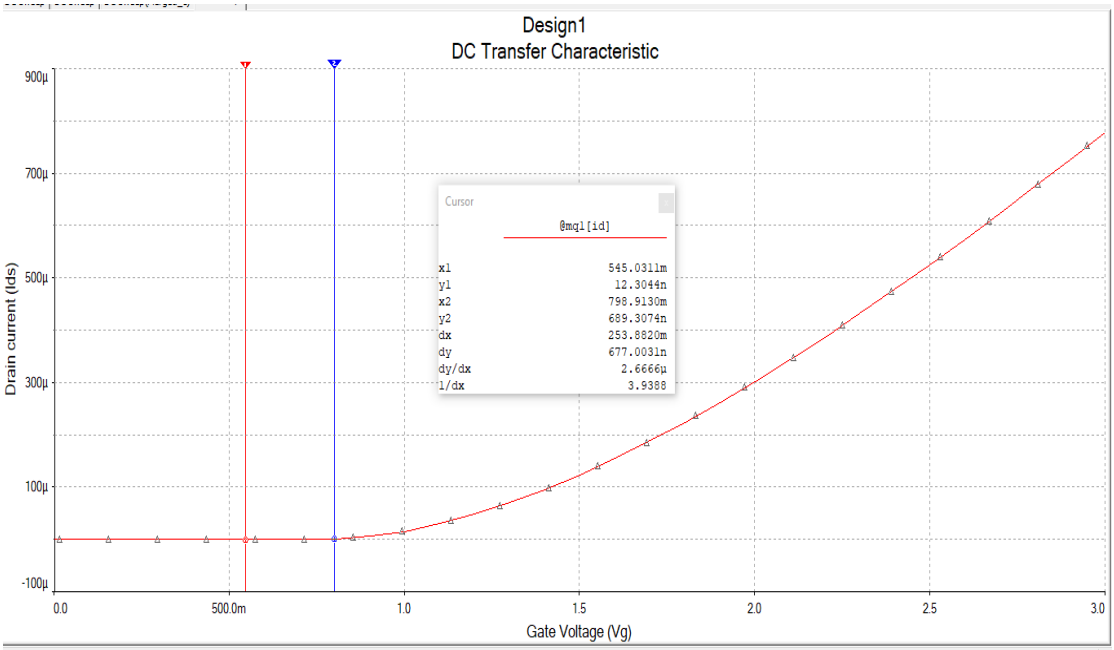


figure 2.2 Vg – Id relation

After simulation on MULTISIM we found that Vth = 0.798 volts



simulation figure

The relation between Ids and Vds

By making Vgs = 2v and plotting the relation between Ids and Vds as illustrated in figure 2.3 . We get the curve shown in figure 2.4 which we will use to calculate and MnCox and λ

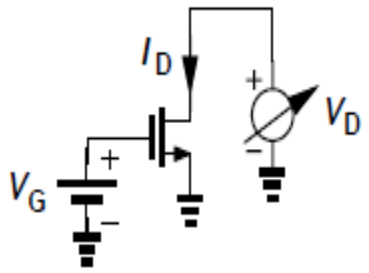


figure 2.4

Vds - Ids curve

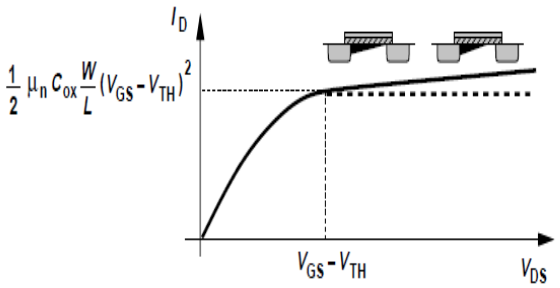


figure 2.3

NMOS with Vg = 2v

Calculating the quantity $\mu_n C_{ox}$

$$I_{ds} \approx \mu_n C_{ox} \frac{w}{L}(V_{gs} - V_{th})V_{ds}$$

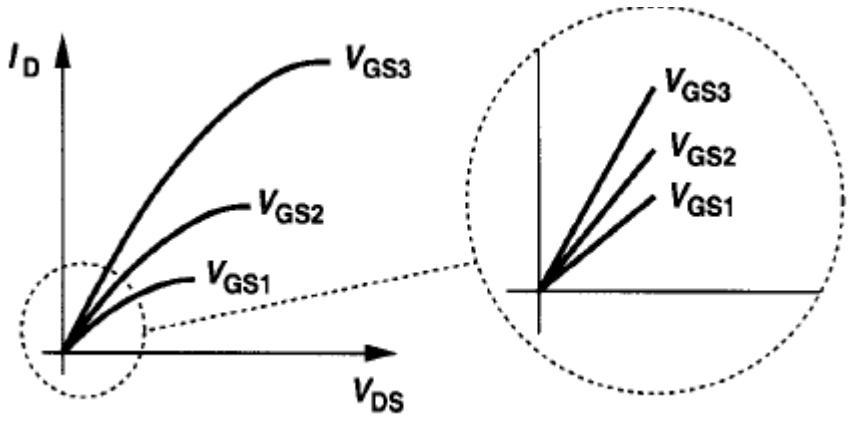


figure 2.5

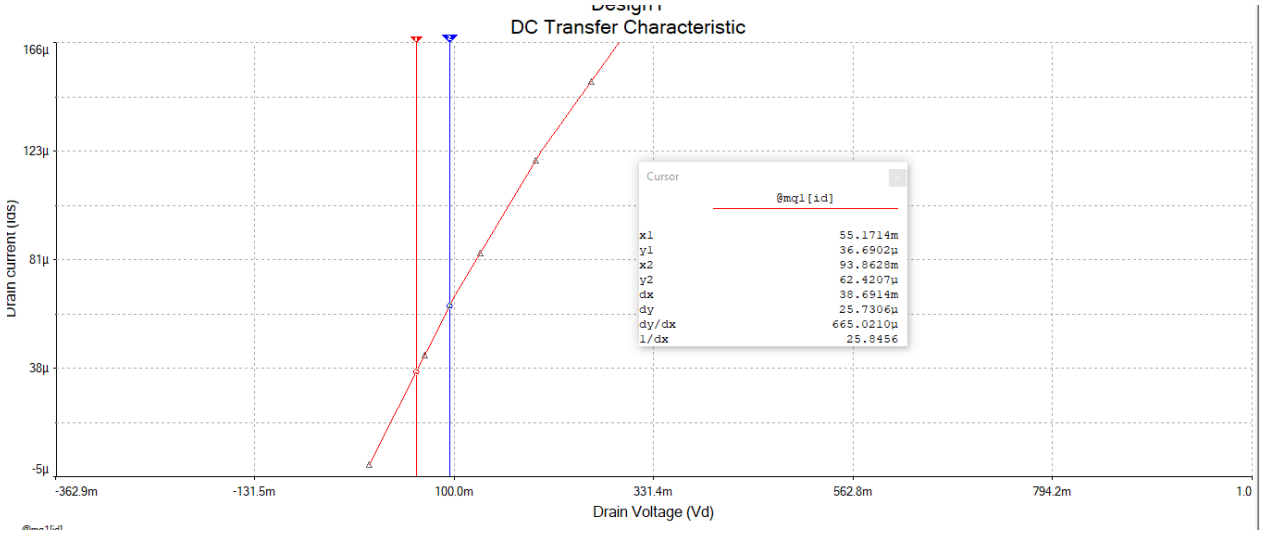
Deep linear (Triode Region)

By differentiating Ids w.r.t Vds we get the conductance (g)

$$g_0 = \frac{\partial I_{ds}}{\partial V_{ds}} = \mu_n C_{ox} \frac{w}{L}(V_{gs} - V_{th})$$

by getting the slope in the deep triode region (where Vds < 0.1v)

$$g_0 \approx 665.02 \times 10^{-6} \Omega^{-1}$$



after that we can get $\mu_n C_{ox}$ substituting with W/L=5 and Vgs-Vth = 1.2 v

$$\mu_n C_{ox} = 1.11 \times 10^{-4}$$

Then we calculate Ids at the edge of saturation from this relation

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$$

then Id = 3.996 x 10^(-4) Ampere

In saturation region we find that there is the channel length modulation effect appears and we Ids relation takes the form

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}),$$

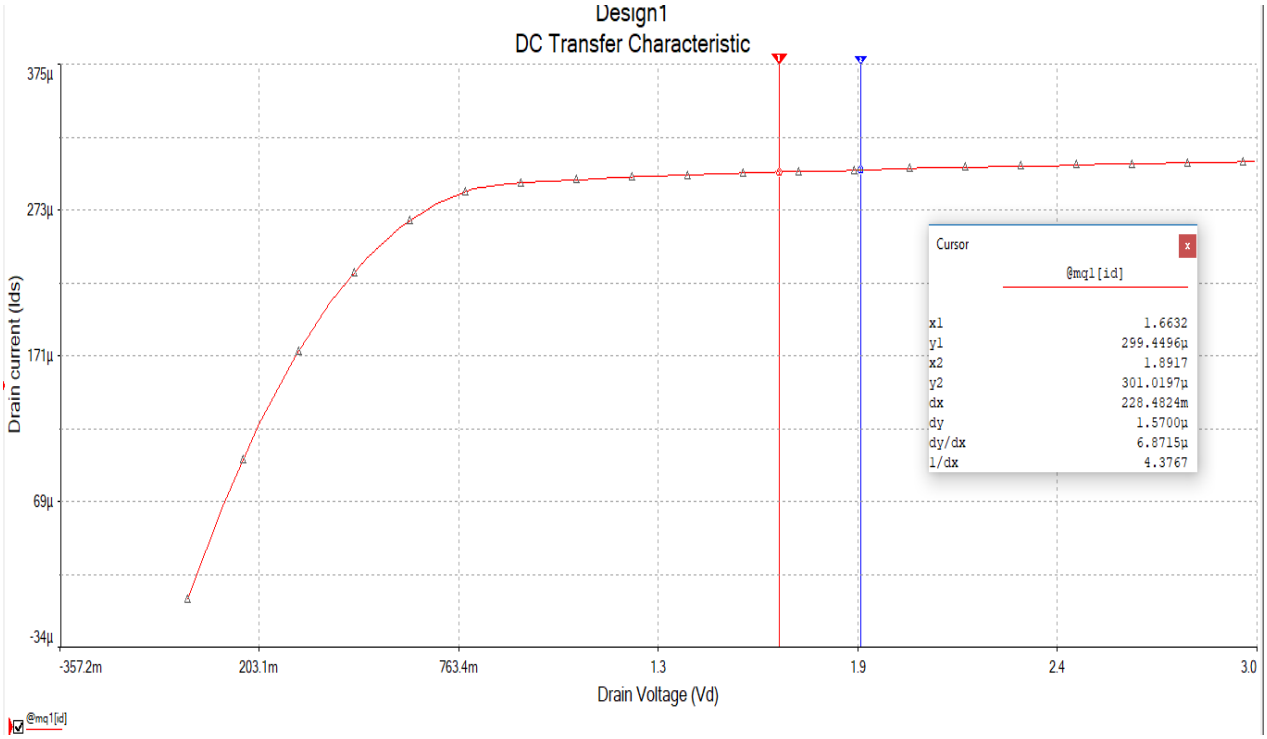
The slope of this curve gives us 1/Rds and then we can calculate λ from the following relation

$$\lambda \approx \frac{1}{R_{ds} I_{ds}}$$

from simulation figure (3) we find that the slope

$$\frac{\partial I_{ds}}{\partial V_{ds}} = \frac{1}{R_{ds}} = 6.871 \times 10^{-6} \Omega^{-1}$$

$$\lambda \approx \frac{1}{R_{ds} I_{ds}} = \frac{6.871 \times 10^{-6}}{3.996 \times 10^{-4}} = 0.0172 V^{-1}$$



simulation figure 3

Discussion of Results and calculations

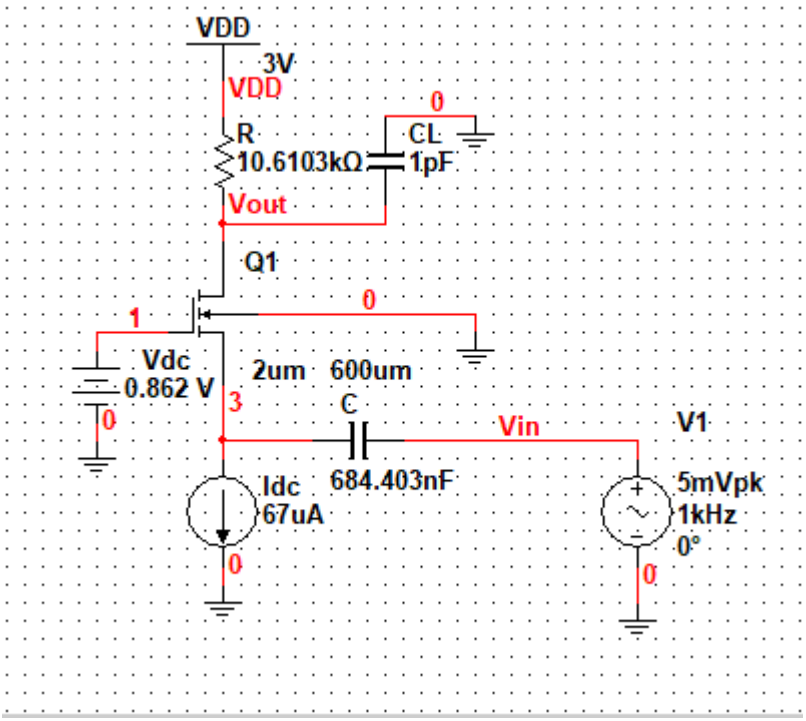
We notice that Vth = 0.798 volts which is so close to typical values of threshold voltage. We also noticed that

$$\lambda \approx \frac{1}{R_{ds} I_{ds}} = \frac{6.871 \times 10^{-6}}{3.996 \times 10^{-4}} = 0.0172 V^{-1}$$

which is also in the range of typical values of λ 0.005 to 0.02

Problem 2

Schematic diagram



First from solving the above figure, we begin to deduce a series of equations to represent boundaries of the design

Assume we take some values from problem 1

$$\mu_n C_{ox} = 1.11 \times 10^{-4}$$

Vth = 0.8 v

Design corners

a) First from AC analysis

1) We begin by solving to get R = R_d given WH = 15MHz.

$$R_d = \frac{WH}{C_L}$$

$R_d = 10.6103\ kohm$

2) Then we begin to get relations between the other parameters. We get an expression for mid band voltage gain A_v.

$$A_v = gm \times R_d \quad @\ A_v \geq 19.9526$$

From above we can deduce a minimum value for gm

$$gm \geq \frac{A_v}{R_d} \geq 1.88055\ mA/V$$

3) Then we try to get expression for WL.

$$WL = \frac{gm}{C_{in}} = 500\text{Hz}$$

$C_{in} \geq 598.6\ nFarad$

B) from DC analysis we get the following.

4) For the circuit to remain in saturation $V_d \geq V_g - V_{th}$
Where $V_{gs} - V_{th} = V_{eff}$
From givens $I_{DC} \leq 100\ uA$.

$$V_d = 3 - I_{DC} \times R_d$$

Then by substituting from above:

V_{eff} =0.0643volts

5) Getting a relation between gm and I_{DC}.

$$\text{Gm} = \sqrt{2 \times \mu n\, cox\, \frac{w}{l} \times I_{DC}}$$

At minimum gm we can get a relation between $I_{DC}\ and\ \frac{w}{l}$.

$$\sqrt{\frac{w}{l}\ I_{DC}}_{min} = 0.1293368$$

Trials:

Assume $I_{DC} = 67\ \mu A$ and $\frac{w}{l} = 300$ (we are above minimum values so it's ok !)

Then gm = 2.15 mA/V

$C_{in} = 684.403\ nF$

Then we get the gm from simulation where gm = 2.14208

Where the error = 0.374%

$V_{eff} = 43.194\ mV$

$V_{ds} = 2.27\ V$

$V_{Dc} = 0.862\ V$

1) DC operating point (**I_D=67uA, V_{DS}= 2.27volts, V_{eff}=43.19480mV), and V_{DC}=843.19mV**)
gm = 2.14208 mA/V (So close to the calculated gm with an error below 1%)

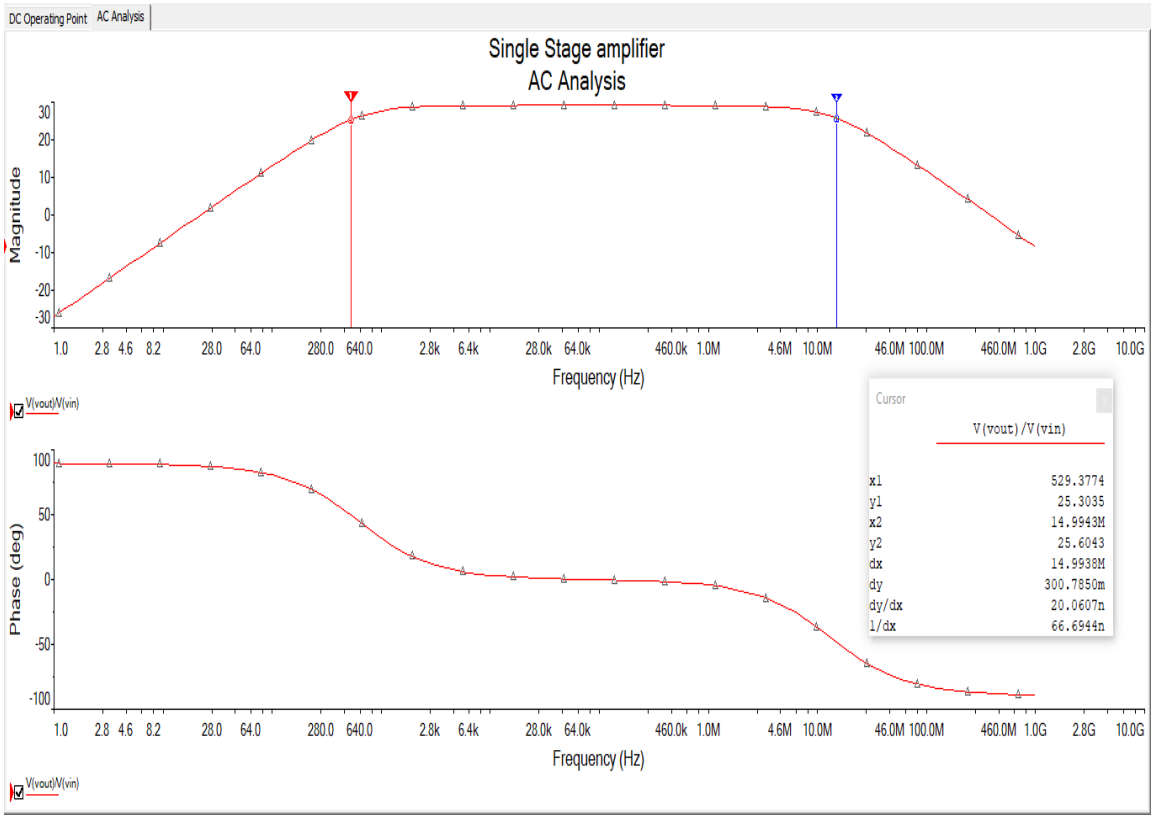
Gm as shown in the figure below.

DC Operating Point

Single Stage amplifier
DC Operating Point

	DC Operating Point	
1	@mq1[gm]	2.14208 m
2	@mq1[id]	67.00002 u
3	@mq1[rds]	0.00000
4	I(IDC)	67.00000 u
5	@mq1[vgs]	843.19480 m
6	@mq1[vds]	2.27000

b) **AC analysis frequency response at 1GHz**.

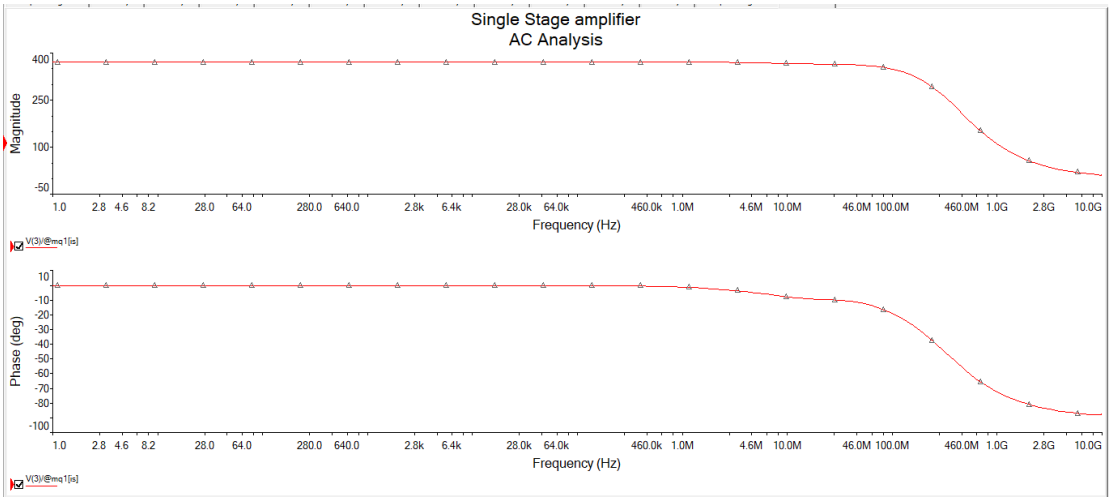


Average gain is about 28 db which satisfies the condition Av >= 26 db

(There is a small error in F(low) (about 4%) due to the neglection of r0 and other assumptions and approximations

c) **Rin and Rout**

To get Rin we put a Coupling capacitor (C=1mF) after The input signal To ensure that we are in the bias point at high frequencies then we get it from Multisim using the expression (Vin/Iin) where Vin is the Voltage at the node after this input capacitor (C=1F) to neglect its effect at low frequency which makes Rin at low frequency very large



The AC analysis R_{in} vs frequency up to 10 GHz

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a)Rin = 1/ gm =370.7371 ohms

Note: At high frequencies (above 1 Ghz) parasitic capacitors will shunt Rin to zero

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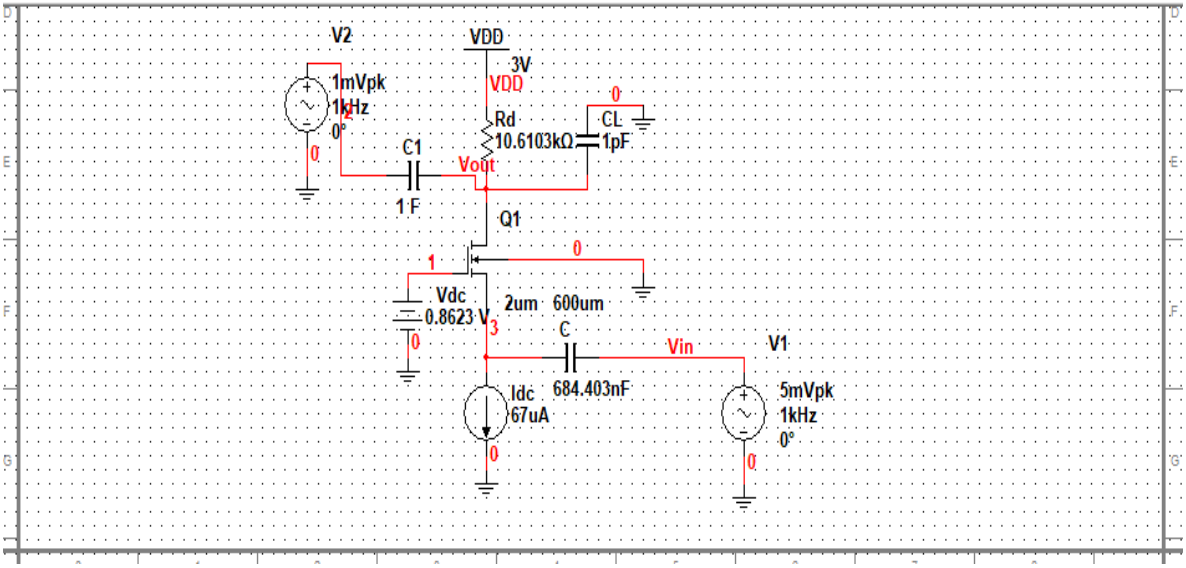
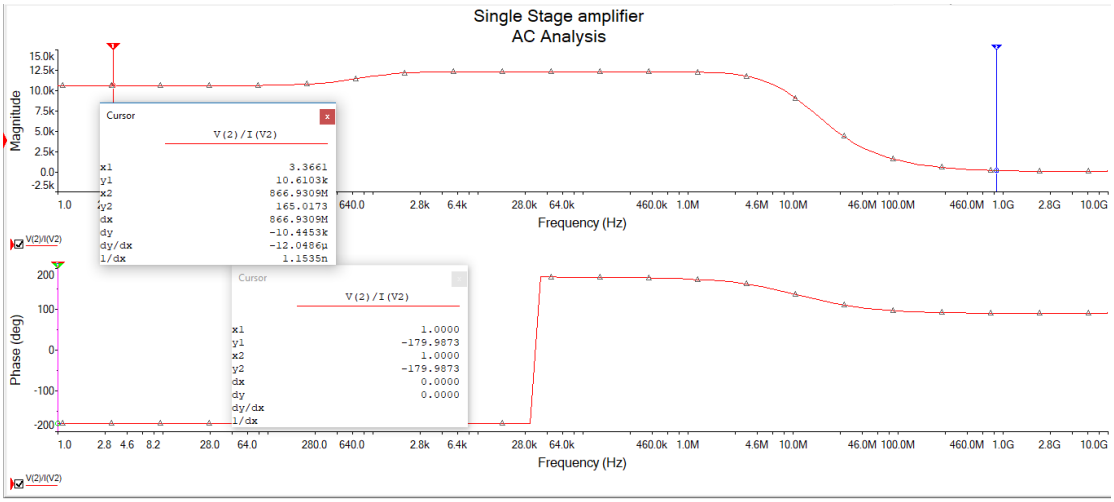
- To get Rout we put a capacitor (C=1F) in series with an AC voltage source and get Rout from the expression (Vx/Ix=Rout) The following figure shows the circuit after this modification



4)The AC analysis R_{out} vs frequency up to 10 GHz



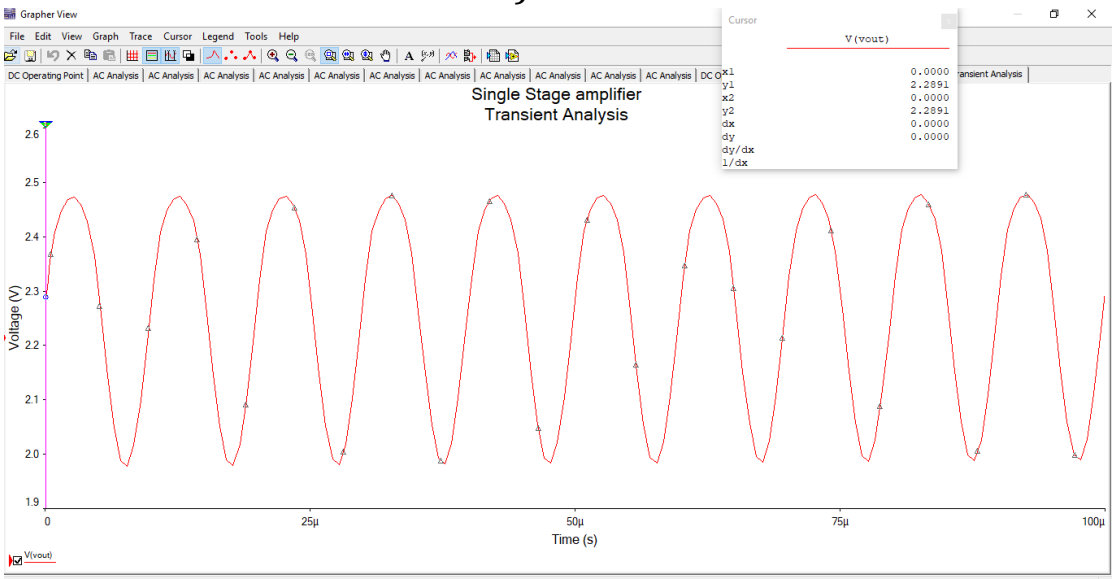
Rout = Rd = 10.6103 Kohms

At High frequencies parasitic caps and **CL** will shunt Rout to zero , that is , it these capacitors will make short circuit in parallel to R out and Rin that will shunt them

Transient analysis with Vin=A.sin(2πft)

When **A=10 mV and f=100 kHz**(which means that we are in mid - band so that Av = mid-band gain (about 20 in linear

scale and 28 in decibel scale)

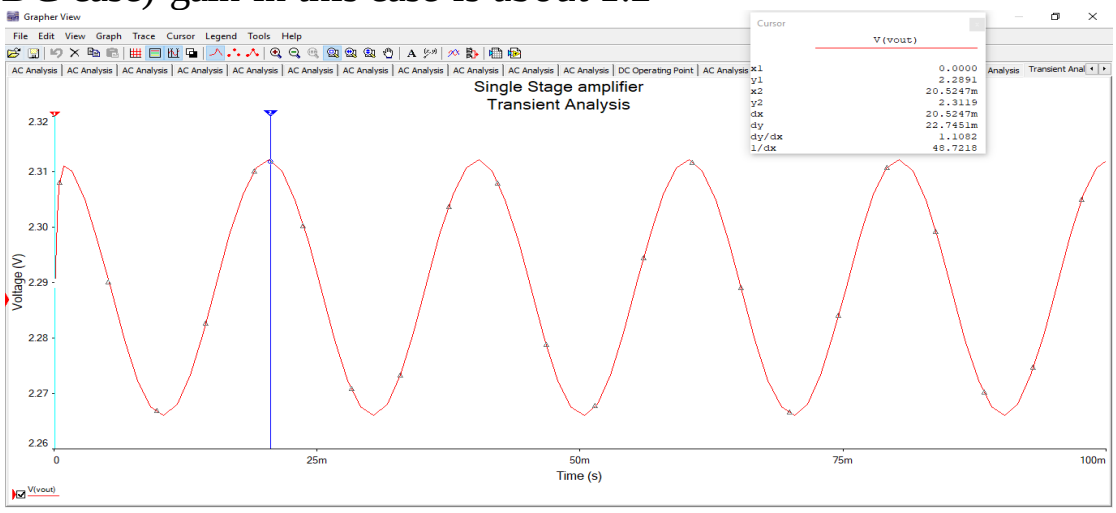


This shows the DC + AC components of Vout , we note that the amplitude of Vout is 200 mV as the average gain is about 20 and the input signal is 10 mV

-The Dc component from DC analysis = 2.27 volts which shifts up the output curve by this offset

transient analysis at $F = 50\ Hz$

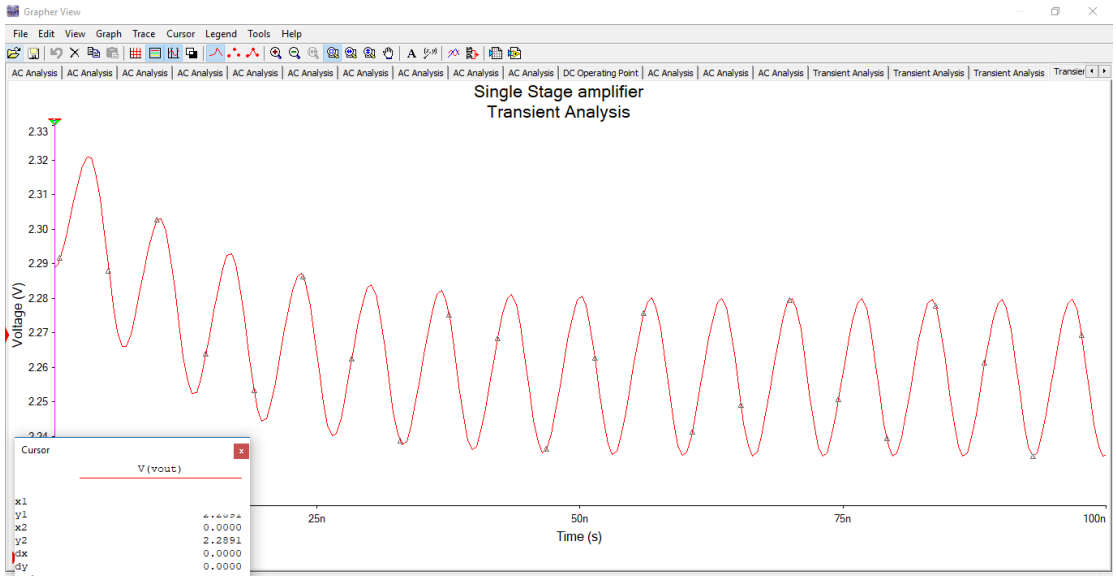
(which means that we are in low frequency that approximates to DC case) gain in this case is about 1.2



We note that the frequency is so low that the Ac components is negligible with respect to the DC component.(RECALL That Vd=2.27 volts)

transient analysis with F = 150 MHz

(here we use high frequency gain which is also so small because of the parasitic capacitors effect . The Ac signal has a small impact and the DC component dominates here as in the (F=50hz) case



Design summary

Parameter	Value
Power	P=Vdd*Ids=201 microwatts
gm	2.15 mA/V
B.W	14.9995 Mhz
Mid-band gain	28 DB (average)
Veff	0.0682 volts
Rin	1/gm = 370 ohms
Rout	Rd = 10.6103 Kohms
Cin	684.403 nF
Idc	67 uA
Vd (DC component)	2.27 volts