Cairo University
Faculty of Engineering
Electronics & Comm. Dept.

ELC201B
Year 2019/20
May 2020

2-Stage Op-amp Design

Please read carefully before starting:

- Simulation tool to be used is National Instruments (NI) Multisim.
- The setup of the NMOS and PMOS transistors and their models are given at the end of the document.
- **Maximum no. of students per group is 2.**
- You are required to deliver a soft copy report that contains:
    1. Design procedure (hand calculations)
    2. Schematic diagrams (snapshots from Multisim showing dimensions and values)
    3. Simulation results (snapshots from Multisim)
    4. Discussion of your results and conclusions
- The deadline to submit the project on google classroom is **June 6th, 2020**.
- Any identical/copied reports will be given zero.

Project description:

Design the 2-stage op-amp shown in Fig.1. to have zero systematic offset and achieve the specifications listed in table I. The amplifier is supposed to provide 80dB of gain, and consume 1mW of DC power while operating from a 3.3V supply. Design the op-amp to operate properly for a maximum input common mode voltage of 3V, and a minimum output voltage of 0.2V. You can ignore the compensation of the op-amp (Ccomp). Assume that the bias current I_{BIAS}=100uA.

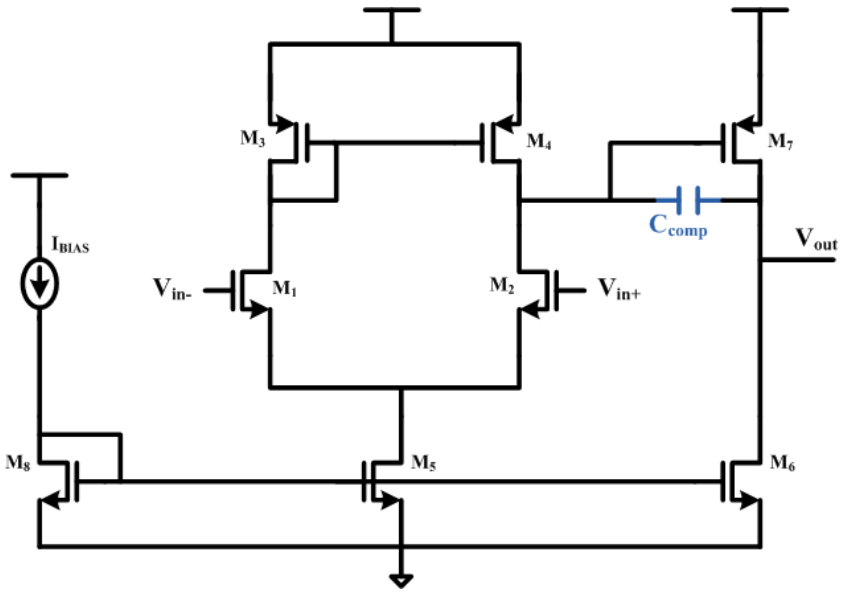


Fig. 1: 2-stage Opamp Schematic

Include in your report the hand analysis used to design the 2-stage op-amp showing:

- how you choose the device sizes (M1-M8), bias point, gm, ro
- how did you choose the gain per stage A_{v1} and A_{v2}
- Op-amp input referred thermal noise
- Op-amp CMRR (common mode rejection ratio)

Also **include plots of all the simulation results** supporting the specs that were achieved and **summarize them in table I**, i.e. include simulations for the differential gain, CMRR, and input referred noise versus frequency.

Table I: Op-amp specs. & simulation results

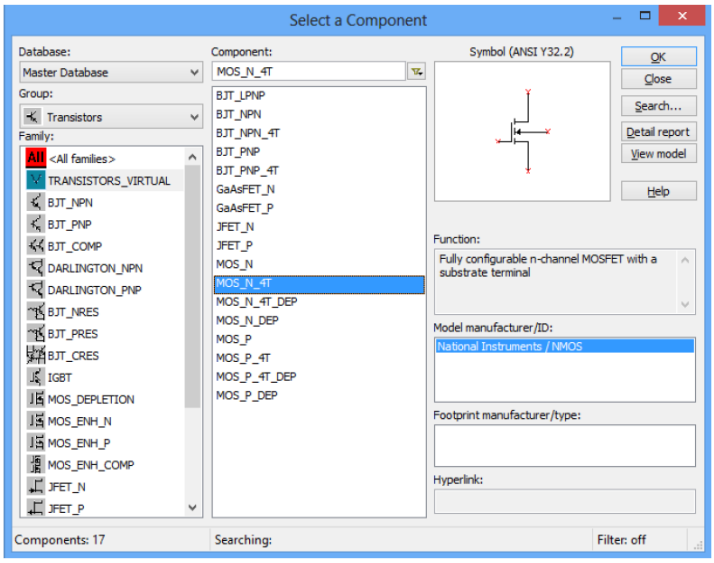
Spec.	Target	Sim. results	Units	Comment
Differential mode gain	80		dB	
Common mode gain	--		dB	
CMRR	>60		dB	
Open Loop 3dB BW	>500		MHz	
Input referred noise	<7		nV/√Hz	**Hint:** simulate the output referred noise then divide by the differential mode gain
Supply voltage	3.3		V	
Max Input common mode	3		V	
Min input common mode voltage	--		V	
Max output voltage	--		V	
Min output voltage	0.2		V	
Power consumption	1		mW	Assume the power is equally distributed between stage 1 and stage 2. Neglect the power consumption due to the bias branch (I_{BIAS})

Notes:

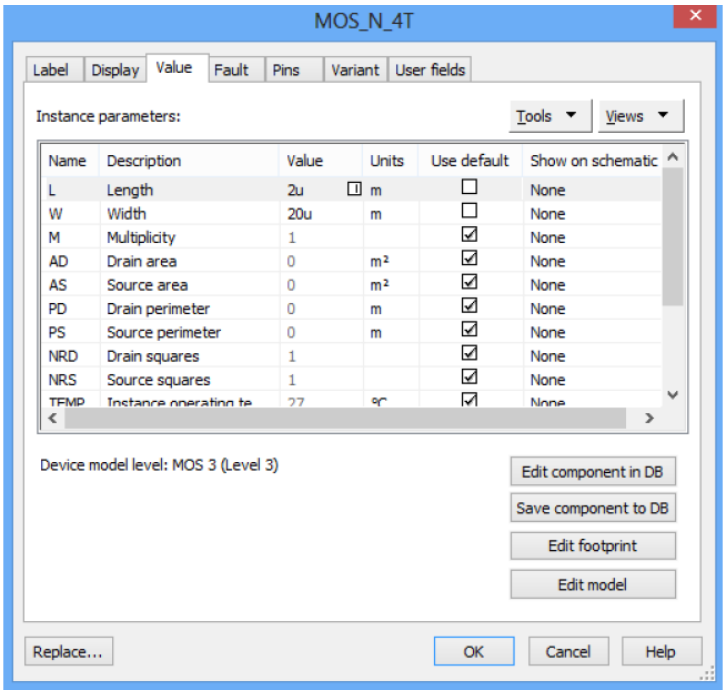
- Any quantity identified in the spec table by "—" is left for your choice
- The Simulation column on the table should be filled based on your simulation results
- For the hand analysis consider only thermal noise, and you can use the following process parameters: V_{TN}=0.8 V, $|V_{TP}|$=0.9 V, $\mu_n C_{ox}$=120 μA/V^2, $\mu_p C_{ox}$=40 μA/V^2, λ_n =0.04 V^{-1}, λ_p=0.065V^{-1}, Boltzmann constant k=1.38x10^{-23} J/K, T=300^o K, γ=1.
- You can use minimum length for all the transistors (1 μm)

Setup of the NMOS and PMOS transistors:

Choose an NMOS_4T from the menu of Place → Component (as shown below) and place it in your schematic.

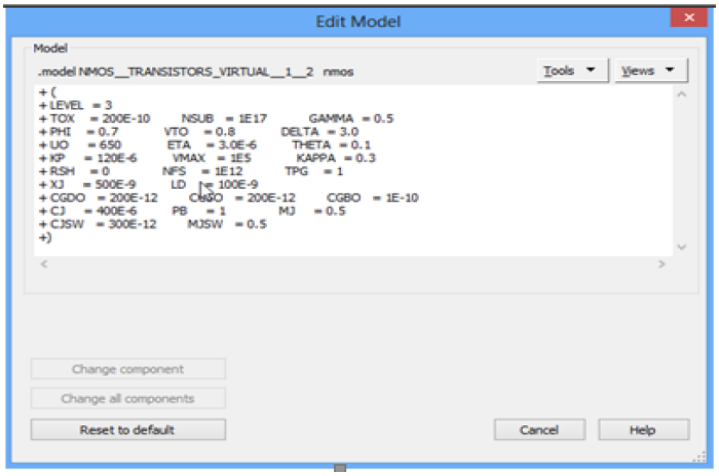


Double click on the transistor and choose the tab of "Value". This is where you can change the dimensions (W,L) of the transistor.



Click on the "Edit model" button.

Copy and paste the model of the NMOS (as shown) in the "SPICE view" Make sure to click on the "Change component" button to save changes.



If you need to place another transistor in a schematic, copy the transistor that you have just created to get the correct model and you can then change the dimensions. Repeat the same for the PMOS transistor (MOS_P_4T).

Minimum length of any transistor is 1 µm. The bulk of an NMOS device should be connected to lowest voltage (ground) and that of a PMOS device should be connected to the highest voltage (V_{DD}).

NMOS:

```
+ (
+ LEVEL = 3
+ TOX = 200E-10 NSUB = 1E17 GAMMA = 0.5
+ PHI = 0.7 VTO = 0.8 DELTA = 3.0
+ UO = 650 ETA = 3.0E-6 THETA = 0.1
+ KP = 120E-6 VMAX = 1E5 KAPPA = 0.3
+ RSH = 0 NFS = 1E12 TPG = 1
+ XJ = 500E-9 LD = 100E-9
+ CGDO = 200E-12 CGSO = 200E-12 CGBO = 1E-10
+ CJ = 400E-6 PB = 1 MJ = 0.5
+ CJSW = 300E-12 MJSW = 0.5
+)
```

PMOS:

```
+ (
+ LEVEL = 3
+ TOX = 200E-10 NSUB = 1E17 GAMMA = 0.6
+ PHI = 0.7 VTO = -0.9 DELTA = 0.1
+ UO = 250 ETA = 0 THETA = 0.1
+ KP = 40E-6 VMAX = 5E4 KAPPA = 1
+ RSH = 0 NFS = 1E12 TPG = -1
+ XJ = 500E-9 LD = 100E-9
+ CGDO = 200E-12 CGSO = 200E-12 CGBO = 1E-10
+ CJ = 400E-6 PB = 1 MJ = 0.5
+ CJSW = 300E-12 MJSW = 0.5
+ )
```