Please read carefully before starting:

- Simulation tool to be used is National Instruments (NI) Multisim.
- The setup of the NMOS and PMOS transistors and their models are given at the end of the document.
- You should be divided into groups of three students.
- Each group should be ready for a discussion in the project (schematics and simulations results on Multisim are needed).
- You are required to deliver a hard copy report that contains:
    1. Schematic diagrams (snapshots from Multisim showing dimensions and values)
    2. Design procedure (hand calculations)
    3. Simulation results (snapshots from Multisim)
    4. Discussion of your results and conclusions

Any missing item from the 4 items above will be penalized in the report grading.

- The total grade of the project is 15 points.
- The deadline to submit the project report (delivered to the classroom) April 24th, 2020.
- Any copied will be given zero.

1. Transistor Characterization:

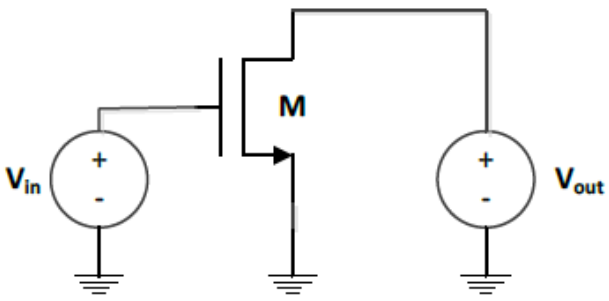


Fig. 1 Transistor Characterization

(a) For the schematic shown in Fig. 1 with W=10µm, L=1µm:

- Perform DC sweep for Vout (from 0 to 3V) while Vin=2V and plot ID vs. Vout.
- Perform DC sweep for Vin (from 0 to 3V) while Vout=2V and plot ID vs. Vin.
- From the above curves determine the value of VTH, µnCOX, and λ.
- Repeat the above for W=20µm, L=2µm.
- Discuss your results

(b) Repeat (a) for a PMOS device with the same dimensions.

(c) Compare between NMOS and PMOS devices.

(d) Discuss your results

2. Current mirrors:

Compliance voltage is the minimum voltage V_{out} for the circuit to operate as a current mirror.

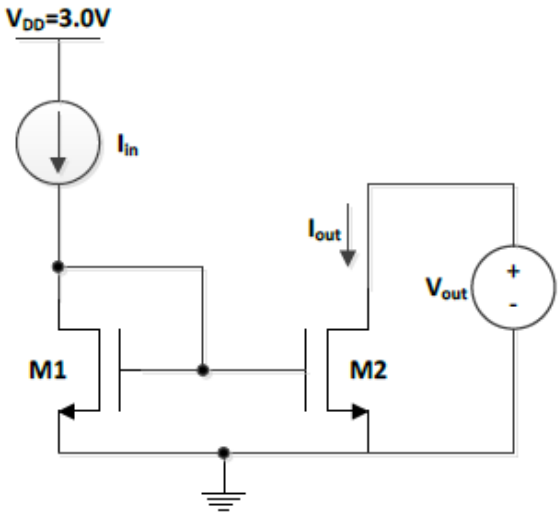


Fig 2(a) Simple Current Mirror

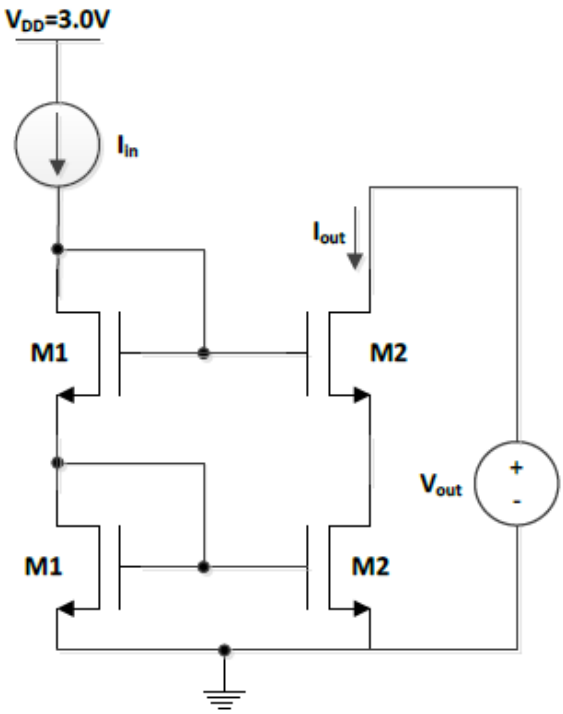


Fig 2(b) Cascode Current Mirror

(a) Design the simple current mirror in Fig. 2(a) such that Iin=100µA, Iout=200µA, and Veff is 0.25V for all transistors. L=1µm.

- Calculate the compliance voltage.
- Perform a DC sweep for Vout (from 0 to 3V) and plot Iout vs. Vout. Plot the percentage error in the output current (relative to the ideal value). Report the compliance voltage from those simulations and compare with calculations.
- Choose a proper DC value of Vout (more than the compliance voltage), run AC analysis to plot Rout vs frequency (up to 10GHz).

Repeat (a) for Iin=200µA and Iout=400µA. Veff should be kept at 0.25V.

(b) Use the same design from Fig. 2(a) to construct the cascode current mirror in Fig. 2(b). Repeat the same simulations.

3. Differential Pairs:

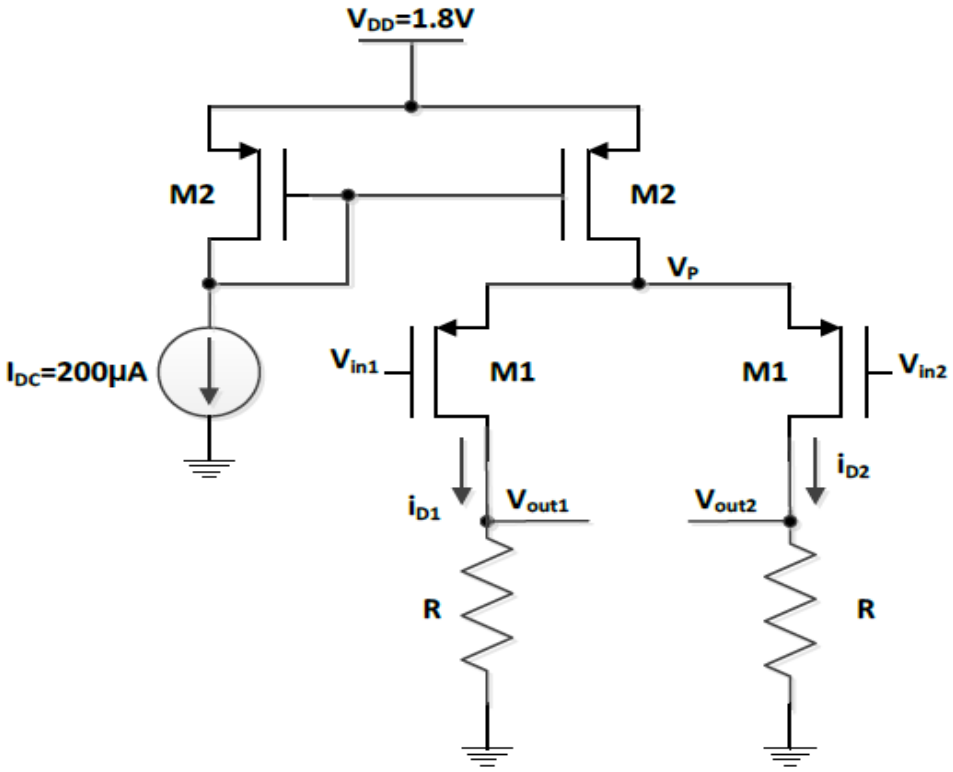


Fig. 4 Differential Amplifier

(a) Design the differential buffer shown in Fig. 4 with the following specifications:

- ADM ≥ 5
- Input linear range ≥ 0.2V
- Differential output voltage swing ≥ 1.0Vpp (peak to peak)

(b) Calculate the common-mode input range for your design.

(c) Document the design procedure and the results of the following simulations:

- DC analysis and show the Q-point (ID, VDS, Veff) of all transistors.
- DC sweep for Vid from -1.8V to 1.8V and plot iD1, iD2, and iOD.
- AC analysis and show the small-signal differential gain ADM, conversion gain ACM-DM (due to for 5% mismatch in the two resistors R), and CMRR vs. frequency.
- Transient analysis with

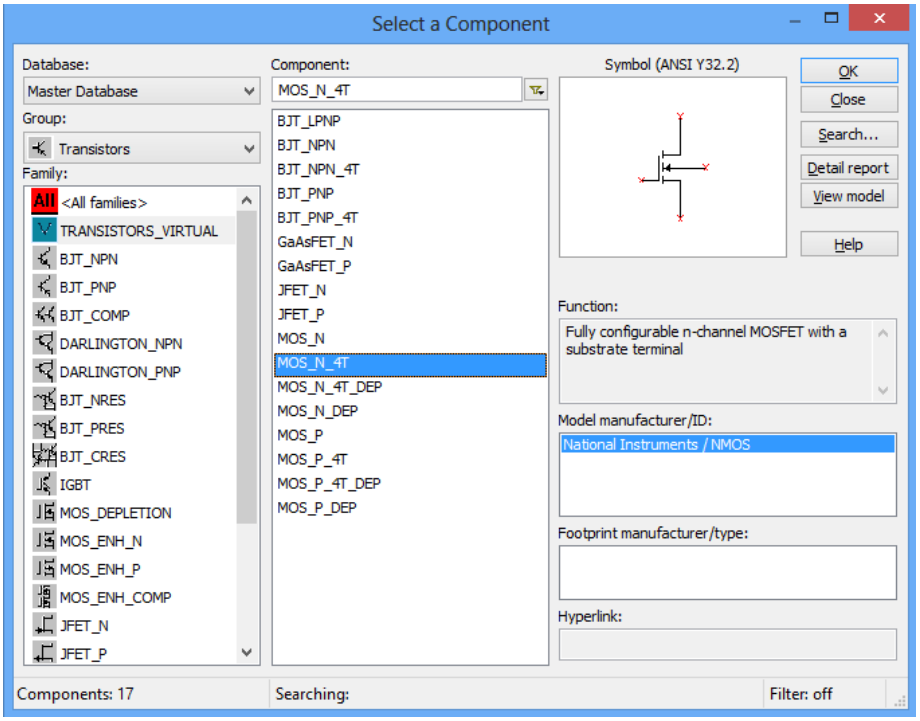
Vin1=DC+A.sin(2πft)+B.sin(4πft), Vin2=DC-A.sin(2πft)+B.sin(4πft).
Plot Vin1, Vin2, VP, Vout1, Vout2, Voutd. Where A=10mV, B=10mV, f=1MHz, DC is a proper DC value of your choice.

(d) **Discuss your results**.

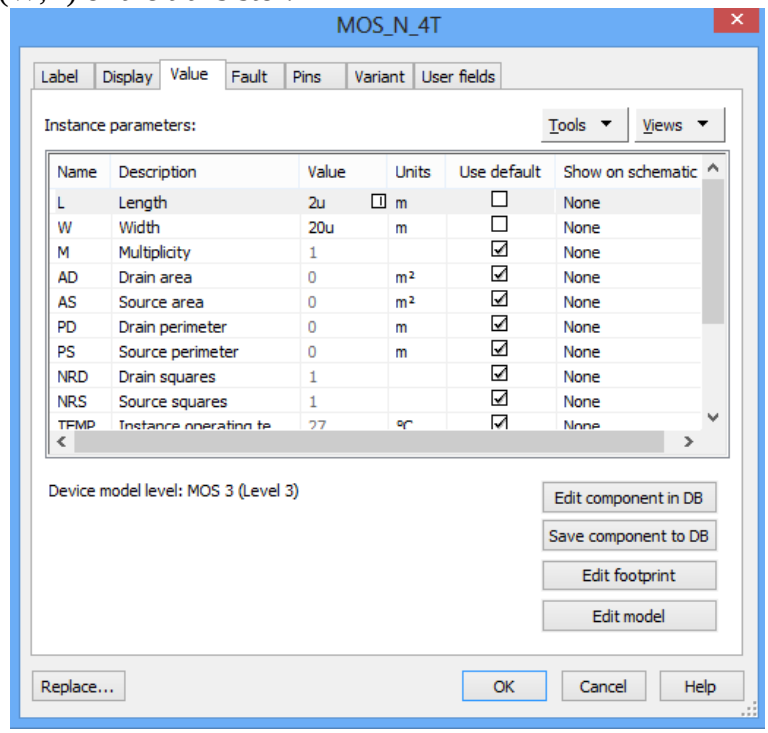
Note: The differential inputs Vin1 and Vin2 can be generated using an ideal transformer or ideal voltage controlled voltage source (VCVS).

Setup of the NMOS and PMOS transistors:

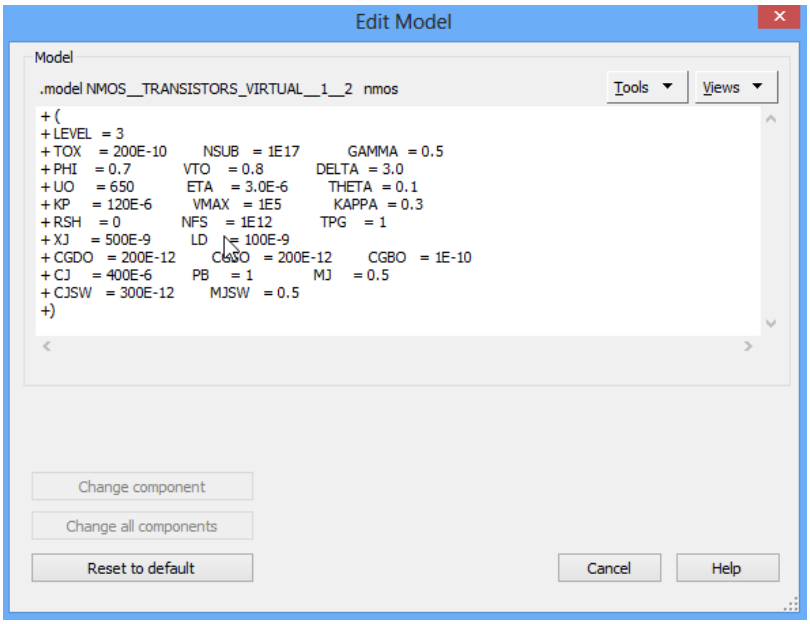
Choose an NMOS_4T from the menu of Place → Component (as shown below) and place it in your schematic.



Double click on the transistor and chosse the tab of "Value". This is where you can change the dimensions (W,L) of the transistor.



Click on the "Edit model" button.
Copy and paste the model of the NMOS (as shown) in the "SPICE view"
Make sure to click on the "Change componnet" button to save changes.



If you need to place another transistor in a schematic, copy the transistor that you have just created to get the correct model and you can then change the dimensions.
Repeat the same for the PMOS transistor (MOS_P_4T).
Minimum length of any transistor is 1µm. The bulk of an NMOS device should be connected to lowest voltage (ground) and that of a PMOS device should be connected to the highest voltage (V_{DD}).

NMOS:

```
+ (
+ LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17         GAMMA  = 0.5
+ PHI    = 0.7           VTO    = 0.8          DELTA  = 3.0
+ UO     = 650           ETA    = 3.0E-6       THETA  = 0.1
+ KP     = 120E-6        VMAX   = 1E5          KAPPA  = 0.3
+ RSH    = 0             NFS    = 1E12         TPG    = 1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12      CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1            MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5
+)
```

PMOS:

```
+ (
+  LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17         GAMMA  = 0.6
+ PHI    = 0.7           VTO    = -0.9         DELTA  = 0.1
+ UO     = 250           ETA    = 0            THETA  = 0.1
+ KP     = 40E-6         VMAX   = 5E4          KAPPA  = 1
+ RSH    = 0             NFS    = 1E12         TPG    = -1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12      CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1            MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5
+ )
```