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2-Stage Op-amp Design

Using Multisim

Submitted to:

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Hand Analysis:

- **Device Sizes (M1-M8), bias point, gm, ro , the Gain Analysis**

We are given that : VDD=3.3 V & I bias=100 uA then I_8=100uA

1. P(consumption)=1mW

And the power is equally distributed between stage "1" and stage" 2" and with Neglect the power consumption due to (I bias).

Then for stage "1": P1=0.5 mW

P1= $(I_3 + I_4)*VDD$

And we know that $I_1 = I_2 = I_3 = I_4 = I_5/2$

P1= $((I_5/2) + (I_5/2))$ *VDD then we get **I_5 =151.52 uA**

I_1=I_2=I_3= I_4 =75.76 uA

For stage "2" : P2=0.5 mW

P2= I_7 *VDD then we get **I_7 = 151.52 uA**

And we know that I_6=I_7

I_6= 151.52 uA

By using this equation (1/(λ*I) we can determine ro for transistors:

$ro_{1,2}$=330 KΩ, $ro_{3,4}$=203 KΩ , $ro_{5,6}$=165 KΩ, ro_7= 101.5 KΩ, ro_8= 250 KΩ

2. Maximum Input Common Mode Voltage = 3V

This value for M1 to be in SAT VD>VG-VTHn

VG=VinCM

Then VG < VD+VTHn then

VinCM)max= VD+VTHn VD=VDD-VSG3 && VTHn=0.8 V

Then we can get VSG3=1.1 V and |VTHp|=0.9 then **Veff3=0.2 V**

We know that VSG3=VSG4 then **Veff4=0.2 V**

3 .Zero Systematic Offset:

To achieve that we need to made Prefect Mirroring between M3&M4 then We need VSD3=VSD4 and as VS3=VS4 so we need VD3=VD4

VD3=VDD-VSG3 & VD4=VDD-VSG7 then we need to achieve that condition

VSG3=VSG7 so we can say that **Veff7=0.2V**

4. Differential mode gain=80dB

Then the gain =10^4 we can get the gain by get the gain of each stage

For Stage "1":

$Av1=-gm_{1,2}*(ro_{1,2}//ro_{3,4})$

For Stage "2":

$Av2=-gm_7*(ro7//ro6)$

Total Gain=Av1*Av2 then **Total Gain=Av1*Av2**

$gm_7=(2*I_7)/Veff7$ then **gm7=1.52*10^-3 A/V**

$10^4= gm_{1,2} *(ro2//ro4)* gm_7*(ro7//ro6)$ then **$gm_{1,2}$ = 8.33*10^-4**

$gm_{1,2} =(2* I_{1,2})/Veff_{1,2}$ **Veff1=Veff2=0.2 V**

5.Min output voltage=0.2

Veff5=Veff6=Veff8= Min output voltage

Then **Veff5=Veff6=Veff8=0.2 V**

By using the equation of current of transistor in SAT region &assume L=1um

We can get the Width for transistors:

IDS= 0.5 µnCox (W/L) $((VGS-VTH)^2$

W1=W2=32 um, W3=w4=95 um, W5=W6=63 um, W7= 189 um, W8= 42 um

gm for the rest of transistors: using gm=(2*I) /Veff

gm1=gm2= 8.33*10^-4 A/V (from equation of gain)

gm3=gm4=7.6*10^-4 A/V

gm5 = gm6 = gm7 = 1.52*10^-3 A/V

gm8= 10^-3 A/V

➢ Op-amp Noise Analysis:

* OP-amP Noise analysis:

We will take in Consideration Thermal noise only.

We know That: The Source of The Thermal noise from drain to Source and These are The formulas To determine it:

$$i_n^2 = 4KT\gamma g_m, \quad v_n^2 = \frac{4KT\gamma}{g_m}$$

we are given That: $K = 1.38 * 10^{-23}$ J/K
$T = 300°K$, $\gamma = 1$

we will divide also The analysis for The two stages:

→ For stage "1": we have M_1 & M_2 & M_3 & M_4

$$v_{n_1}^2 = v_{n_2}^2 = \frac{4KT\gamma}{g_{m_{1,2}}} \quad //$$

$$v_{n_3}^2 = v_{n_4}^2 = \frac{4KT\gamma}{g_{m_{3,4}}}$$

Due to $M_{1,2}$: $v_{o_{n_{1,2}}}^2 = 2v_{n_{1,2}}^2 * \left[g_{m_{1,2}}(r_{o_{1,2}} \| r_{o_{3,4}}) * g_{m_7}(r_{o_7} \| r_{o_6})\right]^2$

Due To $M_{3,4}$: $\overline{v_{on}^2}_{3,4} = 2\overline{v_n^2}_{3,4} * \left[g_{m_{3,4}} (r_{o_{1,2}} \| r_{o_{3,4}}) * g_{m_7} (r_{o_7} \| r_{o_6}) \right]^2$

→ For stage "2": we have M_6 & M_7

$$\overline{i_n^2}_7 = \overline{i_n^2}_6 = 4KT\gamma\, g_{m_{6,7}}$$

Due To M_6 & M_7 : $\overline{v_{on}^2}_{7,6} = 2\,\overline{i_n^2}_{6,7} * (r_{o_7} \| r_{o_6})^2$

→ For OP amP:

$$\overline{v_{on}^2}_{\text{"Total"}} = \overline{v_{on}^2}_{1,2} + \overline{v_{on}^2}_{3,4} + \overline{v_{on}^2}_{6,7}$$

$$\overline{v_{in}^2}_{\text{refered}} = \frac{\overline{v_{on}^2}_{\text{Total}}}{A_{dm}^2}, \quad A_{dm} = g_{m_{1,2}} (r_{o_{1,2}} \| r_{o_{3,4}})\, g_{m_7} (r_{o_6} \| r_{o_7})$$

$$\overline{v_{in}^2}_n = 2\overline{v_n^2}_{1,2} + 2\overline{v_n^2}_{3,4} * \frac{g_{m_{3,4}}^2}{g_{m_{1,2}}^2} + 2\,\overline{i_n^2}_{6,7} * \frac{1}{g_{m_7}^2 g_{m_{1,2}}^2 (r_{o_2} \| r_{o_4})^2}$$

$$\overline{v_{in}^2}_n = 2\left(\frac{4KT\gamma}{g_{m_{1,2}}}\right) + 2\left(\frac{4KT\gamma}{g_{m_{3,4}}}\right)\left(\frac{g_{m_{3,4}}^2}{g_{m_{1,2}}^2}\right) + 2\left(\frac{4KT\gamma}{g_{m_7} * g_{m_{1,2}}^2 (r_{o_2} \| r_{o_4})^2}\right)$$

$$\overline{v_{in}^2}_{\text{refered}} = 8KT\gamma \left[\frac{1}{g_{m_{1,2}}} + \frac{g_{m_{3,4}}}{g_{m_{1,2}}^2} + \frac{1}{g_{m_7} (g_{m_{1,2}})^2 (r_{o_6} \| r_{o_7})^2} \right]$$

⇓

Input refered noise = 8.7 nV/√Hz

➢ OP-amp CMRR Analysis:

* Hand analysis for CMRR:

→ for Diff. Mode analysis:

We get that : $\boxed{A_{dm} = g_{m_{1,2}} (r_{o_2} \parallel r_{o_4}) * g_{m_7} (r_{o_7} \parallel r_{o_6})}$

→ for CM. Mode analysis:

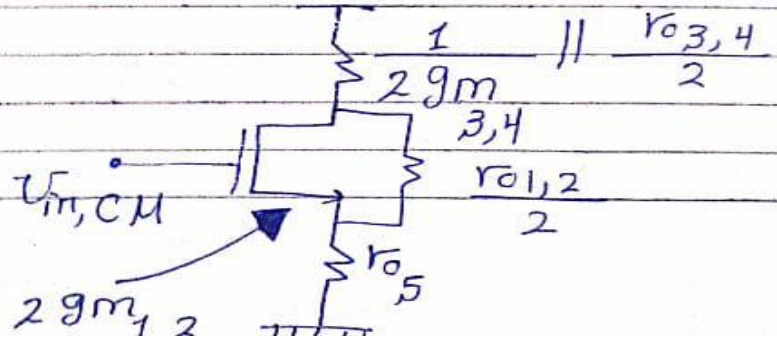
We will get also the gain from each stage

→ for Stage "1":

we will add M_1 and M_2 in Parallel. and M_3 and M_4 in Parallel

and the output R for $M_5 = r_{o_5}$

Then we will get this:



Neglecting $r_{o_{1,2}}$ and assuming

$$\frac{1}{g_{m_{3,4}}} \ll r_{o_{3,4}}$$

Then: $$\frac{A}{1} \simeq \frac{-2g_{m_{1,2}} * \left[\frac{1}{2g_{m_{3,4}}} \,||\, \frac{r_{o_{3,4}}}{2}\right]}{1 + 2g_{m_{1,2}} * r_{o_5}}$$

$$\frac{A}{1} \simeq \frac{-g_{m_{1,2}}}{g_{m_{3,4}}} * \frac{1}{1 + 2g_{m_{1,2}} * r_{o_5}}$$

→ for stage "2":

$$\frac{A}{2} = -g_{m_7} * (r_{o_6} \,||\, r_{o_7})$$

Then:

$$\frac{A}{CM} = \frac{A}{1} * \frac{A}{2} = \frac{g_{m_{1,2}}}{g_{m_{3,4}}} * g_{m_7} (r_{o_6} \,||\, r_{o_7}) * \frac{1}{1 + 2g_{m_{1,2}} * r_{o_5}}$$

$$CMRR\Big|_{dB} = 20 \log \left| \frac{A_{dm}}{A_{CM}} \right|$$

$$\Downarrow$$

$$* \boxed{CMRR\Big|_{dB} = 84.23 \text{ dB}} * > 60 \text{ dB}$$

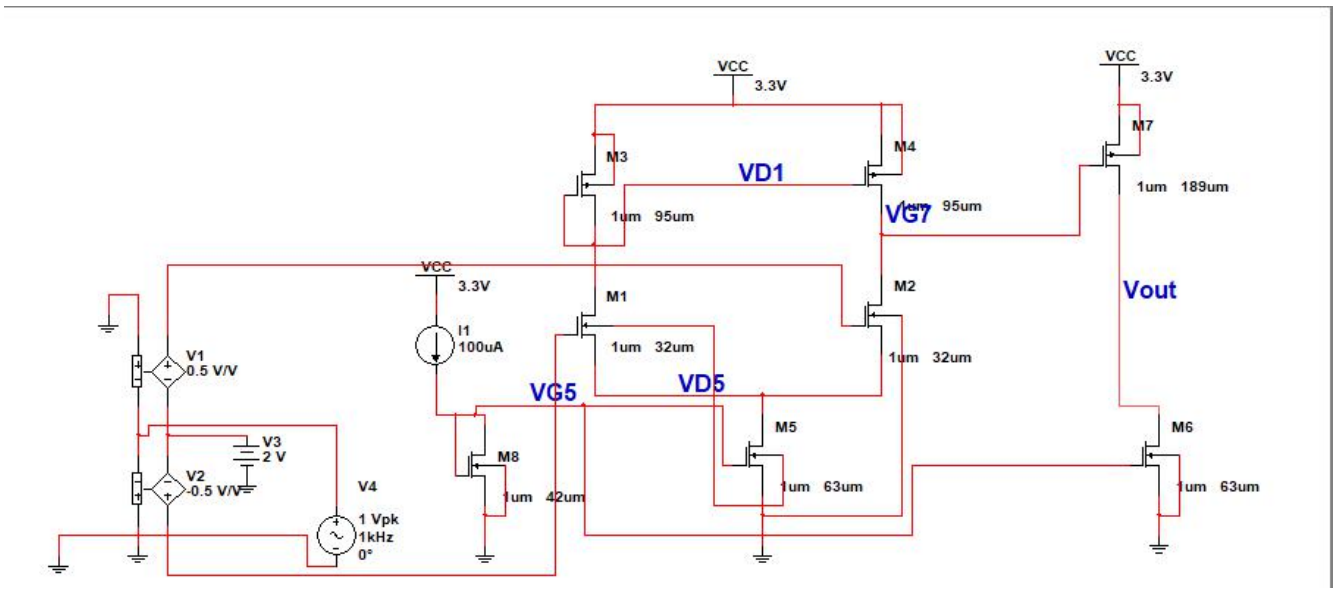
➢ Summary for “Hand Analysis”

We can summarize “Hand Calculations” by this Table:

“Hand Analysis “	L	W	I	ro	gm(A/V)	Veff
M1	1um	32um	75.76 uA	330KΩ	8.33*10^-4	0.2 V
M2	1um	32um	75.76 uA	330KΩ	8.33*10^-4	0.2 V
M3	1um	95um	75.76 uA	203KΩ	7.6*10^-4	0.2 V
M4	1um	95um	75.76 uA	203KΩ	7.6*10^-4	0.2 V
M5	1um	63um	75.76 uA	165KΩ	1.52*10^-3	0.2 V
M6	1um	63um	151.52 uA	165KΩ	1.52*10^-3	0.2 V
M7	1um	189um	151.52 uA	101.5KΩ	1.52*10^-3	0.2 V
M8	1um	42um	100 uA	250KΩ	10^-3	0.2 V

“Hand Analysis”	Input Refereed Noise	CMRR
	8.7 nV /(HZ)^{½}	84 dB

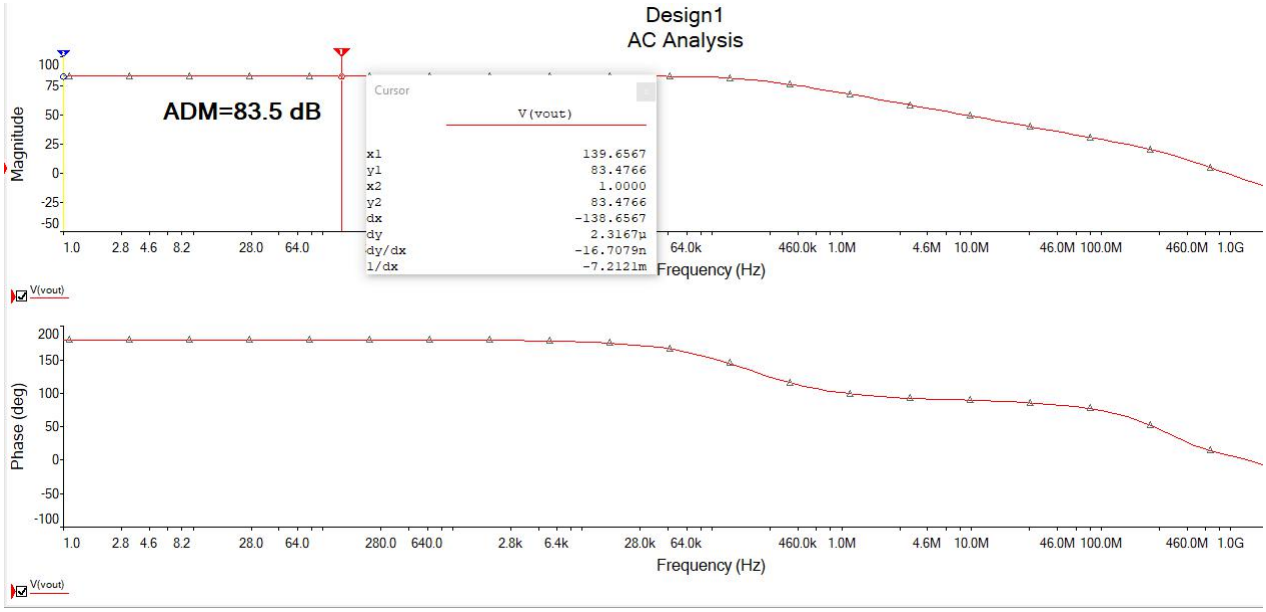
Design& Simulation results:



➢ Gain & Bandwidth & CMRR

1.Differential Mode Gain:

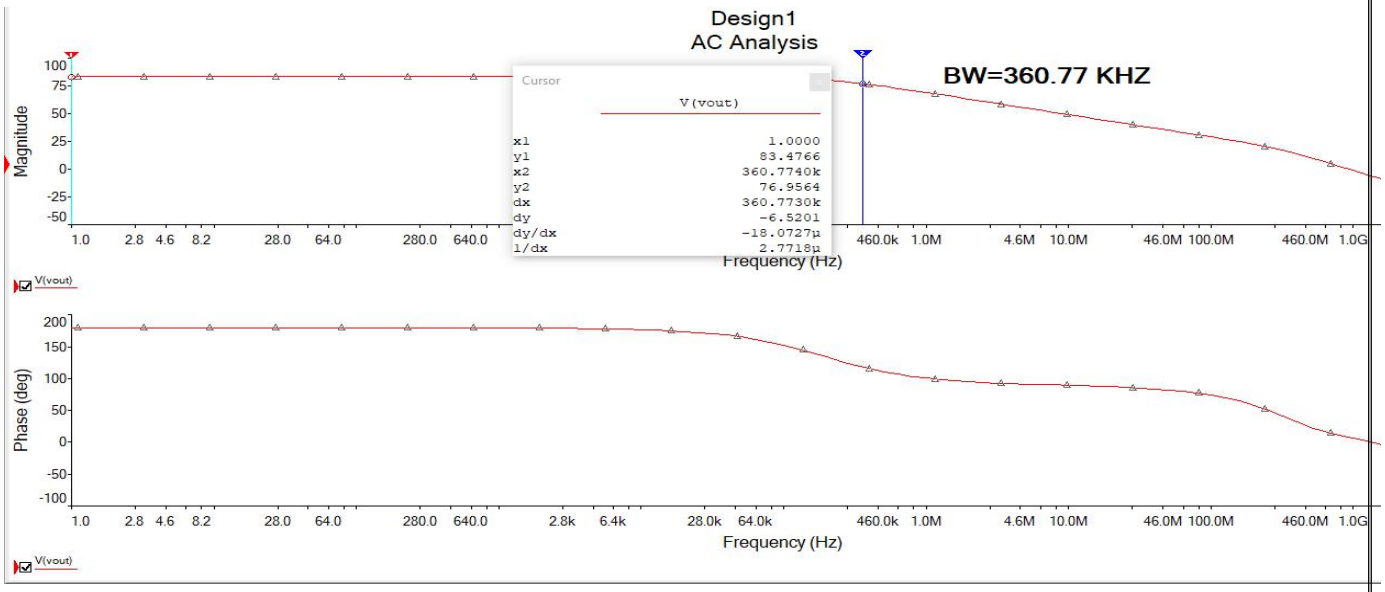
We make AC analysis and this is the simulation result:



As we see that we achieved the target of diff mode gain : **Adm=83.5 dB**

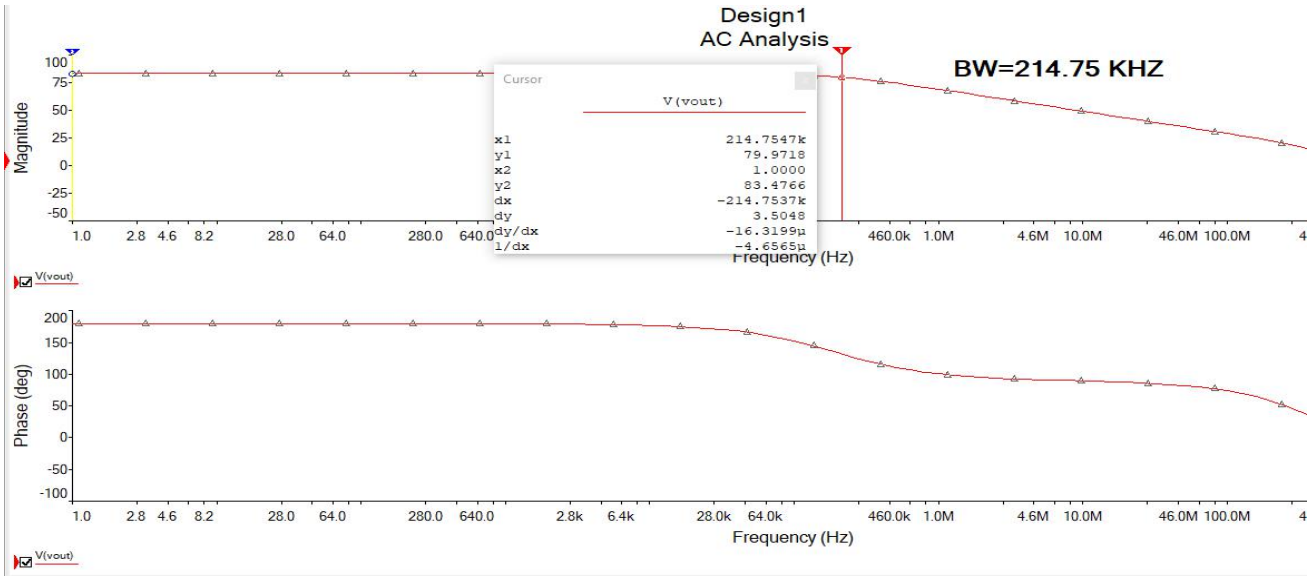
2.Open Loop 3dB Bandwidth:

Bandwidth=fc where fc(cut off frequency) at which the gain will be Adm= 77dB From Simulation Results:



As we see that we achieved the target of Bandwidth: **BW=360.77 KHZ**

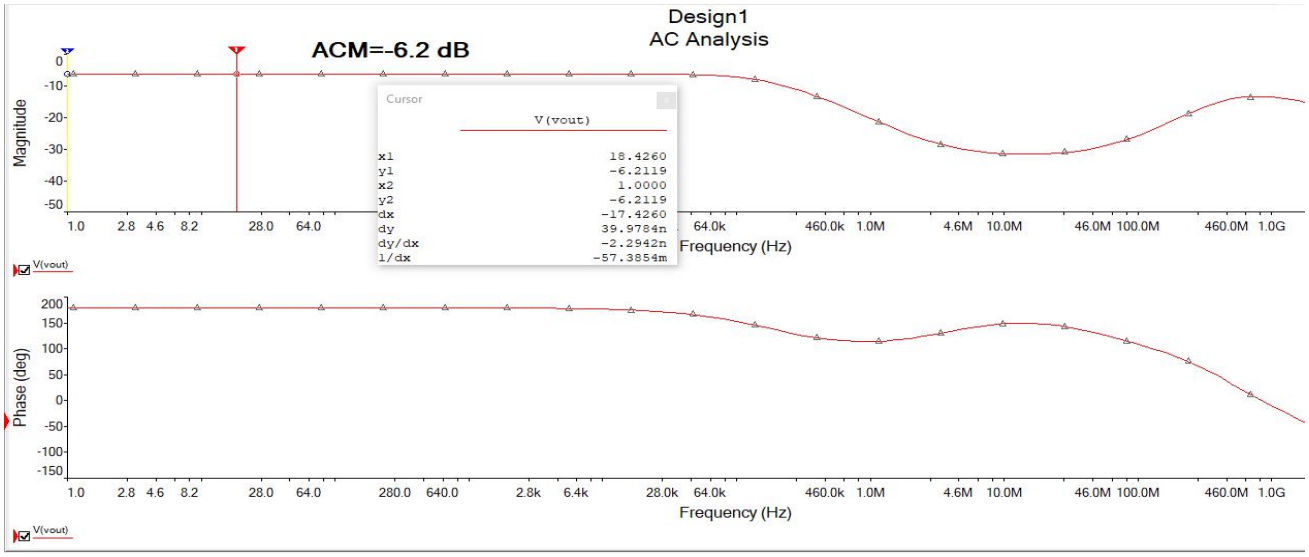
Or if we need to get at which the gain that we get from simulation decrease by a 3dB So we can get the bandwidth at Adm=80 dB and this simulation result:



As we see that we also achieved the target of Bandwidth**:**

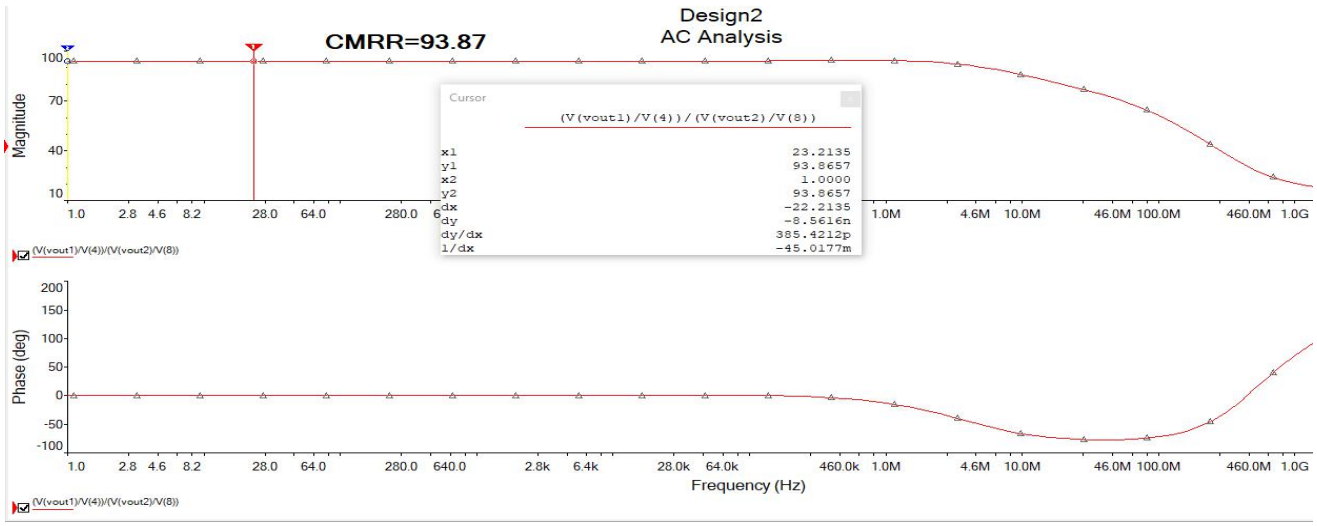
BW=214.75 KHZ

3.Common Mode Gain



We have achieved that we want ACM very small as: **ACM=-6.3 dB**

4.CMRR:

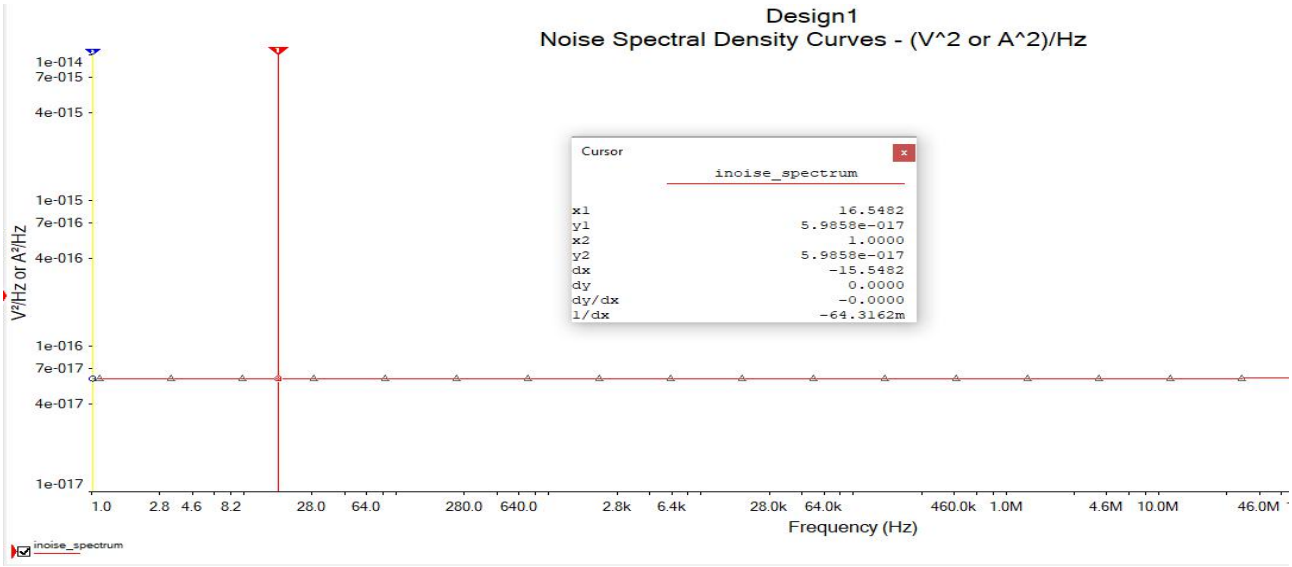


We have achieved the target by: **CMRR=93.87dB**

It differs slightly from that we got from hand calculation as we made many approximations and neglections.

➢ Input Referred Noise

We made Noise analysis and this is the simulation result:



V^2in(noise referred)=6*10^-17 nV^2/HZ then

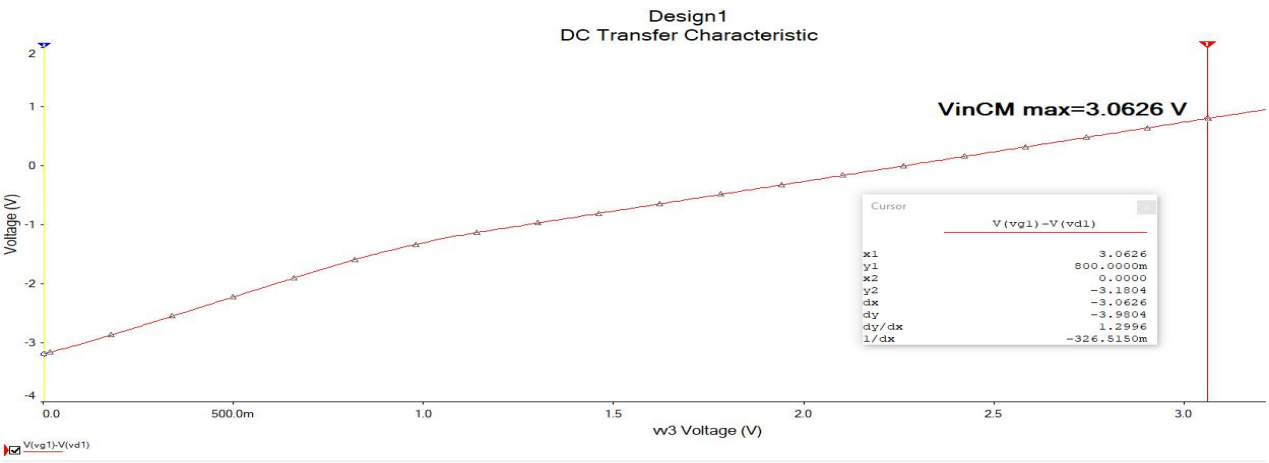
Input Referred Noise= 7.75 nV/(HZ)^{½}

➢ Input Common Mode Range:

1.Max Input Common Mode

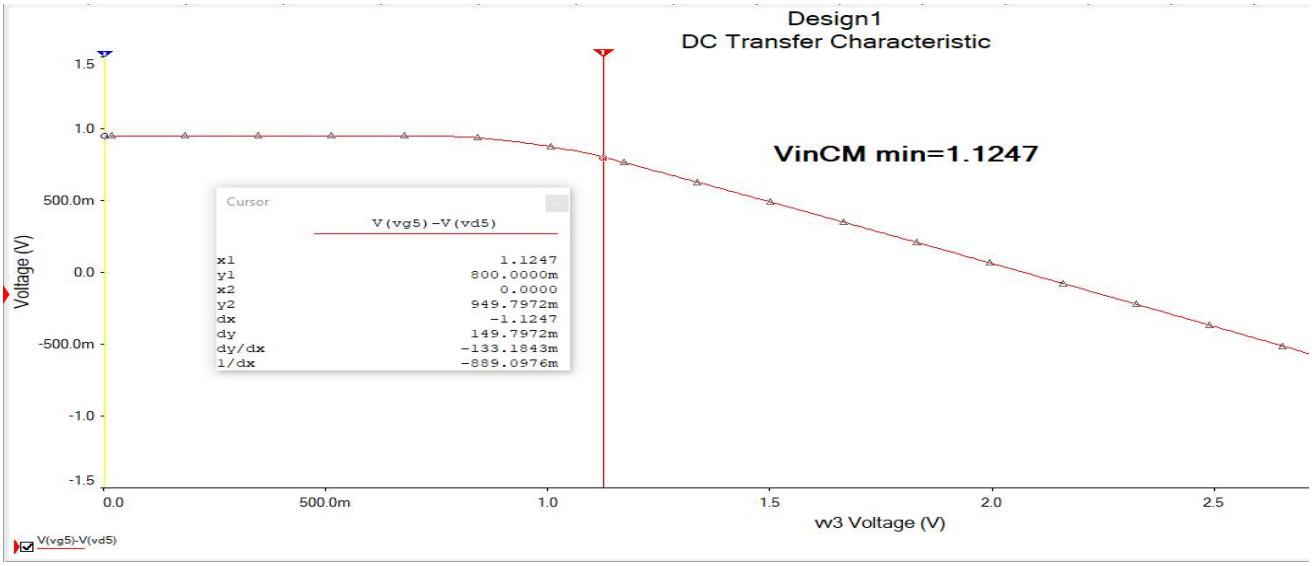
As we said previously that this value that make M1 to be in sat

Then simply we can check this value by simulation through DC sweep for VinCM that is in our design V3 with (VG1-VD1) and see which value for V3 that VG1-VD1=VTHn=0.8 V , this will be max input common mode and this is the simulation result:



2.Min Input Common Mode

In this case this value that make M5 to be in sat and to check this value we will do as we did with Max and this is the simulation result:



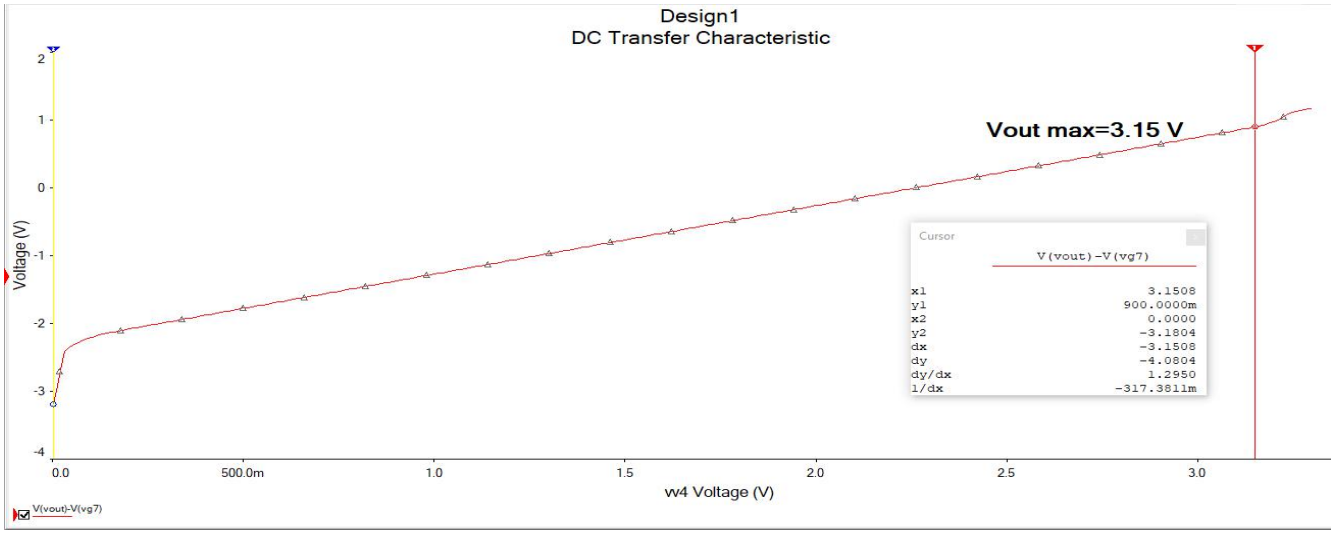
➢ Output Voltage Range:

We need to sweep the output voltage so we will connect output node with source but in the same time we need to enter the input so we made a negative feedback by connect output node with Vin^+ then we benefit from the properties of op-amp that higher gain (approximately infinite)&negative feedback then $Vin^+=Vin^-$ so we connect the source with Vin+ and with negative feedback then $Vin^+=Vin^-=Vout$ so we can sweep on the output voltage.

1.Max Output Voltage

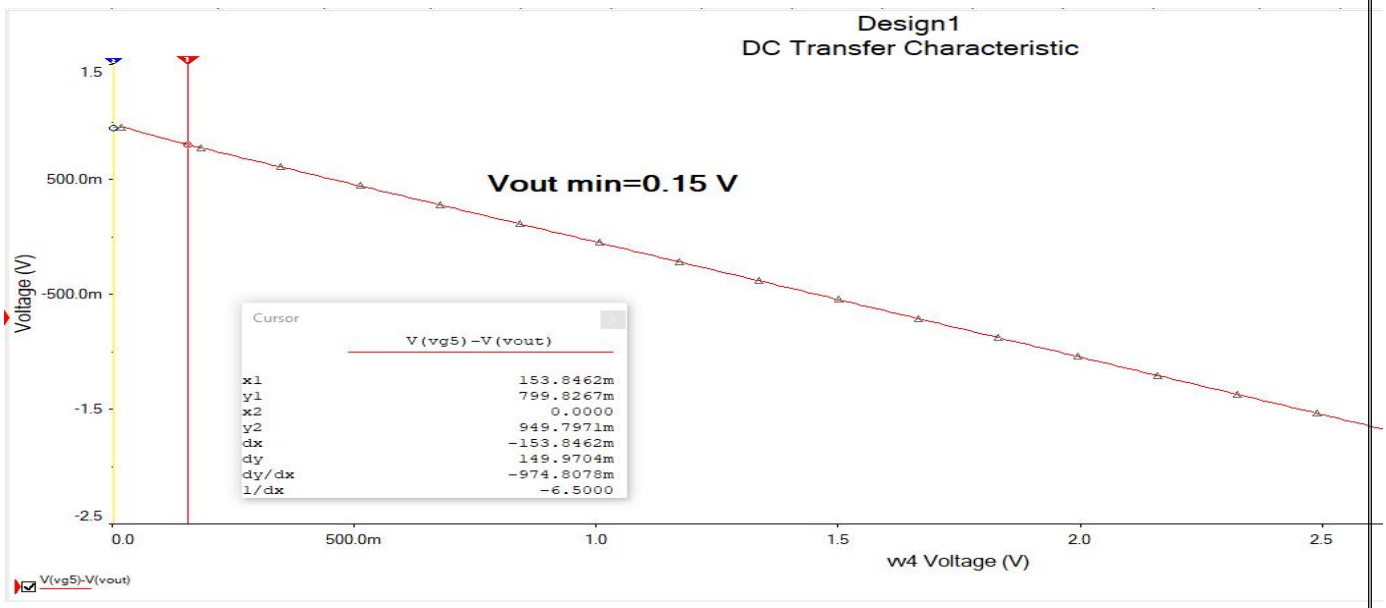
This is the value that make M7 in sat then to check this value we will use the same method that we used it in the input common mode range but in this case M7 is PMOS so we will see at which value of VOUT that

VD7-VG7=0.9 V and this is the simulation result:



2.Min Output Voltage

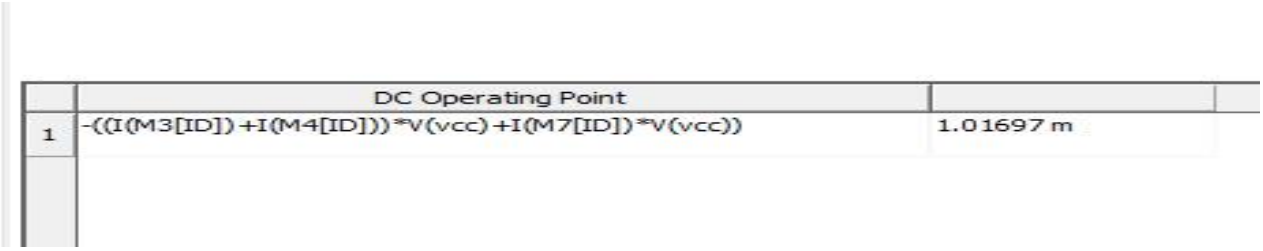
This is the value that make M6 in sat then to check this value we will use the same method that we used it in the input common mode range and this is the simulation result:



➢ Power Consumption:

We can check this value by making DC analysis and get the P through:

$P=(I_3+I_4)*VCC+(I_7)*VCC$ and this is the result of simulation:



	DC Operating Point	
1	-((I(M3[ID])+I(M4[ID]))*V(vcc)+I(M7[ID])*V(vcc))	1.01697 m

➢ Summary for Simulation Results:

Spec.	Target	Sim.results	Units	Comment
Differential Mode Gain	80 dB	83.5	dB	We get an extra gain than the achieved but in op_amp we need higher gain.so it's accepted
Common Mode Gain	….	-6.3	dB	We need a low "Acm" and that we have achieved here.
CMRR	>60	93.87	dB	We need to get a higher ratio and that we have achieved here.
Open Loop 3dB Bandwidth	Min 180-280	360.77 or 214.75	KHZ	First value if we consider at A=77 dB and the second at A=80.
Input Refereed Noise	7-8	7.75	$7nV/(HZ)^{½}$	It differs from hand analysis due that gm in the simulation be higher.
Max Input Common Mode	3 V	3.0626	V	
Min Input Common Mode	….	1.1247	V	
Max Output Voltage	….	3.15	V	It's very close to its value from hand analysis (Vout=VDD-veff) Vout=3.1V
Min Output Voltage	0.2 V	0.15	V	Which is approximately equals 0.2 as the target
Power Consumption	1	1.017	mW	Neglecting I bias we achieved the target

General comment: we have achieved the targets for design op_amp the higher gain by two stages and extra thing the higher bandwidth and the high input impedance by mos. diff.pair ,we can add to this design a third stage like source follower to get the low output impedance for op_amp to repair this op_amp to use it in many applications .