ECSE 323 – Digital System Design
Card Dealer Circuit
g39_dealerFSM
g39_dealerTestBed

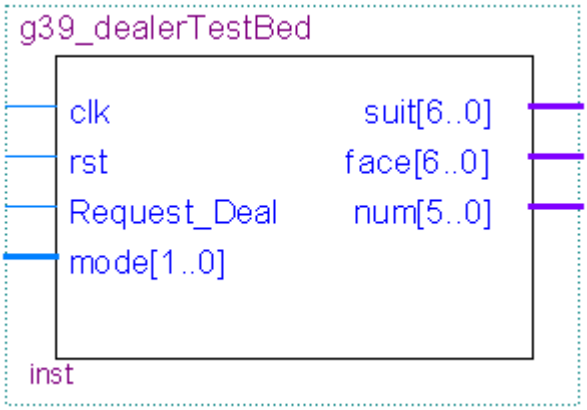
Description:

The g39_dealerTestBed circuit puts together g39_dealerFSM, g39_lab3 (stack52), g39_7_segment_decoder, g39_RANDU, g39_Modulo_13 along with other library components to represent a dealer deck. The objective here is to pop - at random - a card from the dealer deck and push in onto a player's deck.

The circuit has the following inputs/outputs:

Request_Deal: 1-bit input to request a deal
mode: 2-bit input representing the operation desired
rst: 1-bit input
clk: 1-bit input

suit: 7-bit output representing the suit
face: 7-bit output representing the face value
num: 6-bit output representing the number of cards in the dealer deck



Implementation Details:

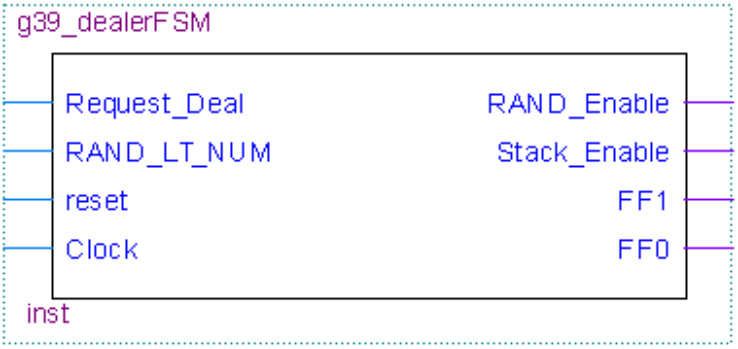
Sub-circuits:
(Modulo_13, 7_segment_decoder, stack52 and RANDU were explained in previous reports)
(library components used: lpm_compare, lpm_DFF, lpm_decode)

g39_dealerFSM:

Description:
The circuit is a finite state machine taking care of the different states the dealer circuit has. The FSM is a Moore machine implementing the sequence described in lab 4.

The circuit has the following inputs/outputs:
Request_Deal: 1-bit input to request a deal (starts process)
RAND_LT_NUM: 1-bit input representing whether the random address < number of cards
reset: 1-bit input
clock: 1-bit input

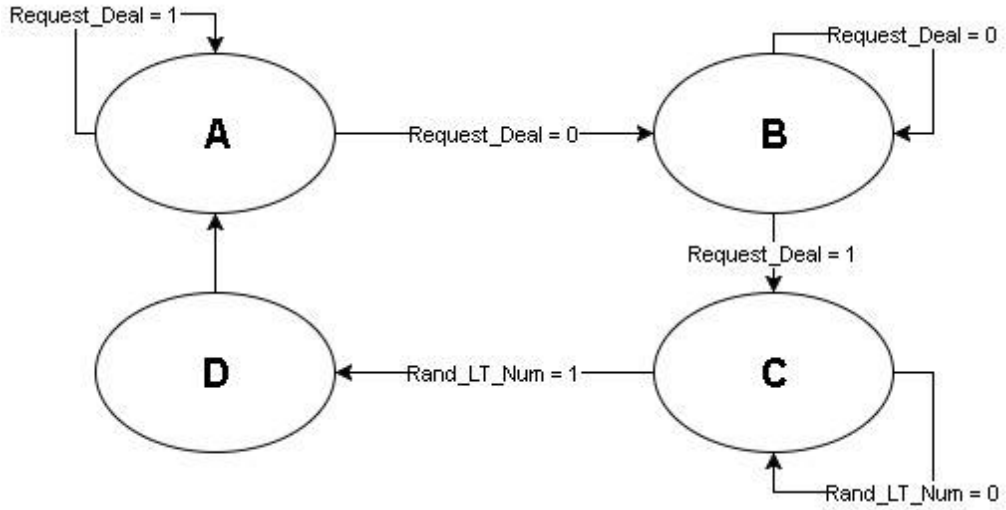
RAND_Enable: 1-bit output that enables a new random number to be generated
Stack_Enable: 1-bit output that enables the pop operation
FF1: 1-bit output representing $Q1^+$
FF0: 1-bit output representing $Q0^+$



Implementation Details:

****:** The FSM was implemented in VHDL using D flip flops

State diagram



Present State			Next State $Q_1^+Q_0^+$				Output	
state	Q_1	Q_0	Request_Deal 0	Request_Deal 1	Rand_LT_Num 0	Rand_LT_Num 1	Stack_Enable	Rand_Enable
A	0	0	01	00	XX	XX	0	0
B	0	1	01	11	XX	XX	0	0
C	1	1	XX	XX	11	10	0	1
D	1	0	00	00	00	00	1	0

Q_1^+	Request_DealRand_LT_Num			
Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	1	1	1	1
10	0	0	0	0

$$\mathbf{Q_1^+} = Q_1Q_0 + Q_0.\text{Request\_Deal}$$

Q_0^+	Request_DealRand_LT_Num			
Q_1Q_0	00	01	11	10
00	1	1	0	0
01	1	1	1	1
11	1	0	0	1
10	0	0	0	0

$$\mathbf{Q_0^+} = Q_1'Q_0 + Q_1'.\text{Request\_Deal}' + Q_0.\text{Rand\_LT\_Num}'$$

Rand_Enable = Q_1Q_0 (state C)

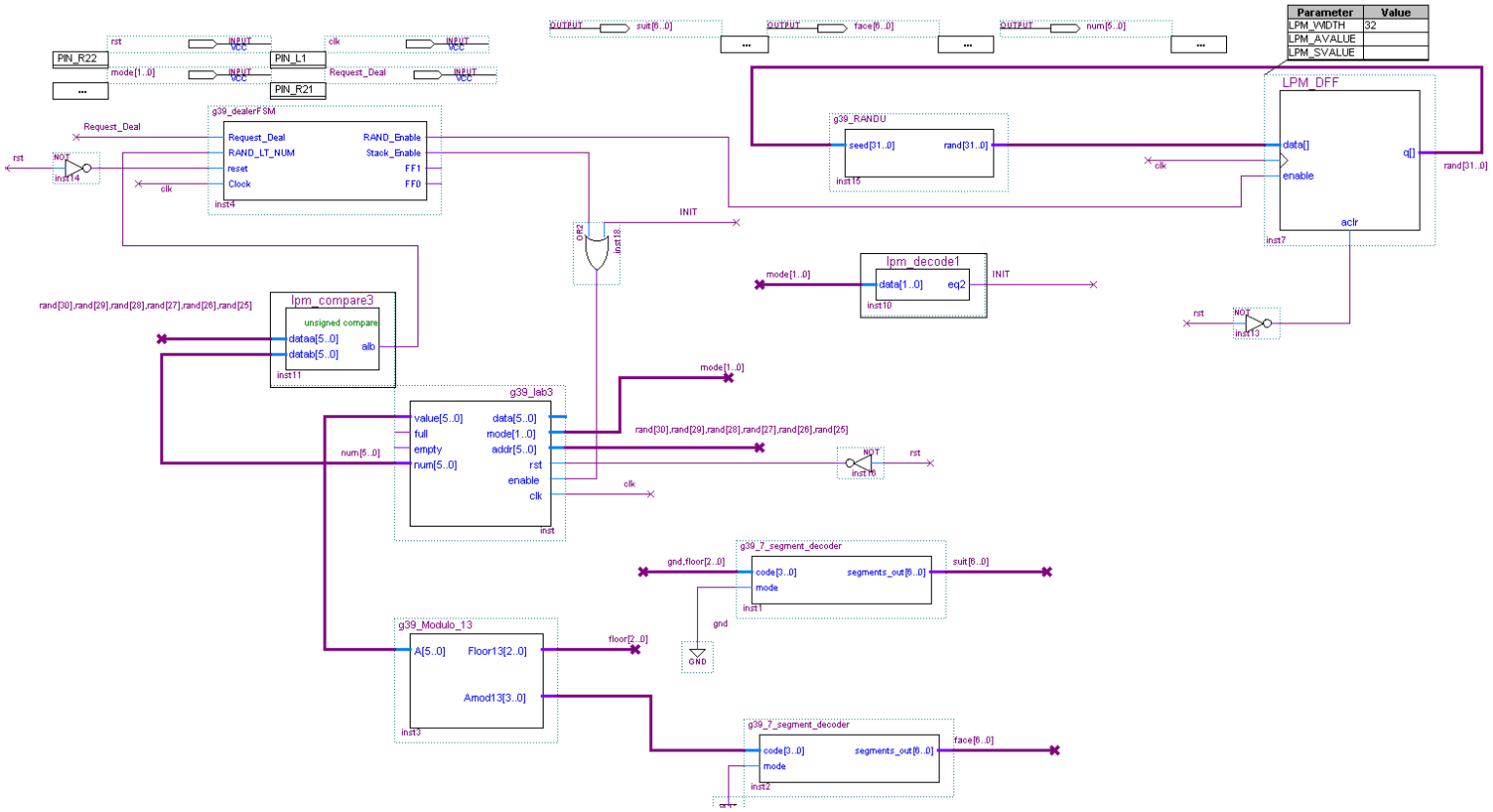
Stack_Enable = Q_1Q_0' (state D)

g39_RANDU:

The circuit works as described in lab 2 with a small change.

When implementing the testbed, a problem occurs if SEED is initialized to 0 since b = 0 (as instructed in lab 2). The RANDU circuit will generate all 0s. To solve this, we set b to 1 so that SEED is initialized to 1.

Test_bed Logic:



- Initially Request_Deal is high, since the pushbutton is high when not pressed
- The deck is initiall initialized by setting the mode to “10”, then the mode is set to “11” to allow for popping
- Once a button is pressed by the user (Request_Deal is low) then we follow the following path for the states: 00 (A) → 01 (B) → 11 (C)
- Since we are at state 11, Rand Enable becomes ‘1’ or high, enabling the D-FF to take values from the g39_RANDU circuit, which generates random numbers.
- The random number (an address) is then compared with “num”, the number of cards in the deck resulting. One of two scenarios is then followed:
    1. If the random number is less than the number of cards in the deck, RAND_LT_NUM is set to ‘1’ or high. Meaning we are at state 11 (C), and RAND_LT_NUM is ‘1’, therefore Stack_Enable becomes ‘1’, and a card is popped
    2. If the random number is greater or equal to the number of cards in the deck, RAND_LT_NUM is set to ‘0’, meaning we stay at state 11 (C) allowing for another random number to be generated. This continues to happen until we satisfy the first scenario
- The g39_lab3 (stack52) circuit provides a “value” which is then passed to the g39_Modulo13 circuit which provides the floor (suit) and remainder (face value) to the 7 segment decoders. The 7 segment decoders show the card on the LED screens

Testing:

Pin assignments:

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Differential Pair
num[3]	Output	PIN_Y19	6	B6_N1	PIN_Y19	3.3-V LV...default)		24mA (default)	
num[5]	Output	PIN_V19	6	B6_N1	PIN_V19	3.3-V LV...default)		24mA (default)	
num[2]	Output	PIN_U19	6	B6_N1	PIN_U19	3.3-V LV...default)		24mA (default)	
num[4]	Output	PIN_T18	6	B6_N1	PIN_T18	3.3-V LV...default)		24mA (default)	
rst	Input	PIN_R22	6	B6_N0	PIN_R22	3.3-V LV...default)		24mA (default)	
Request_Deal	Input	PIN_R21	6	B6_N0	PIN_R21	3.3-V LV...default)		24mA (default)	
num[0]	Output	PIN_R20	6	B6_N0	PIN_R20	3.3-V LV...default)		24mA (default)	
num[1]	Output	PIN_R19	6	B6_N0	PIN_R19	3.3-V LV...default)		24mA (default)	
mode[0]	Input	PIN_M1	1	B1_N0	PIN_M1	3.3-V LV...default)		24mA (default)	
mode[1]	Input	PIN_L2	2	B2_N1	PIN_L2	3.3-V LV...default)		24mA (default)	
clk	Input	PIN_L1	2	B2_N1	PIN_L1	3.3-V LV...default)		24mA (default)	
suit[0]	Output	PIN_J2	2	B2_N1	PIN_J2	3.3-V LV...default)		24mA (default)	
suit[1]	Output	PIN_J1	2	B2_N1	PIN_J1	3.3-V LV...default)		24mA (default)	
face[1]	Output	PIN_H6	2	B2_N0	PIN_H6	3.3-V LV...default)		24mA (default)	
face[2]	Output	PIN_H5	2	B2_N0	PIN_H5	3.3-V LV...default)		24mA (default)	
face[3]	Output	PIN_H4	2	B2_N0	PIN_H4	3.3-V LV...default)		24mA (default)	
suit[2]	Output	PIN_H2	2	B2_N1	PIN_H2	3.3-V LV...default)		24mA (default)	
suit[3]	Output	PIN_H1	2	B2_N1	PIN_H1	3.3-V LV...default)		24mA (default)	
face[4]	Output	PIN_G3	2	B2_N0	PIN_G3	3.3-V LV...default)		24mA (default)	
suit[4]	Output	PIN_F2	2	B2_N1	PIN_F2	3.3-V LV...default)		24mA (default)	
suit[5]	Output	PIN_F1	2	B2_N1	PIN_F1	3.3-V LV...default)		24mA (default)	
suit[6]	Output	PIN_E2	2	B2_N1	PIN_E2	3.3-V LV...default)		24mA (default)	
face[0]	Output	PIN_E1	2	B2_N1	PIN_E1	3.3-V LV...default)		24mA (default)	
face[5]	Output	PIN_D2	2	B2_N0	PIN_D2	3.3-V LV...default)		24mA (default)	
face[6]	Output	PIN_D1	2	B2_N0	PIN_D1	3.3-V LV...default)		24mA (default)	

Flow summary:

Flow Summary

Flow Status	Successful - Thu Mar 30 19:10:20 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	g39_lab4
Top-level Entity Name	g39_dealerTestBed
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	758 / 18,752 (4 %)
Total combinational functions	756 / 18,752 (4 %)
Dedicated logic registers	350 / 18,752 (2 %)
Total registers	350
Total pins	63 / 315 (20 %)
Total virtual pins	0
Total memory bits	3,328 / 239,616 (1 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

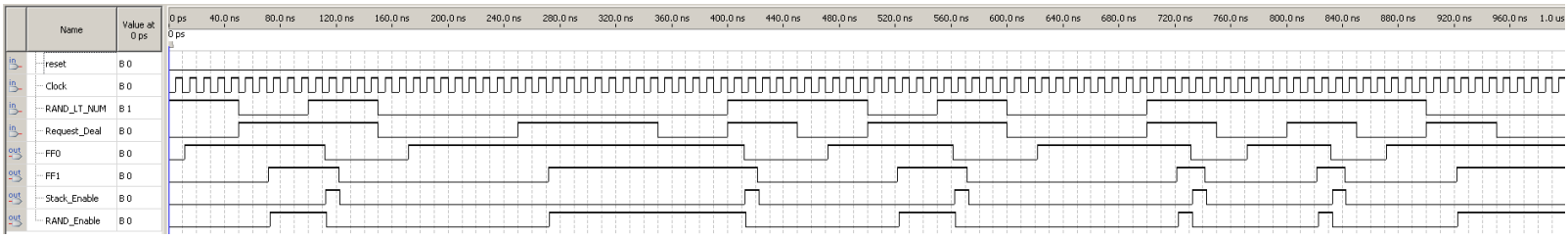
Timing:

Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-6.688	0.215	N/A	N/A	-1.814
1	clk	-6.688	0.215	N/A	N/A	-1.814
2	Design-wide TNS	-1750.061	0.0	0.0	0.0	-472.867
1	clk	-1750.061	0.000	N/A	N/A	-472.867

Simulations:

g39_dealerFSM:

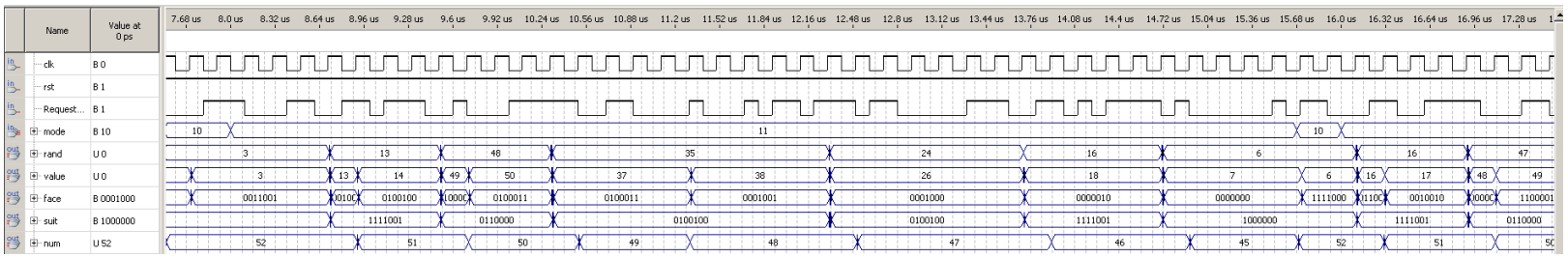


We can see that RAND_Enable = 1 only when state is C (FF1 = 1, FF0 = 1)

Stack_Enable = 1only when state is D (FF1 = 1, FF0 = 0)

Next state equations follow the table in g39_dealerFSM above

g39_dealTestBed:



We can see that the circuit is generating random address (“rand”) every time. The value displayed is the one at the same address after popping.