ECSE 323 – Digital System Design
g39_testbed

Description:

The testbed circuit puts together stack52, Modulo_13, 7_segment_decoder and single pulse generator circuits in order to later on upload it onto the Altera board and display the different outputs representing a card deck.

The circuit has the following inputs/outputs:

pushbutton: 1-bit input to enable the circuit, i.e. carrying out the operation selected
mode: 2-bit input representing the operation desired
addr: 6-bit input representing a location in the stack
rst: 1-bit input to create an empty hand
clk: 1-bit input

suit: 7-bit output representing the suit of *card*
card: 7-bit output representing the card at the input *address*

Implementation Details:

Sub-circuits:

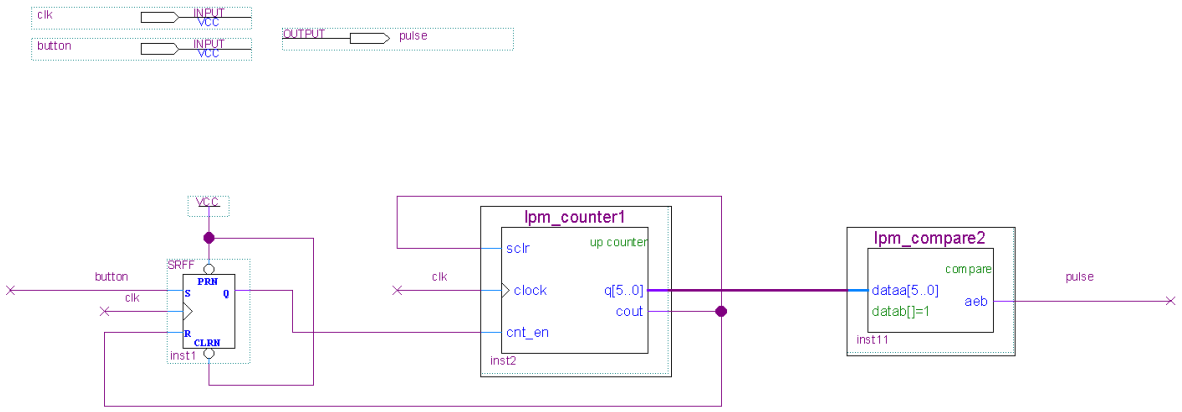
(Modulo_13, 7_segment_decoder and stack52 were explained in previous reports)

Single Pulse generator:

The main purpose of this circuit is to eliminate the de-bouncing effect explained in the lab description. To do so, we use an SR Flipflop, a counter and a comparator.

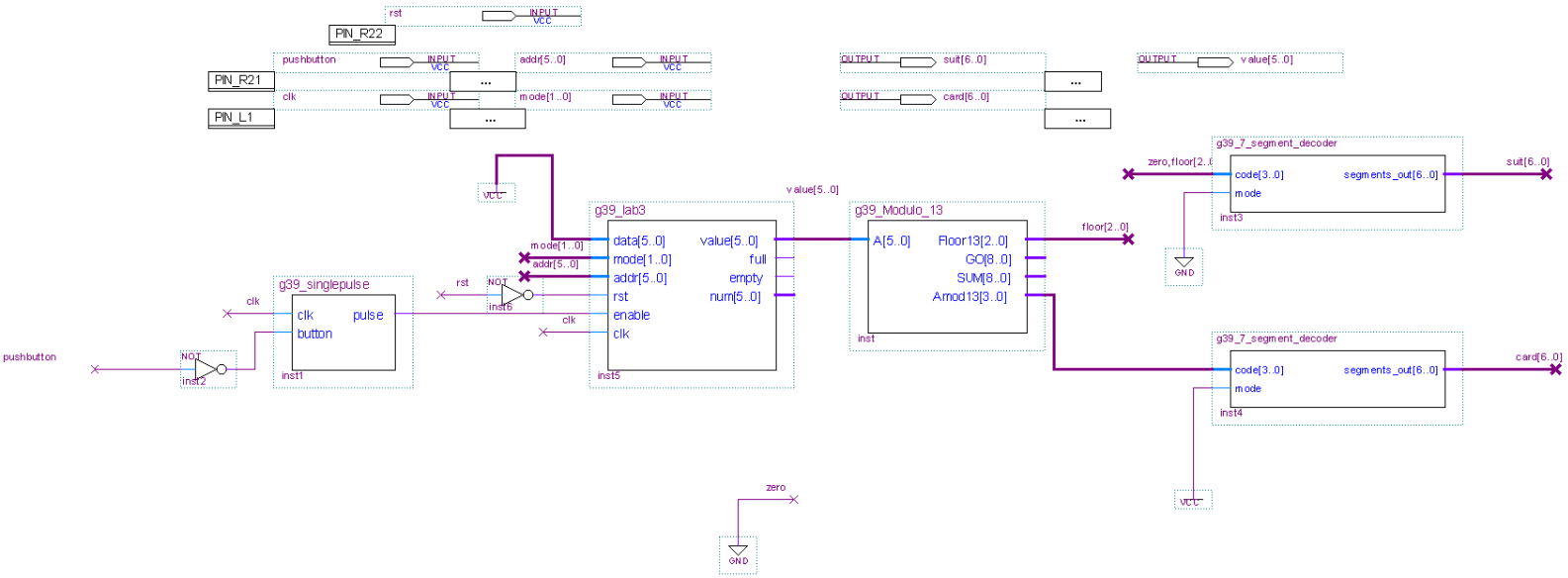
Logic:

- When a button is pushed S = 1, R = 0. So, the SR Flipflop sets Q to 1 and thus the counter is enabled.
- The counter then gets incremented to 1 and C_{out} = 0. This results in S=0, R=0 with Q_n = 1 which means the SR is in hold mode with Q_{n+1} = 1.
- The output of the comparator is compared with 1. This generates a pulse at this stage since output is 1.
- Pulse (output of comparator) is 0 for all subsequent increments since the output of the counter is not 1.
- Once the output of the counter exceeds the limit set (overflow takes place), C_{out} will become 1. This resets the SR Fliplop as well as counter waiting for the next button press.



Test_bed Logic:

- When a button is pressed, the stack52 is enabled and will carry out the operation specified.
- The output of the stack52 (VALUE) is now fed to Modulo_13 circuit.
- Modulo_13 outputs a floor representing a suit since floor(VALUE/13) where VALUE is 6-bits is 0, 1, 2, or 3 (4 values). The floor output is then fed to a 7_segment_decoder to display it on the board.
- Modulo_13 also outputs VALUEmod13 which takes 13 possible values representing the card (13 cards/suit). This is fed into a second 7_segment_decoder to display it on the board.



Testing:

Pin assignments:

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Differential Pair
addr[5]	Input	PIN_U12	8	B8_N0	PIN_U12	3.3-V LV...default)		24mA (default)	
addr[4]	Input	PIN_W12	7	B7_N1	PIN_W12	3.3-V LV...default)		24mA (default)	
addr[3]	Input	PIN_V12	7	B7_N1	PIN_V12	3.3-V LV...default)		24mA (default)	
addr[2]	Input	PIN_M22	6	B6_N0	PIN_M22	3.3-V LV...default)		24mA (default)	
addr[1]	Input	PIN_L21	5	B5_N1	PIN_L21	3.3-V LV...default)		24mA (default)	
addr[0]	Input	PIN_L22	5	B5_N1	PIN_L22	3.3-V LV...default)		24mA (default)	
card[6]	Output	PIN_D1	2	B2_N0		3.3-V LV...default)		24mA (default)	
card[5]	Output	PIN_D2	2	B2_N0		3.3-V LV...default)		24mA (default)	
card[4]	Output	PIN_G3	2	B2_N0		3.3-V LV...default)		24mA (default)	
card[3]	Output	PIN_H4	2	B2_N0		3.3-V LV...default)		24mA (default)	
card[2]	Output	PIN_H5	2	B2_N0		3.3-V LV...default)		24mA (default)	
card[1]	Output	PIN_H6	2	B2_N0		3.3-V LV...default)		24mA (default)	
card[0]	Output	PIN_E1	2	B2_N1		3.3-V LV...default)		24mA (default)	
clk	Input	PIN_L1	2	B2_N1	PIN_M2	3.3-V LV...default)		24mA (default)	
mode[1]	Input	PIN_L2	2	B2_N1	PIN_L2	3.3-V LV...default)		24mA (default)	
mode[0]	Input	PIN_M1	1	B1_N0	PIN_M1	3.3-V LV...default)		24mA (default)	
pushbutton	Input	PIN_R21	6	B6_N0		3.3-V LV...default)		24mA (default)	
rst	Input	PIN_R22	6	B6_N0	PIN_R22	3.3-V LV...default)		24mA (default)	
suit[6]	Output	PIN_E2	2	B2_N1		3.3-V LV...default)		24mA (default)	
suit[5]	Output	PIN_F1	2	B2_N1		3.3-V LV...default)		24mA (default)	
suit[4]	Output	PIN_F2	2	B2_N1		3.3-V LV...default)		24mA (default)	
suit[3]	Output	PIN_H1	2	B2_N1		3.3-V LV...default)		24mA (default)	
suit[2]	Output	PIN_H2	2	B2_N1		3.3-V LV...default)		24mA (default)	
suit[1]	Output	PIN_J1	2	B2_N1		3.3-V LV...default)		24mA (default)	
suit[0]	Output	PIN_J2	2	B2_N1		3.3-V LV...default)		24mA (default)	

Flow summary:

Flow Summary

Flow Status	Successful - Sun Mar 19 17:43:03 2017
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	g39_lab3
Top-level Entity Name	g39_testbed
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	679 / 18,752 (4 %)
Total combinational functions	679 / 18,752 (4 %)
Dedicated logic registers	325 / 18,752 (2 %)
Total registers	325
Total pins	31 / 315 (10 %)
Total virtual pins	0
Total memory bits	3,328 / 239,616 (1 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

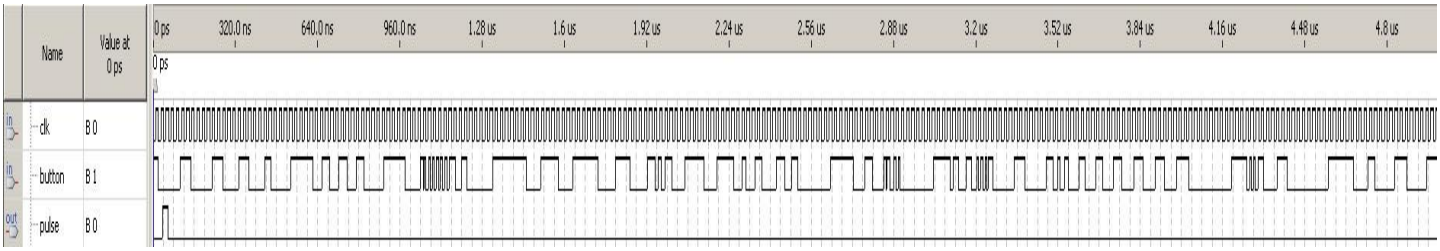
Timing:

Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-5.138	0.215	N/A	N/A	-1.814
1	clk	-5.138	0.215	N/A	N/A	-1.814
2	Design-wide TNS	-1514.226	0.0	0.0	0.0	-442.317
1	clk	-1514.226	0.000	N/A	N/A	-442.317

Simulations:

Single pulse generator:



testbed: