BIRICHA DIGITAL

Voltage Mode with Voltage Feedforward and Current Mode Control Methods

Detailed Implementation & Control Loop Design

Material to Cover in this Section

- Problems with standard voltage mode control and how to improve them
- Voltage mode with voltage feedforward
  - Control loop design with WDS
- Peak current mode control
  - Subharmonic oscillation & slope compensation
  - Leading edge blanking
  - Current gain and current measurement
  - Right-hand plane zero and its impact on phase margin
- Peak current mode control loop design
  - Loop design with Transconductance amplifiers
- Labs

Fixed Frequency Power Supply Control Methods Recap

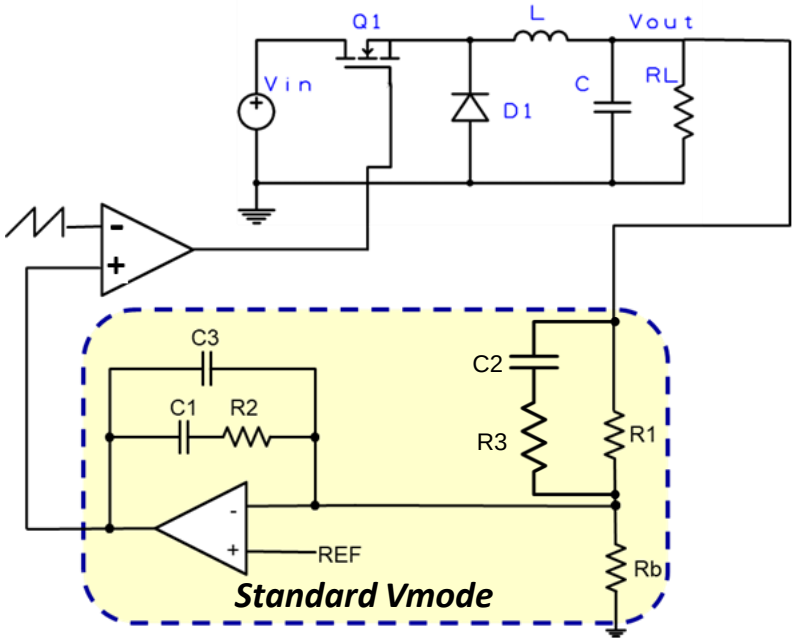
- Standard Voltage Mode (Vmode)
  - Buck/Forward topologies
  - Fixed Frequency - one control loop
  - Measure Vout and compare with Vref and then compensate to get new value of PWM
- Voltage Mode with *Input* Voltage Feedforward Vmode+VFF
  - Buck/Forward topologies
  - Measure input voltage and incorporate it in the control loop
  - Gives better line regulation
- Current Mode → Boost/Flyback/SEPIC/Cuk…. and Buck
  - Fixed Frequency + two control loops
    - Outer loop controls the voltage and the inner loop controls peak (most commonly) inductor current
  - Has advantages over Voltage mode
  - Also has headaches such as sub-harmonic oscillations, needs ramp compensation

There are 2 main sub-categories:

1 - Peak Current Mode Control for DC/DC PSUs
&
2 - Average Current Mode Control for PFCs

Today we will cover Peak CMC
We will cover Average CMC during the PFC day

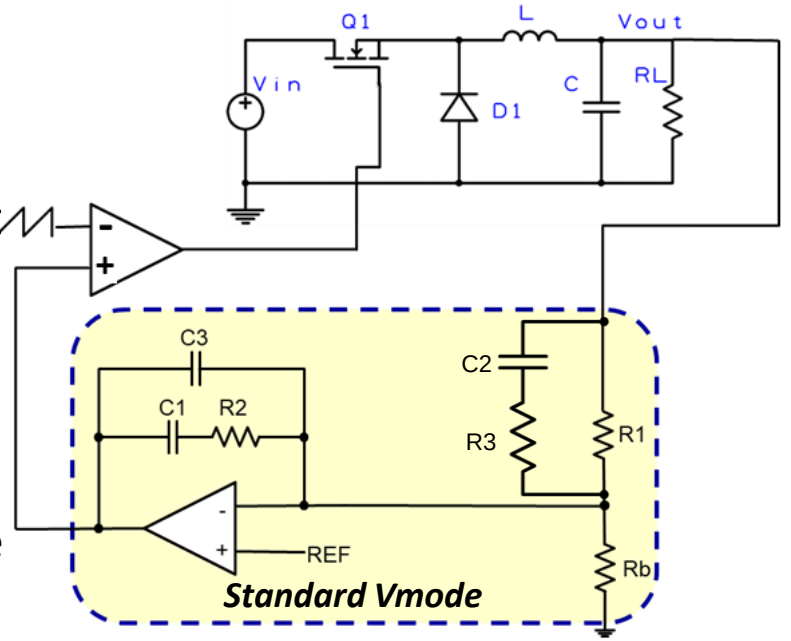
So What Was Wrong with Standard Voltage Mode?



- There are several issues but here are the main ones:
  - 1 - Although our control loop knows exactly what is happening on the output, it doesn't "directly" know what is happening on the input
    - A change in Vout will get immediately detected by the control loop
      - i.e. standard Vmode has very good load regulation
    - A change in Vin, however, needs to go through the massive time constant of the LC stage before it manifests itself as a change in Vout on the output
      - i.e. standard voltage mode is very slow to react to changes Vin → it has poor line regulation
  - 2 - Please recall that $\frac{V_{in}}{V_{RAMP}}$ appears in the transfer function of the standard Vmode PSU
    - If Vin halves so will our crossover frequency Fx…. and if Fx halves our recovery time after a transient will get much slower
    - If Vin doubles, Fx will also double, potentially causing instability
    - i.e. transient response changes with Vin → that is not a good thing!

So What Was Wrong with Standard Voltage Mode?

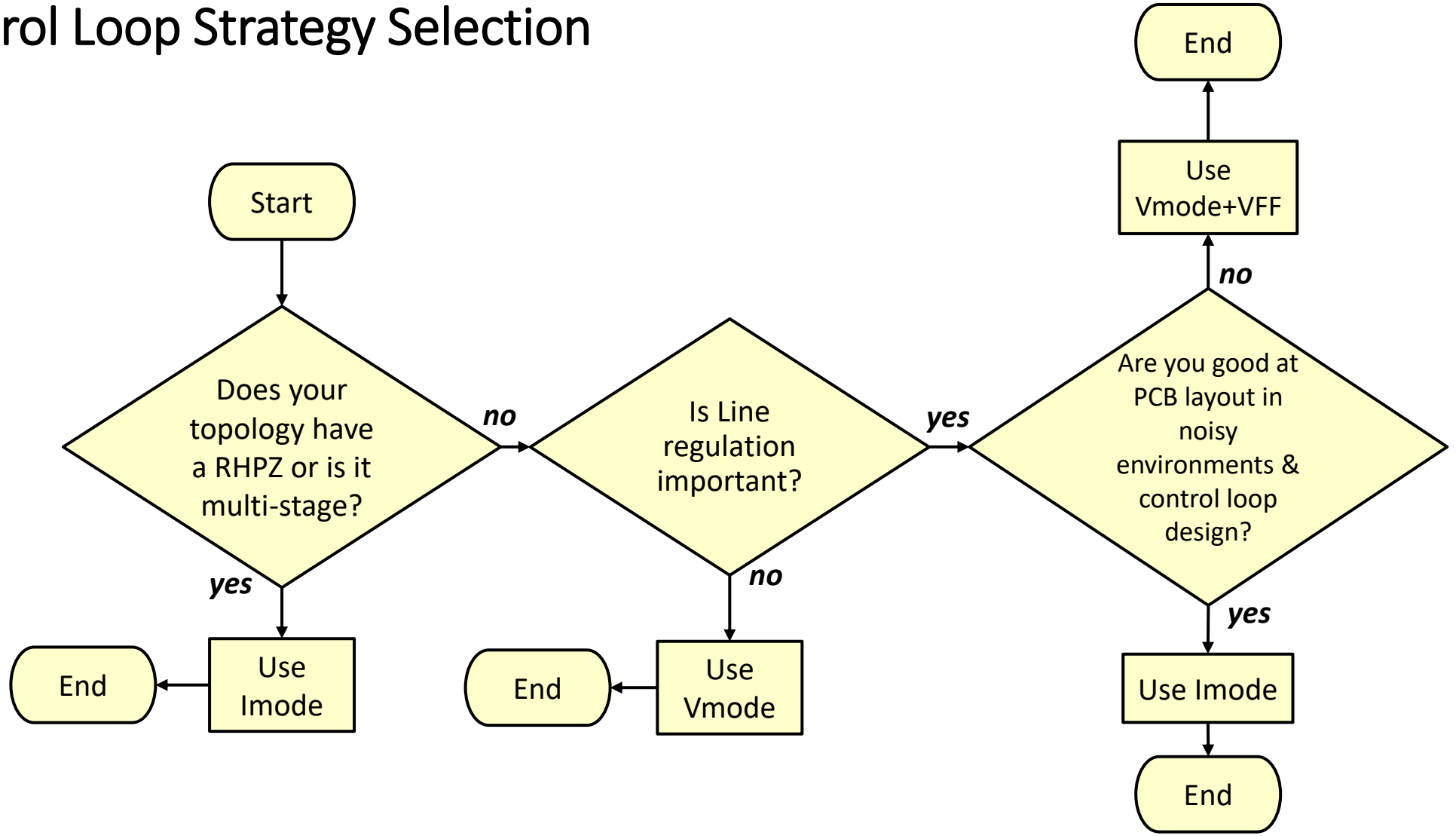
- 3 - We are not measuring the current → no information about current means no current limiting
  - If we have to measure the current anyway for safety, why not use it in the control loop?
  - Note that current measurement for safety is much simpler than current measurement for control loop stability and often is done internally in the PWM controller → so this is not a big deal
- 4 - Can not use Vmode with any topology that has a Right Hand Plane Zero (RHPZ)
  - We will talk about RHPZ soon
- 5 - Can't current share in multi-stage/interleaved PSUs with Vmode
  - In Vmode there will be conflict between the control loop of each stage as to which one controls Vout
  - If we have one global loop for Vout and a local current loop per stage we solve this problem



How Do We Solve the Problems with Standard Vmode?

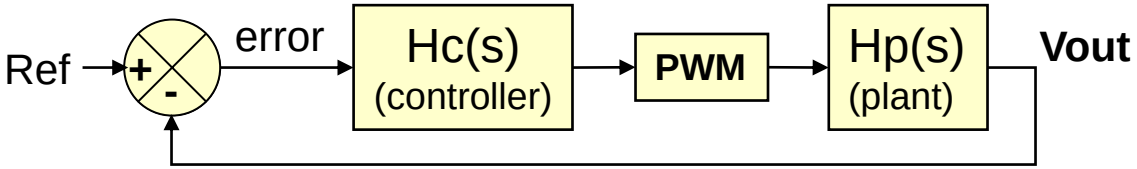
- To solve problems 1 & 2 we clearly need to take a measure of our input and somehow incorporate it in our control loop
- Engineers invented 2 methods to do this:
  - Voltage Mode with Input Voltage Feedforward (Vmode+VFF)
    - Measures Vin and incorporates into the control loop
  - Current Mode Control (Imode)
  - Measures the inductor current and incorporates into the control loop
    - Peak current mode → DC/DC PSUs
    - Average current mode → PFCs
- Vmode+VFF solves the first 2 problems
  - You still can not use it for topologies with a RHPZ
  - You still can not current share in multi-stage converters
  - You still have a current limiting issue → easy to solve
- Current mode solves all of the 5 issues identified in the previous slides
  - But, as with anything else in engineering, it has its drawbacks
    - In particular, clean current measurement, subharmonic oscillations and slope compensation is a real pain!

Control Loop Strategy Selection



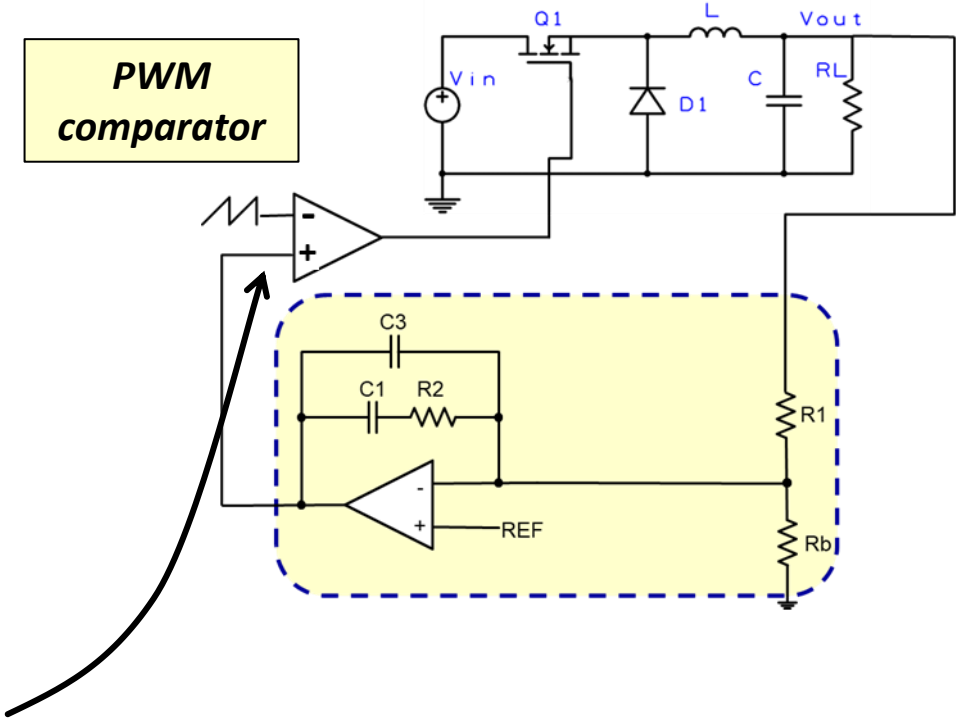
Voltage Mode with Input Voltage Feedforward

- From previous discussions we know that:

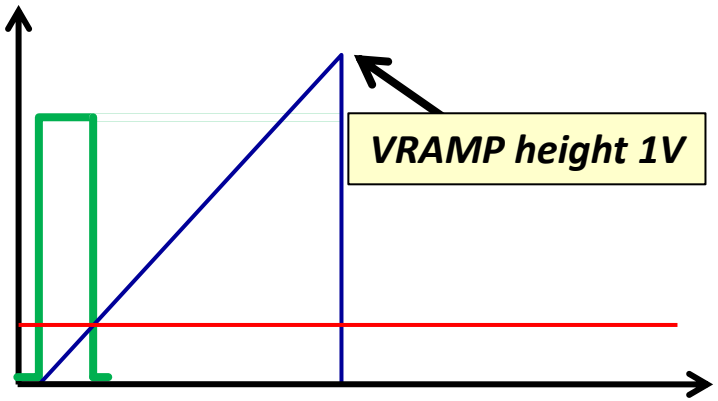


$$Gain_{PWM} = \frac{V_{in}}{V_{RAMP}}$$

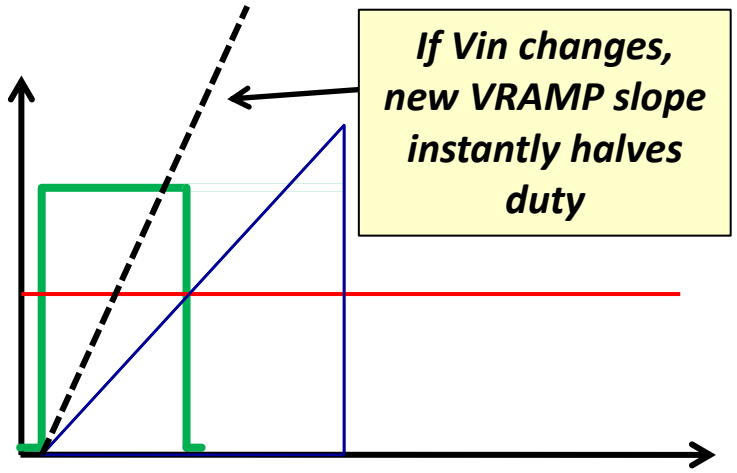
$$Vout = Duty.Vin$$



- We also know that the PWM is generated by comparing our reference from the compensator with a ramp voltage VRAMP in a comparator
  - Red trace = reference
  - Blue trace is our = VRAMP
  - Green trace = our generator PWM



Voltage Mode with Input Voltage Feedforward



- So if Vin suddenly doubles, our PWM gain will suddenly double and therefore our crossover frequency Fx will double
  - Vout will initially rise, after this the control loop will detect the rise in Vout and reduce duty → this process is slow
- In order to solve this a Vmode + VFF PWM IC will internally and automatically make the ramp height proportional to Vin

$$Gain_{PWM} = \frac{V_{in}}{V_{RAMP}.k.Vin} \rightarrow Gain_{PWM} = \frac{1}{k.VRAMP}$$

- You can see that now PWM Gain is independent of Vin
  - Now if Vin doubles, the slope of the ramp height will also double and duty will instantaneously halve independent of the control loop
  - Scaling factor k is specified in the datasheet

Design Example with LM27402 Vmode + VFF PWM Controller*

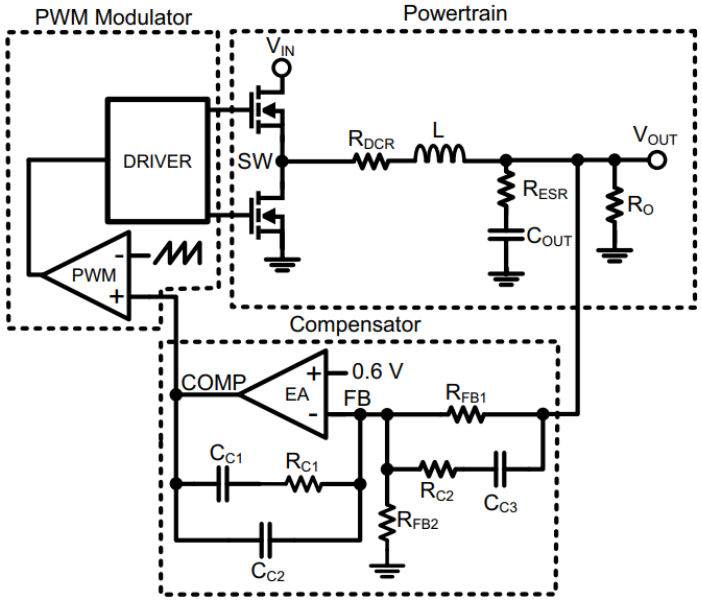


Figure 35. Control Loop Schematic Diagram

The power train consists of the filter inductor (L) with DCR (R_{DCR}), output capacitor (C_{OUT}) with ESR (effective series resistance R_{ESR}), and effective load resistance (R_O). The error amplifier (EA) regulates the feedback (FB) voltage to 0.6V. The passive compensation components around the error amplifier establish system stability. Type-III compensation is shown in Figure 35. The PWM modulator establishes the duty cycle command by comparing the error amplifier output (COMP) with an internally generated ramp set at the switching frequency.

The modulator gain, power train and compensator transfer functions must be taken into consideration when obtaining the total open-loop transfer function. The PWM modulator adds a DC gain component to the open-loop transfer function. In a basic voltage-mode system, the PWM gain varies with input voltage. However the LM27402 internal voltage feedforward circuitry maintains a constant PWM gain of 7:

$$G_{PWM} = \frac{1}{k_{FF}} = 7 \quad (15)$$

All we have to do is to take this into account in WDS

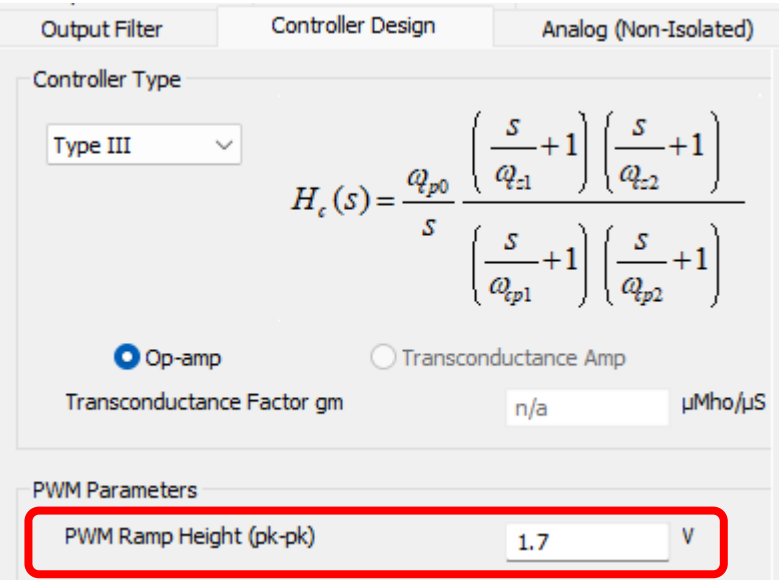
* Taken from device datasheet: https://www.ti.com/lit/ds/symlink/lm27402.pdf?ts=1710160279235

Design Example with LM27402 Vmode + VFF PWM Controller

- From the datasheet of the device we know that PWM gain is fixed at 7
- Following from our previous Lab example, our nominal Vin was 12V and we know that:

$$Gain_{PWM} = \frac{V_{in}}{V_{RAMP}} \rightarrow 7 = \frac{12V}{VRAMP} \therefore \text{effective VRAMP} = \frac{12V}{7} = 1.7V$$

- In WDS under Controller Design tab, set the ramp height to the effective VRAMP above and we are done ☺



However, this control method does not solve our other issues
We still have a current sharing and RHPZ problem
Note that current limiting is now done easily in most modern Vmode ICs so not a big deal

Analog Peak Current Mode

- We control the peak of the inductor current
  - We have two loops
  - An outer voltage loop regulating Vout and an inner current loop controlling the peak of the inductor current → a change in Vin will very quickly change this current
- Advantages vs Voltage Mode:
  - Better line regulation
  - Easier to parallel
  - Much better transition between Discontinuous Conduction Mode (DCM) and Continuous Conduction (CCM)
  - Can deal with topologies with right-hand plane zero (e.g. CCM Flyback, Boost, etc.)
  - Current limiting comes free
  - Maintains flux balance in push-pull converters → not very common these days
- Disadvantages
  - Plant model is complex
  - Current sensing is difficult, sensitive to layout, noisy, expensive, needs more circuitry, can be inaccurate or lossy
  - Needs leading edge blanking → there is a minimum duty limit due to this
  - Under continuous conduction mode (CCM), can have sub-harmonic oscillations and must add a compensating ramp

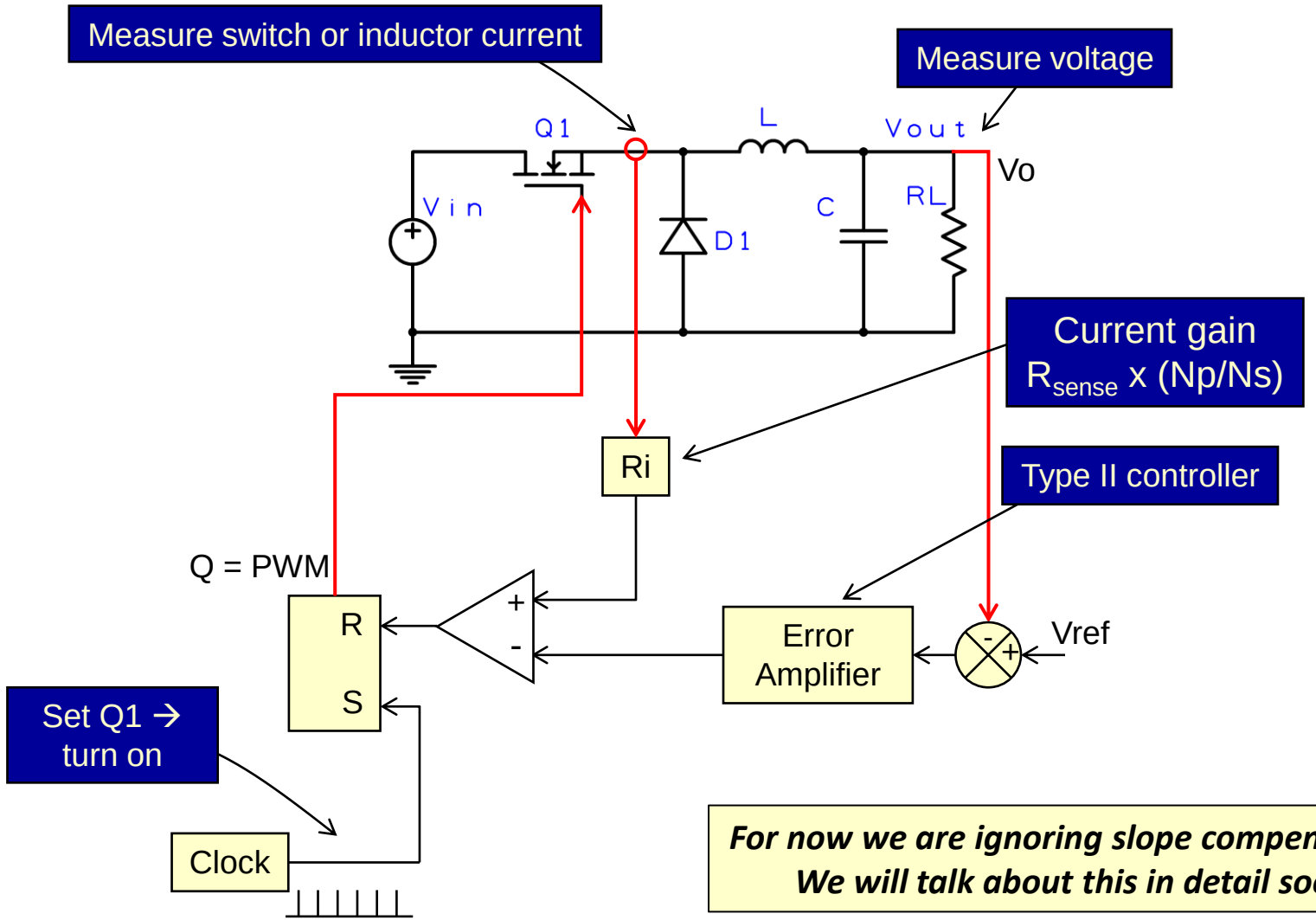
Current mode address all 5 problems that we discussed earlier … but it has some headaches!

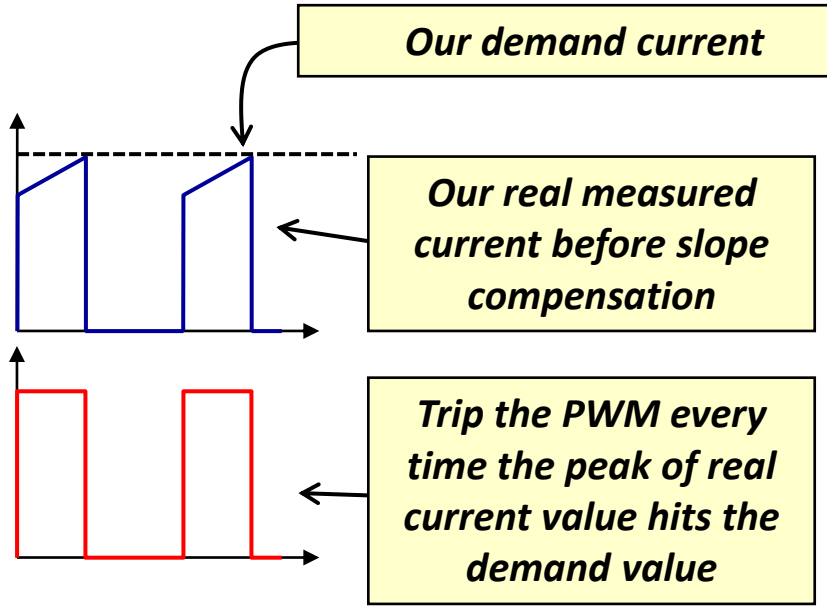
Analog Peak Current Mode

$$H_c(s) = \left(\frac{\omega_{p0}}{s}\right) \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right)}{\left(\frac{s}{\omega_{p2}} + 1\right)}$$

- Transfer function is very complex
  - There are several different models
  - The experts can not agree on the model. There are arguments about which one is correct!
  - We use Ridley's model as it seems to fit well
- Under current mode the system behavior "appears" first order at lower frequencies, like a single pole low pass filter
  - i.e. no double pole resonance and no 180^o phase loss
  - You only need a Type II controller → because there is no 180^o phase loss
  - So we need to calculate the positions of the controller's zero (fz1) and poles (fp0 & fp2) in Hz or if given in ω then in rad/s
- But under CCM, there could be subharmonic oscillations for duties bigger than 50%
  - In practice these can happen at much lower duties
  - In order to overcome this, we add a ramp with a positive slope to the measured inductor current before being fed into the op-amp
  - Note that the switch current is often used instead of the inductor current as it is much easier to measure → peak of the switch current is the same as the peak of the inductor current
  - This is called slope compensation

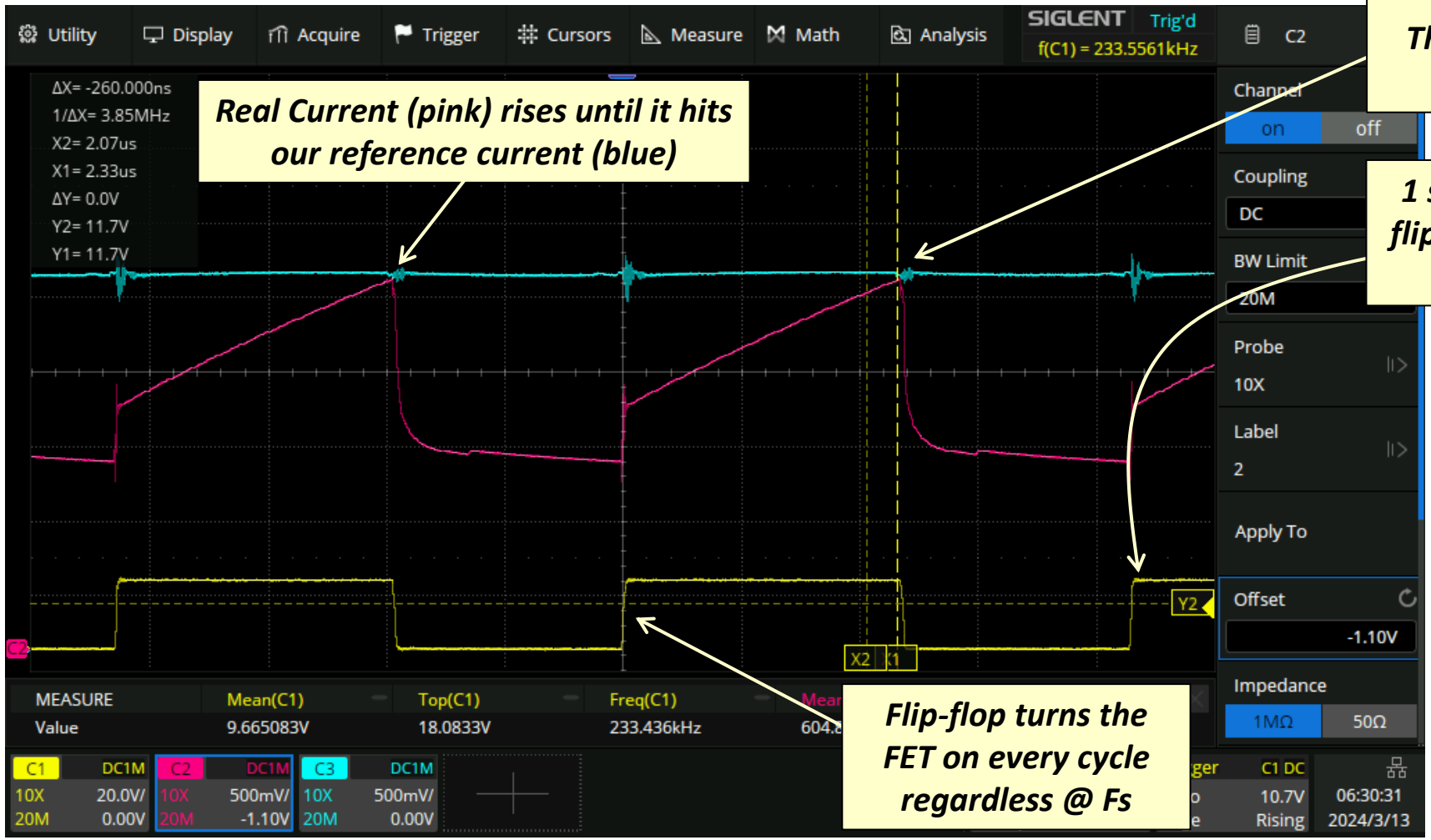
Analog Peak Current Mode Operation





For now we are ignoring slope compensation
We will talk about this in detail soon

Analog Peak Current Mode Operation



When our real current is equal to our reference current, the flip-flop resets and turns FET off

Therefore we are controlling the peak of the inductor current*

1 switching cycle later, the flip-flop will turn on the FET again

* Note there is some propagation delay and an internal 1.1 to 1.4V off-set – please see device datasheet here:
https://www.ti.com/lit/ds/symlink/uc3825a.pdf?ts=1710244414189&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FUC3825A%253FkeyMatch%253D3825