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Final Project Report

ADP1071-1EVALZ Flyback Converter

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Contents

1. Abstract

This report presents a comprehensive evaluation of the ADP1071-1 isolated synchronous flyback controller using the ADP1071-1EVALZ evaluation board from Analog Devices. The ADP1071-1 integrates iCoupler technology for signal isolation and provides dedicated primary and secondary side MOSFET drivers, making it suitable for multi-output isolated power supply designs targeting industrial applications.

The project's main goal is to understand the structure and the operation of the system from the datasheet and to validate its performance experimentally through electrical measurements. Several tests were conducted, including output-voltage regulation under varying input voltage conditions and load regulation for multiple regulated outputs. In addition, the circuit was simulated to further analyze and understand it.

2. Introduction

Isolated flyback converters are widely used in embedded and industrial power systems due to their ability to provide galvanic isolation and generate multiple output rails using a single transformer-based topology. Their flexibility and compact implementation make them suitable for applications where different voltage levels are required while maintaining isolation for safety and noise immunity.

The ADP1071-1 is an integrated isolated flyback controller, and the ADP1071-1EVALZ evaluation board provides a fully documented reference implementation for a multi-output isolated power supply. The purpose of this project is to evaluate the board architecture and experimentally validate its performance through systematic regulation measurements and analysis. The work emphasizes practical characterization and provides engineering insight into expected behavior of multi-output flyback converters.

3. Datasheet Review

3.1 Evaluation Board Overview

The evaluation board is set up to act as an isolated power supply solution that incorporates three output voltages (+5.5 V, +24 V, and −15 V) at a total rated power of 15 W. The evaluation board also provides 5 kV isolation in compact form factors.

The DC voltage source should supply a range of $18V_{DC}$ to $32V_{DC}$ with a 1A current output capability.
The ADP1071-1 controller operates at a switching frequency of $50\ kHz$.The switching frequency minimizes switching losses of the converter and is high enough to keep the transformer size small.

3.2 Key Specifications
A summary of key parameters of the evaluation board

Parameter	**Value**
Input Voltage Range	[18 V: 32 V]
Switching Frequency	[50 kHz]
Output 1	+24 V @ 400 mA (9.6 W max)
Output 2	+5.5 V @ 500 mA (2.75 W max)
Output 3	−15 V @ 200 mA (3 W max)
Total Output Power	[15 W]
Isolation Voltage	[5 kV]

3.3 ADP1071-1's Pin Configuration & Function
3.3.1 Primary side

- GATE: This is the driver output for the MOSFET on the primary side(Q3). The pin is a multiple function pin where the controller determines the duty cycle of the gate switching on the MOSFET.
- AGND1: The common ground on the primary side.
- VREG1: Powers the internal circuitry, primary side iCouplers, housekeeping circuits, and the primary MOSFET driver at the GATE pin. This pin needs to be powered by an external power up circuit.
- MODE: sets the operating mode of the transformer: CCM or LLM (light load mode). LLM is power saving mode where the controller significantly lowers the output current on the secondary side. The transformer can be forced to CCM by connecting the pin to low voltage (preferably AGND1) and to LLM by connecting to high voltage($\leq 2.5\ V$).

- EN: Precision Enable Input. The controller is enabled when EN is above the EN threshold voltage
- CS: Current Sense Input. This pin monitors the primary current through the sense resistor (R15). The voltage on this pin is used for cycle-by-cycle current limiting, overcurrent protection, and input current regulation.
- RT (Pin 7): Switching Frequency Setting
  This pin sets the switching frequency through an external resistor to AGND1. The resistor value determines the oscillator frequency. For the evaluation board, the RT resistor sets the frequency to 50 kHz. The relationship between resistor value and frequency is defined in the datasheet.

- SYNC (Pin 8): External Synchronization Input
  Allows the converter to synchronize to an external clock signal. When driven with an external signal, the internal oscillator locks to the external frequency. This feature is useful in systems where multiple converters need to operate in phase or to avoid interference with sensitive circuits. Leave floating for free-running operation.

3.3.2 Secondary Side

- SS2 (Pin 9): Soft-Start Control

  This pin controls the soft-start timing through an external capacitor. The capacitor charges from an internal current source, setting the soft-start duration. The ADP1071-1 implements a two-stage soft-start: first limiting the inrush current, then gradually increasing the duty cycle. The soft-start time is calculated as:

  $$t\_ss = (C\_ss \times V\_ss) / I\_ss$$

- COMP (Pin 10): Compensation Network Connection
  This is the output of the error amplifier and the connection point for the compensation network. External components (typically RC network) connected to this pin set the control loop characteristics including bandwidth, phase margin, and transient response. The evaluation board uses C59 (470pF), R56 (46.4kΩ), and C40 (10nF) for loop compensation.

- FB (Pin 11): Feedback Input
  This pin receives the combined feedback signal from the secondary side outputs. The ADP1071-1EVALZ uses a weighted feedback network where the +5.5V and +24V outputs are sensed with a 60:40 ratio. The feedback voltage is compared against an internal reference (typically 1.25V) to regulate the outputs. The resistor network consists of R20, R21, R23, and R24.

- OVP (Pin 12): Overvoltage Protection
  Monitors the output voltage for overvoltage conditions. When the voltage on this pin exceeds the OVP threshold (typically 1.31V), the controller immediately shuts down to protect downstream circuitry. The converter enters hiccup mode and periodically attempts to restart. Reset occurs when the OVP condition is cleared.

- VDD2 (Pin 13): Secondary Side Supply
  Powers the secondary side circuits including the synchronous rectifier driver and secondary side iCoupler circuits. Typically powered from one of the output rails through a voltage divider or linear regulator. On the evaluation board, this is connected to the regulated output through the feedback network.

- VREG2 (Pin 14): Secondary Side Regulated Supply
  This is the internally regulated supply for the secondary side analog circuits. Generated from VDD2 through an internal LDO regulator. Typically provides a stable voltage reference for secondary side operation. Requires a bypass capacitor to AGND2 for stability.

- AGND2 (Pin 15): Secondary Side Analog Ground
  The analog ground reference for all secondary side circuits. This ground is isolated from the primary side ground (AGND1) and is referenced to the secondary output ground.

- SR (Pin 16): Synchronous Rectifier Drive
  This pin provides the gate drive signal for the synchronous rectifier MOSFET on the secondary side. The ADP1071-1 uses integrated iCoupler technology to transmit timing information across the isolation barrier without requiring an opto-coupler. The SR driver is synchronized with the primary side switching to enable the synchronous rectifier at the optimal time, improving efficiency by reducing rectification losses.

3.4 **Protection Features**

•Short-circuit protection: The controller monitors the FB pin. If the feedback voltage drops significantly, indicating a short circuit condition, the controller enters a hiccup mode to prevent damage.

•Output overvoltage protection (OVP): The OVP pin monitors the output voltage. If the voltage exceeds the OVP threshold, the controller shuts down the converter to protect downstream circuitry.

•Cycle-by-cycle overcurrent protection: The CS pin monitors primary current. If the current exceeds the threshold during any switching cycle, the gate drive is immediately terminated for that cycle.

•Overtemperature protection: An internal thermal sensor monitors the die temperature. If temperature exceeds 150°C, the controller shuts down and enters thermal hiccup mode.

•Undervoltage lockout (UVLO) with hysteresis: The VREG1 pin is monitored for undervoltage conditions. The controller remains off until VREG1 rises above the UVLO rising threshold (typically 9.9V) and shuts down if it falls below the falling threshold (typically 8.1V), providing hysteresis to prevent chattering.

3.5 **Schematic Analysis**

3.5.1 Primary Side

The primary side includes the input filter, the switching MOSFET, and protection circuits:
Input capacitor bank: **C24–C57**
Switching MOSFET: **Q3**
Snubber network: **D11 + D12**
Current sensing resistor: **R15**

The snubber reduces voltage overshoot across the MOSFET, and the current sense resistor enables monitoring of primary current for control and protection.

3.5.2 Transformer

The transformer T1 (part number 750316825) features a 5-winding configuration providing isolation and multiple output voltages:
• Primary winding (Pins 4-3): Handles the input power transfer from the primary side
• Auxiliary winding (Pins 2-1): Provides power to VREG1 pin for the controller's internal circuits after startup
• 24V output winding (Pins 6-7): Secondary winding for +24V output, rated at 400mA maximum
• 5.5V output winding (Pins 8-9): Secondary winding for +5.5V output, rated at 500mA maximum
• -15V output winding (Pins 9-10): Secondary winding for -15V output, rated at 200mA maximum

3.5.3 Secondary Side

On the secondary side, each output stage includes diode rectification and RC snubbing.
Each output is filtered using capacitor pairs:
+24 V rail: C60, C65
+5.5 V rail: C62, C66
−15 V rail: C7, C67

3.5.4 Feedback & Compensation

The ADP1071-1 implements a multi-output feedback architecture where output regulation is achieved through weighted sensing of the +5.5 V and +24 V rails. The feedback network combines these two outputs with a 60-40 weightage ratio, prioritizing the +5.5 V rail for tighter regulation. The −15 V output is quasi-regulated, relying on transformer coupling rather than direct feedback control.

Feedback Network:

• The FB pin voltage is set to 1.2 V under nominal conditions through a resistive divider network (R23, R24, R20, R21) that samples both the +5.5 V and +24 V outputs
• The feedback signal is processed by an internal transconductance (gm) amplifier with a gain of approximately 250 μS
• The output of the gm amplifier connects to the COMP pin, which serves as the compensation node.

Compensation Circuit:

• The COMP pin requires an external RC network for loop stability
• A series resistor-capacitor combination (typically with an additional high-frequency pole capacitor in parallel) creates the necessary phase margin
• The COMP voltage represents the required peak current limit to maintain regulation and is transmitted across the isolation barrier via integrated iCoupler technology to control the primary-side PWM

Soft Start:

• The SS2 pin controls the secondary-side soft start sequence through a capacitor charged at 20 μA
• During startup, SS2 provides the reference voltage instead of the fixed 1.2 V reference, allowing the output to ramp smoothly
• The soft start time is determined by the formula we referenced earlier.

This feedback architecture eliminates the need for traditional optocouplers, improving reliability and reducing component count while maintaining isolation through the integrated iCoupler technology.

4. Circuit Testing

Test Equipment

Equipment	Specifications
DC Power Supply	0-30 V, 1 A
Electronic Load	Up to 15 W
Precision Digital Multimeter	Accuracy up to 0.01mV
Crocodile & banana test leads	-

Test Setup

The board was tested using the following procedure:
Connect the input DC source to J2.
Connect loads to the output connector J5.
Connect voltmeters to the outputs and input.
Apply the selected input voltage.
Perform sweeps:
Vin sweep (no load)
-Load sweeps for each output
Record measurements for each operating point.

The procedure follows the evaluation described in the user guide.

Test Procedures & Results

4.2.1 V_{out} vs V_{in} $(No\ Load)$

A sweep of the input voltage was performed between 0 V and 30 V under no-load conditions. This test evaluates the ability of the converter to maintain regulated output rails across the specified input range.

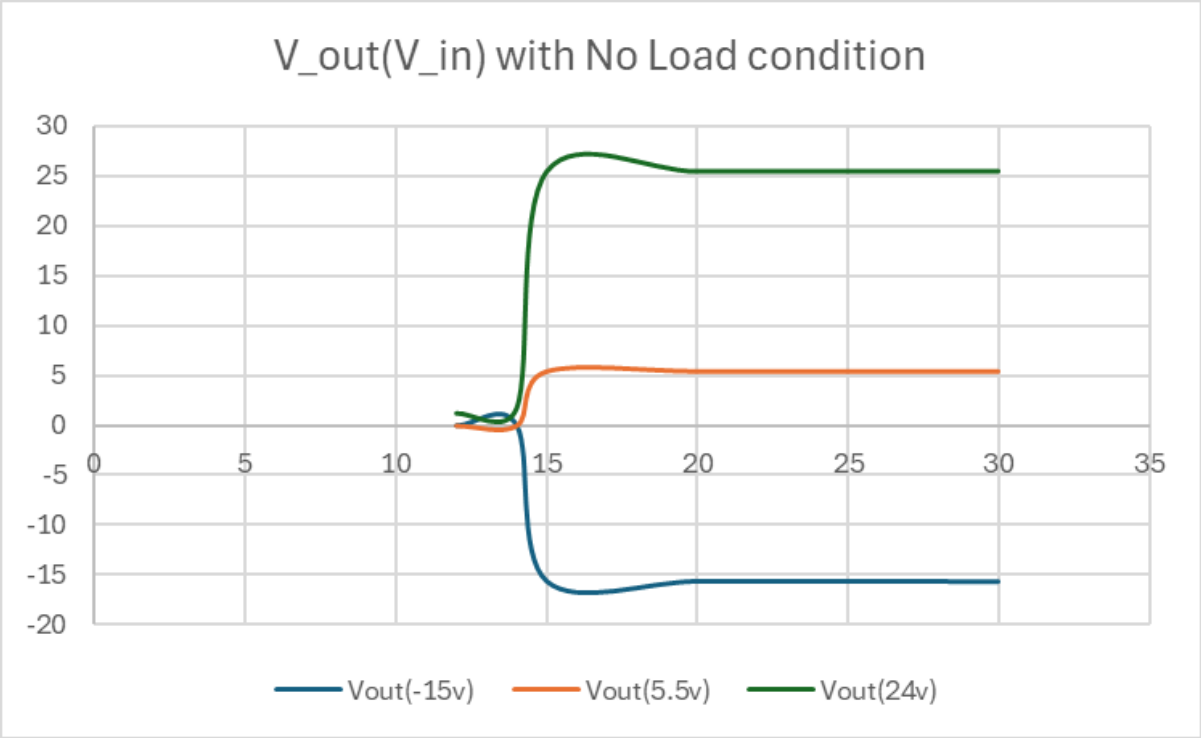


Figure1: Output voltage as a function of the input voltage under no Load conditions

Observation**:** The rails remain approximately constant within the operating range, indicating stable regulation.

Cross Regulation Testing

4.2.1.1 +24V Output

The +24 V output rail was measured under increasing load conditions.

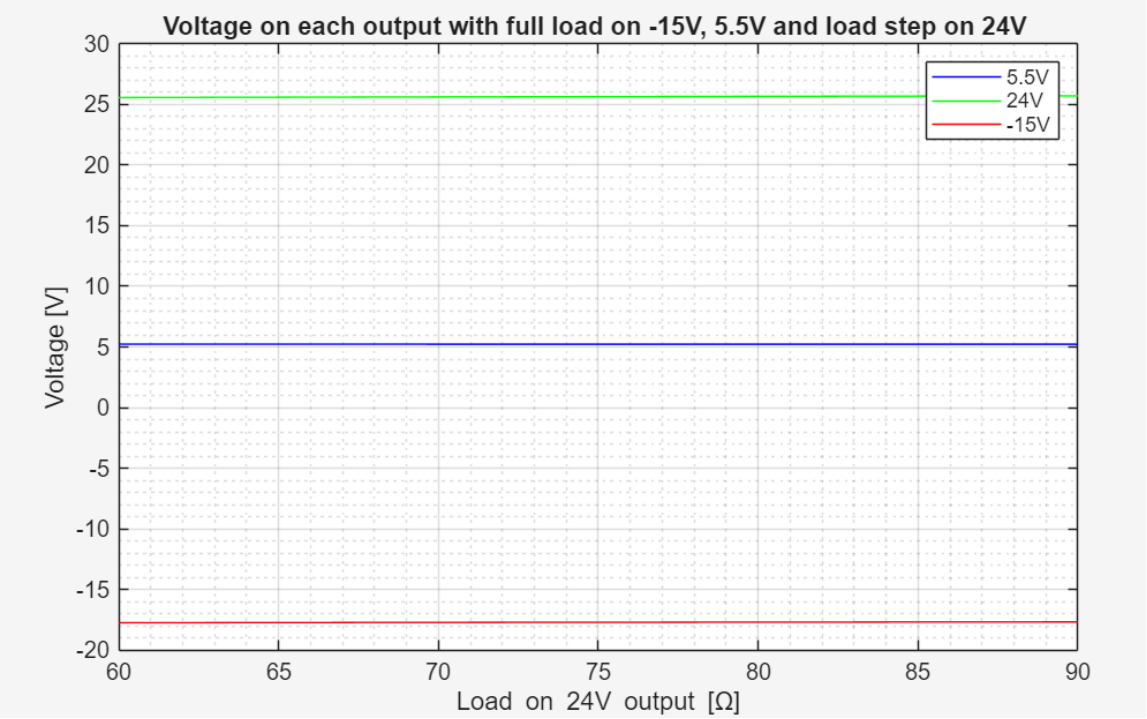


Figure 2: outputs voltages under full load on 5.5V & -15V with varying loads on 24V

Reference Behavior:
According to the ADP1071-1EVALZ user guide, the +24 V rail is one of the primary regulated outputs and is included in the feedback loop with a defined weightage. Therefore, tight load regulation is expected across the rated load range.

Comparison and Discussion:
Comparison between the measured results and the reference behavior from the datasheet shows a similar regulation trend. The measured output voltage remains relatively stable as the load increases, with only a small voltage droop at higher load levels. This behavior is consistent with the expected regulation characteristics described in the user guide and confirms correct operation of the feedback mechanism for the +24 V rail.

Power vs load resistance:

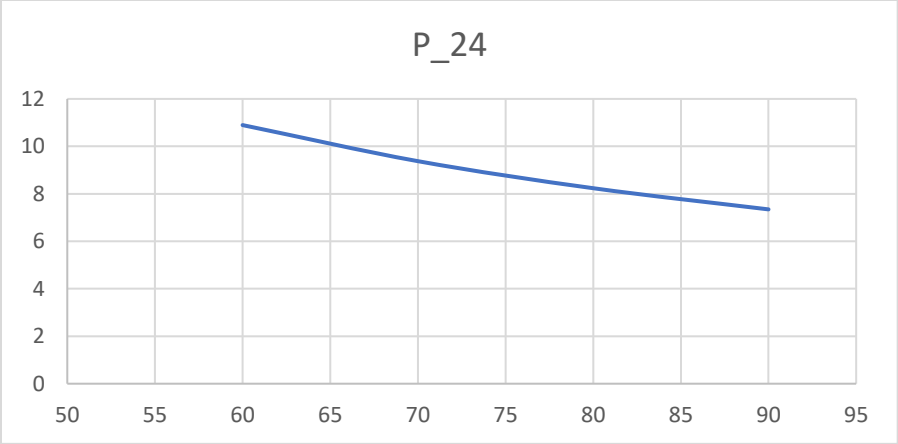


Figure 3: Power vs. resistance on 24V

The power graph depicts expected behavior. Theoretically, the power should decrease as the load increases as per the equation: $P = \frac{V^2}{R}$. Since the voltage should be constant, we expect the power graph to act like the function $\frac{1}{x}$, where x is the resistance. And in fact, the measured value acts in the expected way.

4.2.1.2 +5.5 V Output

The +5.5 V output rail was measured under variable load conditions

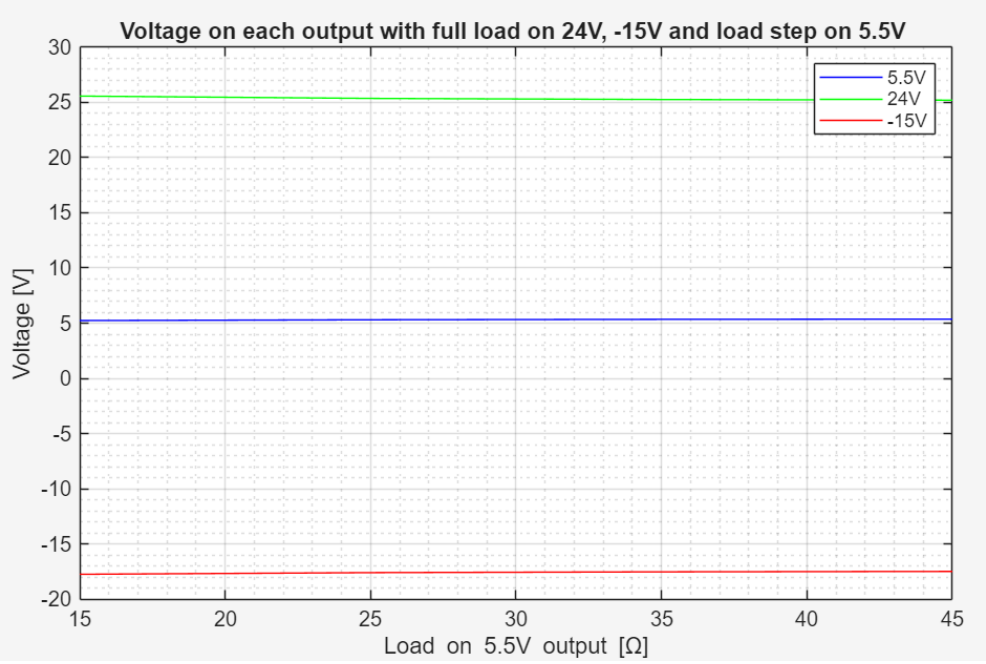


Figure 4: outputs voltages under full load on 24V & -15V with varying loads on 5.5V

Reference Behavior:
The +5.5 V rail is also part of the main feedback loop and is weighted more heavily than the +24 V rail, according to the user guide. As a result, it is expected to exhibit tight regulations across load variations.

Comparison and Discussion:
The measured load regulation behavior of the +5.5 V rail closely follows the expected trend from the datasheet. The output voltage remains well-regulated across the tested load range, showing minimal deviation from the nominal value. The agreement between measured and reference behavior validates the weighted feedback design implemented in the evaluation board.

Power vs load resistance:

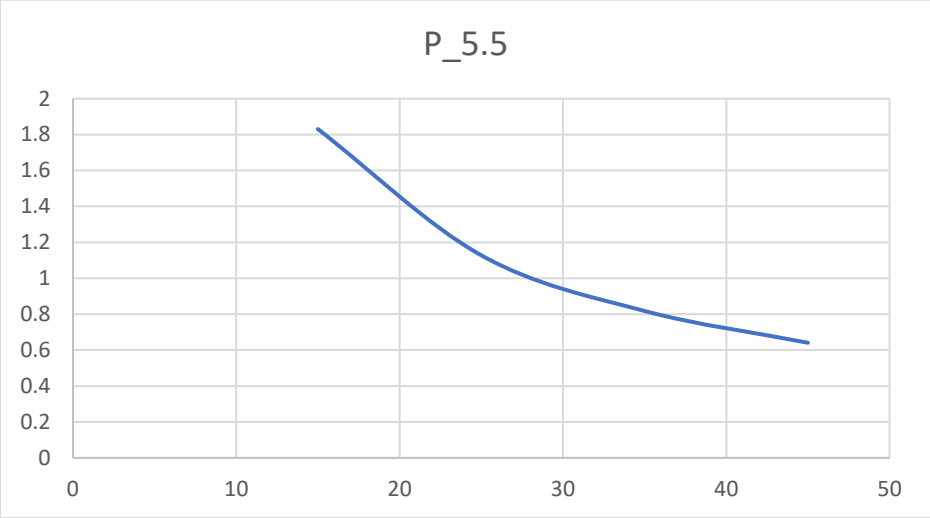


Figure 5: Power vs. resistance on 5.5V

The power graph acts as expected like we explained previously.

4.2.1.3 −15 V Output

The −15 V output rail was measured under increasing load, as shown in Figure 4.

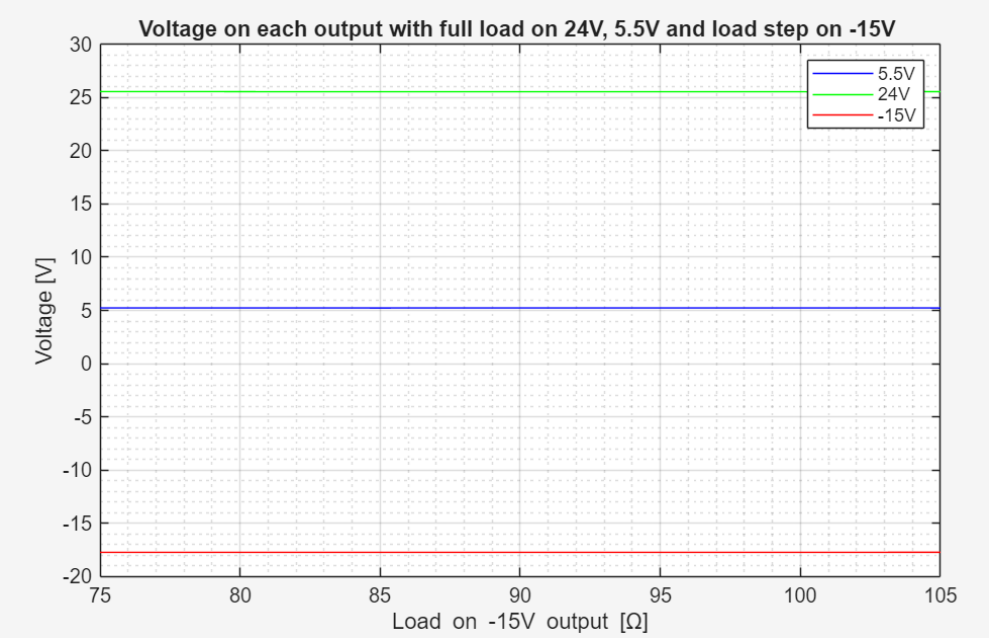


Figure 6: outputs voltages under full load on 5.5V & 24V with varying loads on -15V

Reference Behavior:

Unlike the +24 V and +5.5 V rails, the −15 V output is quasi-regulated and is not directly included in the main feedback loop, according to the user guide. Therefore, larger voltage variation under a load is expected.

Comparison and Discussion:

The measured results demonstrate a larger variation in the −15 V output voltage compared to the regulated rails. This behavior aligns with the expected quasi-regulated nature of the −15 V rail described in the datasheet. The comparison confirms that the observed deviation is an inherent characteristic of the converter topology rather than a malfunction or measurement error.

Power vs load resistance:

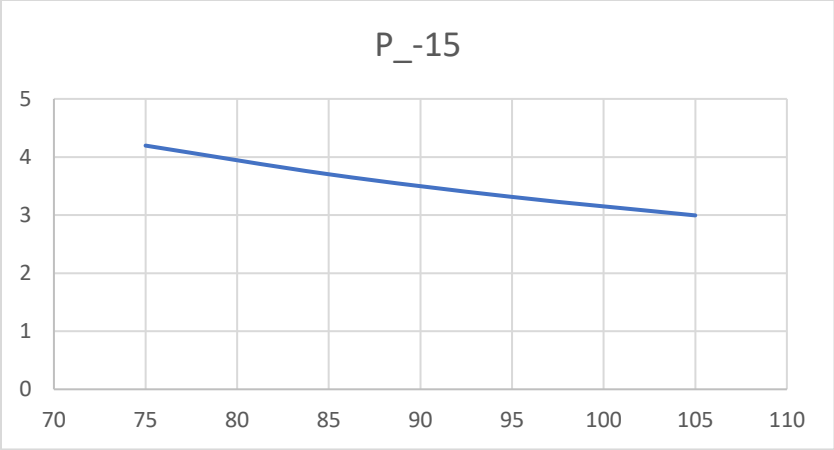


Figure 7: Power vs. resistance on -15V

The power graph acts as expected like we explained previously.

4.2.2 Post Test Analysis

After verifying that the device works as expected. We moved forward with our analysis of the circuit itself. One thing that stood out was the auxiliary wind on the primary side (pins 1&2 on the Transformer).

The measured voltage on the resistor R35 returned a constant 9.8 Volts regardless of load value on the outputs & the input voltage (if it was in the range that the ADP1071-1 could operate). This result is unexpected since there is a diode that theoretically should behave differently based on the changing current in the primary inductor as the transformer functions.

At this point we decided to further investigate this subcircuit. However, doing so could result in permanent damage to the device. So, we simulated it in LTspice and wanted to see if anything more could be extracted.

5. Simulation

Simulation Setup

As mentioned Previously, further testing is performed in LTspice. However, while building the circuit we discovered that there is a built-in model for the ADP1071-1 in the spice library. However, after countless tests we deduced that the model was faulty and didn't power up as expected. There for we subbed it for a pulse generator on the MOSFET gate with a duty cycle of 40%. This slightly affects the results, but it is still an accurate representation of the device.

Simulation Parameters & Circuit Design

As previously stated, the simulation was done in LTspice. The models for the MOSFET, diodes, capacitors & resistors were sourced from the bill of materials mentioned in the datasheet. The Transformer's windings are measured using the turn ratios in its datasheet. The schematic:

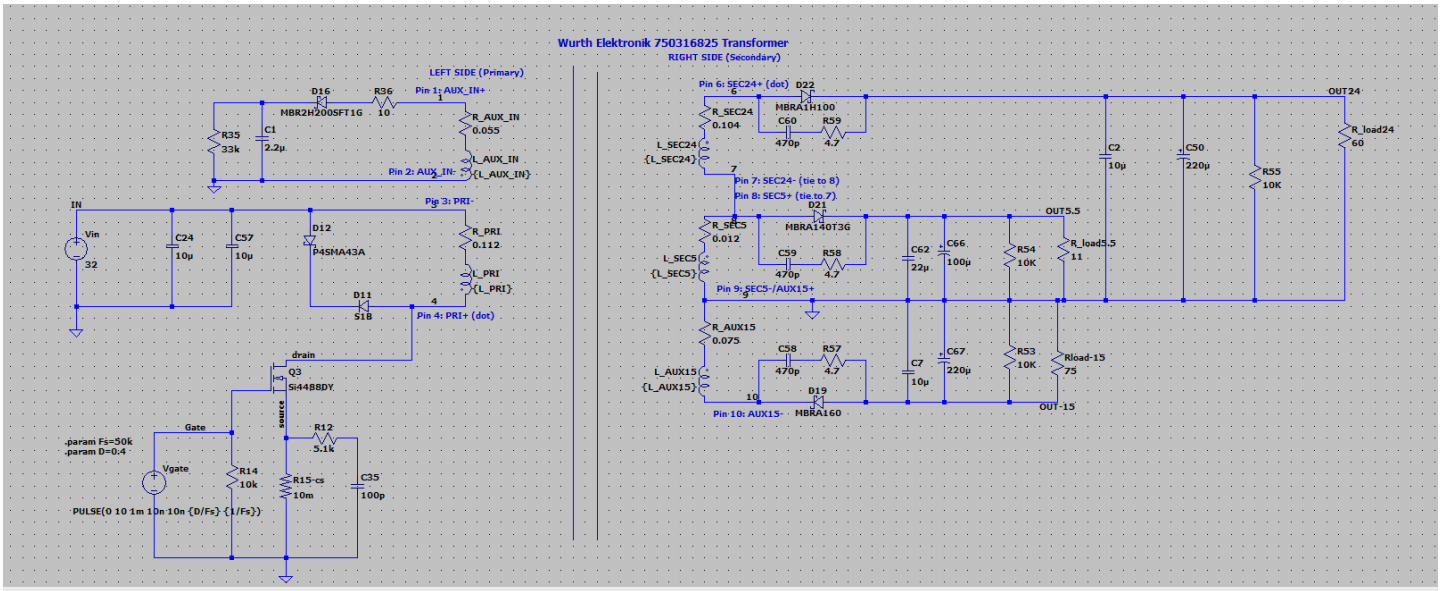


Figure 8: Simulation schematic

Model spice directives:

```
.model BZT52C11 D (Is=1e-14 Rs=10 N=1.05 Bv=11 Ibv=1m Cjo=50p)
.model S1B D (Is=1e-14 Rs=0.05 N=1.05 Bv=100 Ibv=100u Cjo=15p Tt=50n)
.model P4SMA43A D (Is=1e-14 Rs=0.01 N=1.05 Bv=43 Ibv=1m Cjo=500p)
.model MBR2H200SFT1G D (Is=1e-7 Rs=0.05 N=1.05 Bv=200 Ibv=100u Cjo=50p Vj=0.4)
.model MBRA160 D (Is=1e-6 Rs=0.03 N=1.05 Bv=60 Ibv=100u Cjo=30p Vj=0.4)
.model MBRA140T3G D (Is=2e-6 Rs=0.025 N=1.05 Bv=40 Ibv=100u Cjo=40p Vj=0.35)
.model MBRA1H100 D (Is=5e-7 Rs=0.04 N=1.05 Bv=100 Ibv=100u Cjo=25p Vj=0.45)
```

Transformer inductances:

```
MAGNETIC COUPLING:
* Transformer Inductances
.param L_PRI=97u
.param L_AUX_IN=7.6u
.param L_SEC24=50.2u
.param L_SEC5=2.48u
.param L_AUX15=18.8u

* Coupling coefficient
.param Kcouple=0.98
```

The coupling coefficient was chosen to be less than 1 to mirror the real world's non ideal isolation.

Simulation Results

Startup Transient

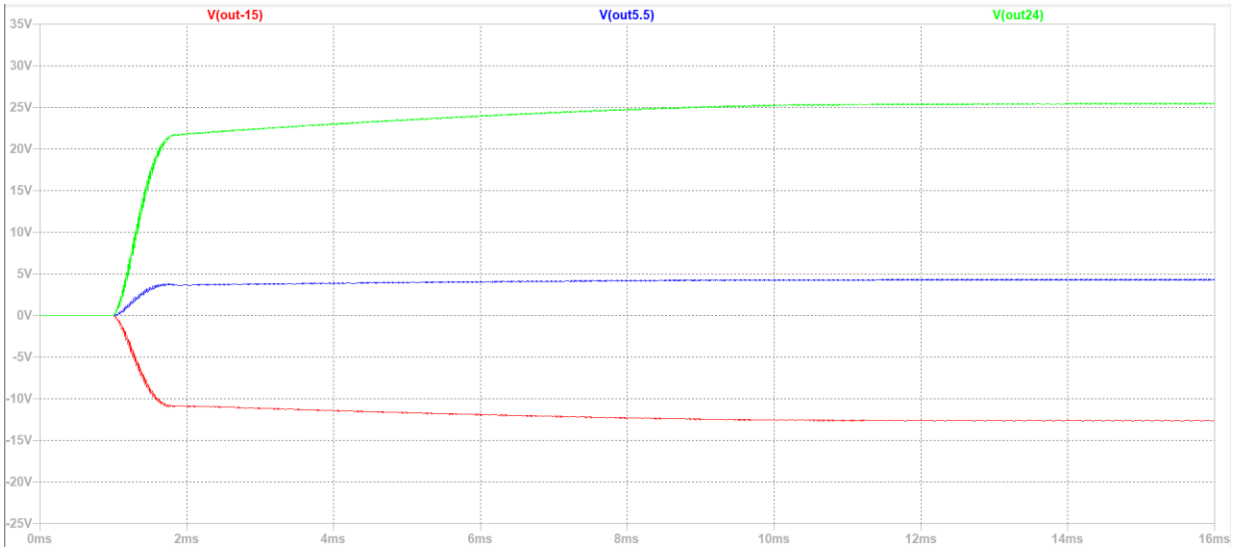


Figure 9: output voltages waveforms under full load startup

Since a pulse generator is used instead of the full ADP1071-1 model, the startup sequence in the simulation is quicker than the startup sequence in the datasheet. This result is expected. In addition, as speculation in previous sections, the output voltages after reaching a steady state are slightly different than the measured result yet are still in an acceptable range.

Median output voltages after reaching a steady state:

Expected	Simulation
24V	25.45V
5.5V	4.3 V
-15V	-13V

5.2.1 Steady State Waveforms

- Primary Inductor current

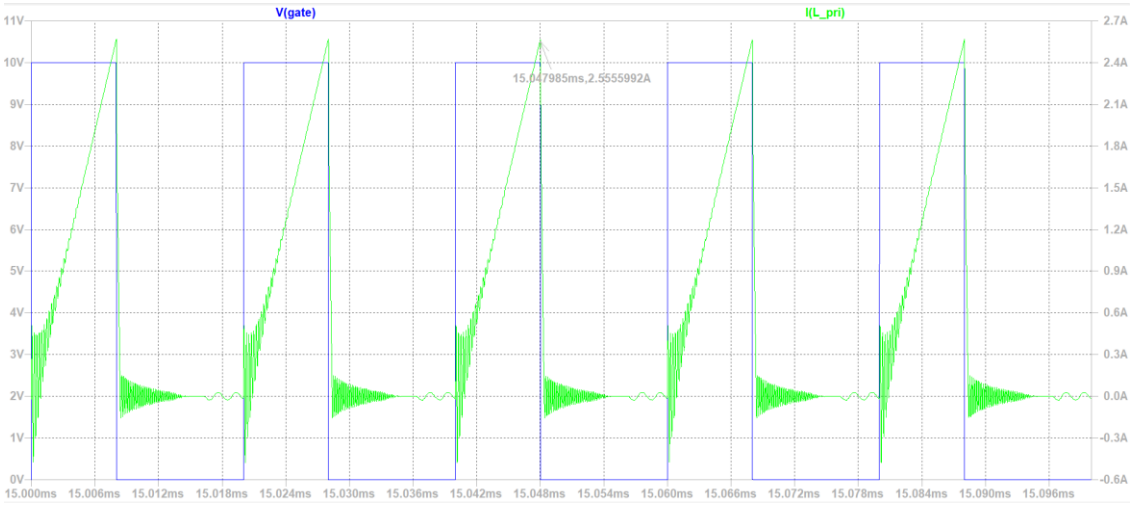


Figure 10: Primary inductor current &gate voltage

The waveform Demonstrates that the transformer operates in CCM as expected; the current ramping up while the MOSFET is on and oscillating around zero while off. In addition, peak current in the simulation is approximately 2.55A which is similar to the peak current in the datasheet (2.2A).

- Drain to source voltage on the MOSFET

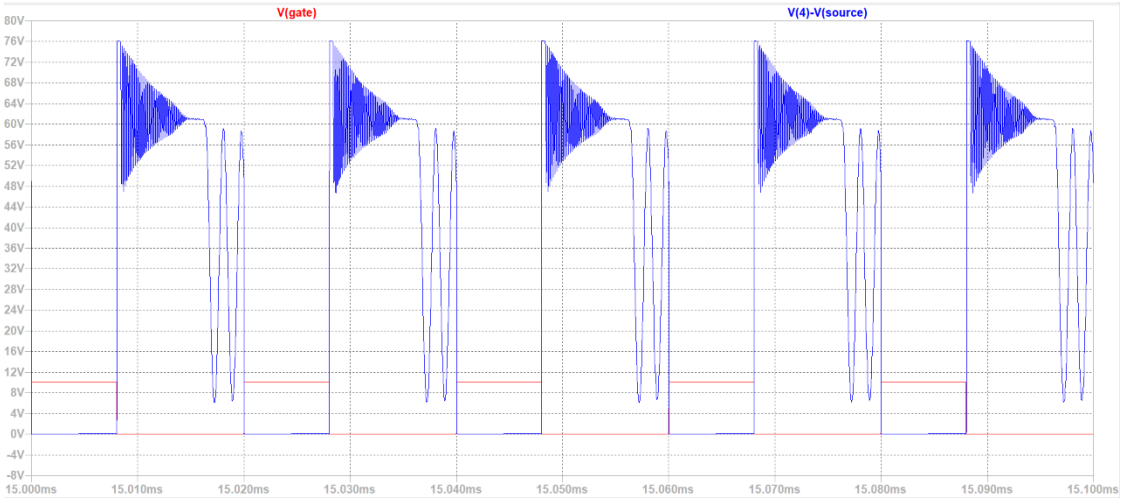


Figure 11: Vds voltage on the mosfet &gate voltage

The simulation results mirror the datasheet in terms of the waveform behavior. The peak voltage is approximately 76V, which is significantly lower than the expected 114V in the datasheet. This could be a result of using a pulse generator instead of the controller which lowered the stress on the MOSFET.

- Diode Stress on the 24V output

Figure 12: Diode stress on the 24V output &gate voltage

The stress on the diode is similar to the datasheet. However, the peak reverse stress in the simulation is larger than expected. This could be the result of the absence of the controller allowing the voltage to have a higher peak. Another reason could be the higher-than-expected output voltage.

- Diode Stress on the 5.5V output

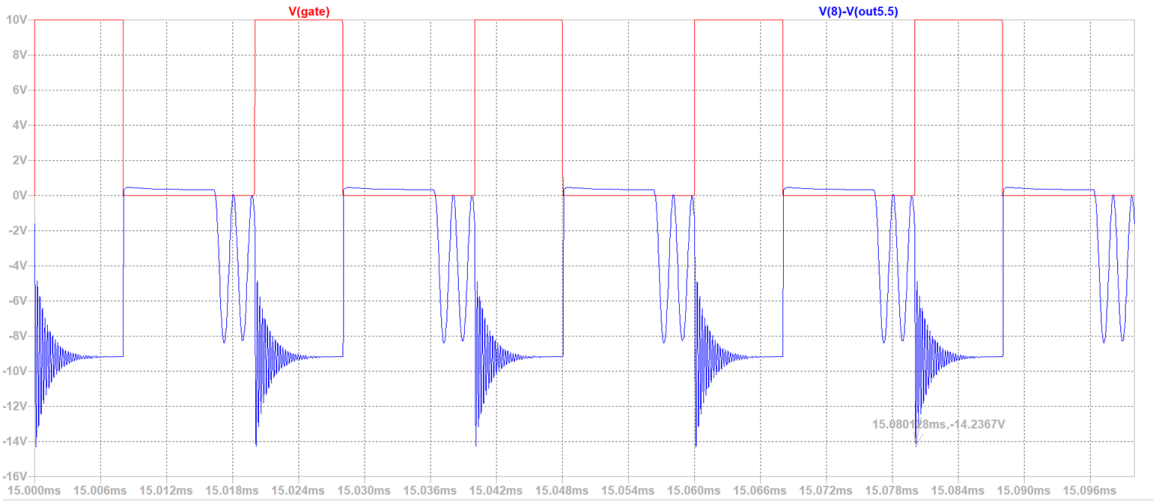


Figure 13: Diode stress on the 5.5V output &gate voltage

The voltage on the diode is behaving as expected. The reverse stress reaches a lower peak than expected. This could be a result of the higher-than-expected peak we received on the 24V output since the two outputs are partially regulated, or the result of having a lower-than-expected output voltage.

- Diode Stress on the -15V output

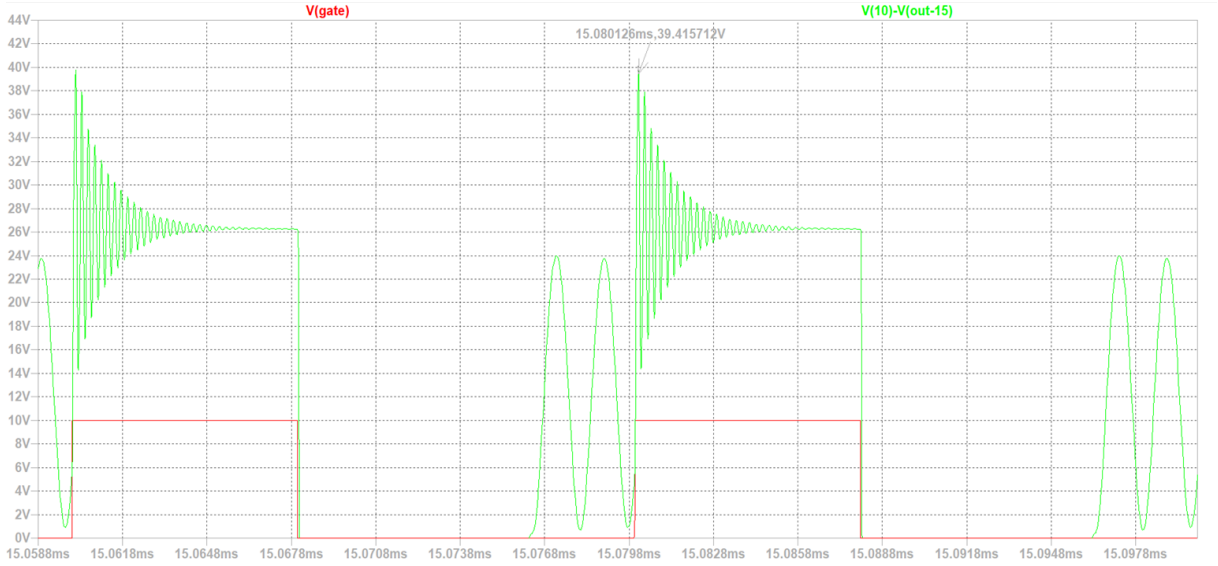


Figure 14: Diode stress on the -15V output &gate voltage

Similar to the other outputs, the diode voltage is like the waveform in the datasheet. The peak voltage is also lower than the expected value. The cause could be the lower than the expected output voltage.

peak voltage summary:

Expected	Simulation
-72.4V	-90.9V
-19.5V	-14.2V
48V	39.4V

5.2.2 Auxiliary Winding Analysis

- Aux. Inductor Current

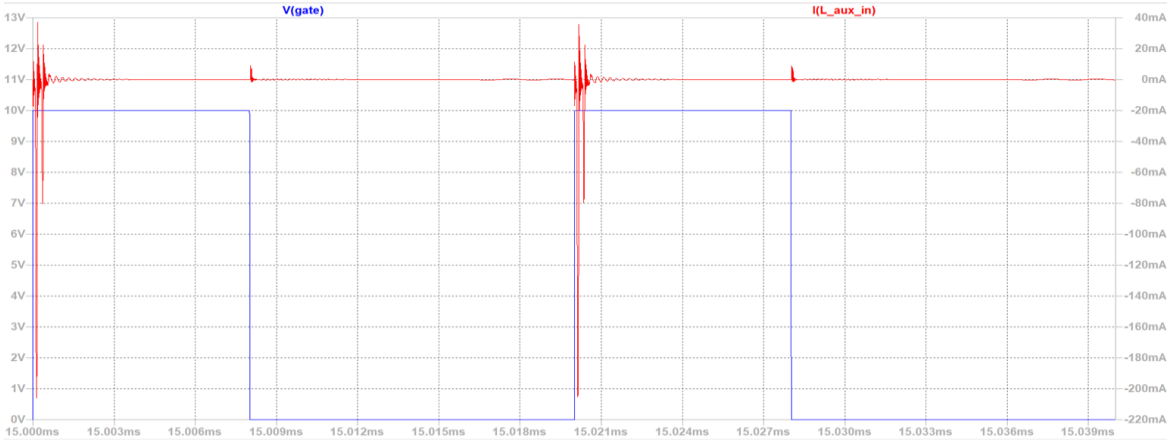


Figure 15: Auxiliary inductor current &gate voltage

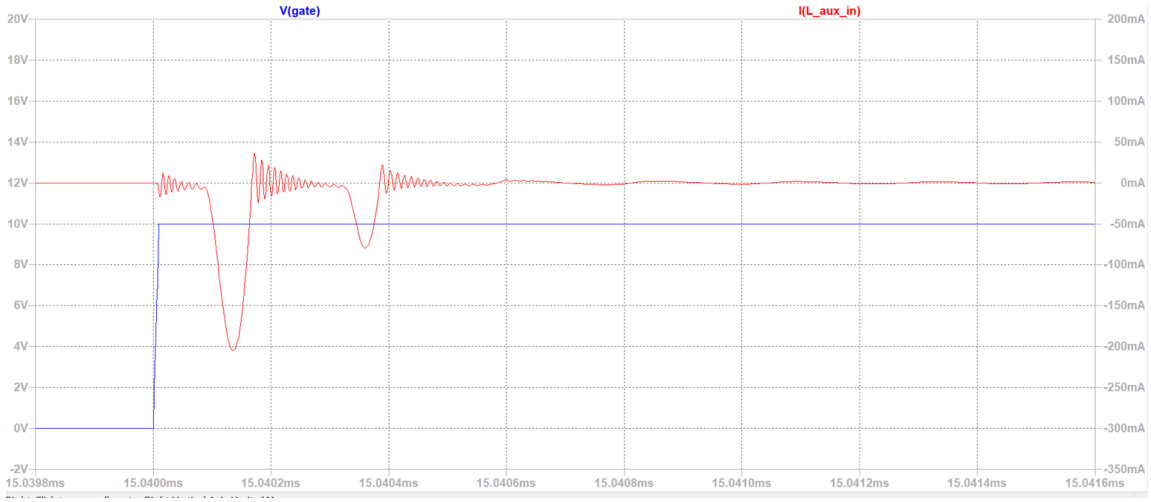


Figure 15.b: Auxiliary inductor current &gate voltage (zoomed in)

The current through the auxiliary inductor is negative. Therefore, the current is flowing out of pin 1 to R36 &D16 which is expected. The current is a pulse that occurs when the gate switches from low to high and then it oscillates decreasingly towards zero. This indicates that the auxiliary winding could be an additional means of protection for the circuit from an expected pulses that can be transferred from the secondary to the primary side.

- Auxiliary Wind Voltage

Figure 15: Auxiliary inductor voltage &gate voltage

The voltage between the pins 1 &2 spikes when the gate switches from low to high. Then it oscillates around 9V. When the gate switches from high to low, the voltage drops to around -8.5V and is oscillating with much smaller ripple.
Before switching from low to high, the voltage starts oscillating with higher ripples around zero.
These behaviors lead us to further believe that the auxiliary winding act as a protection for the circuit that further enhances isolation by absorbing spikes and signals that could transfer from the secondary side back to the primary. In addition, it could be a protective feature for the ADP1071-1 controller since it has components on both sides.

- Voltage Stress on D16 & C1

Figure 16: Voltage stress on the auxiliary diode & the voltage on the capacitor after the diode

The results are as expected. The Voltage on C1 is constant, though slightly higher than what is measured on the vesical device. Thus, the stress on the diode is the same as the voltage between pins 1&2 except for a vertical shift. This reinforces our analysis of the auxiliary wind's functionality.

5.2.3 Simulation without the auxiliary wind

Now that we have a basic idea of the auxiliary wind. We simulate the circuit without it and check for differences in behavior.

- Startup Transient

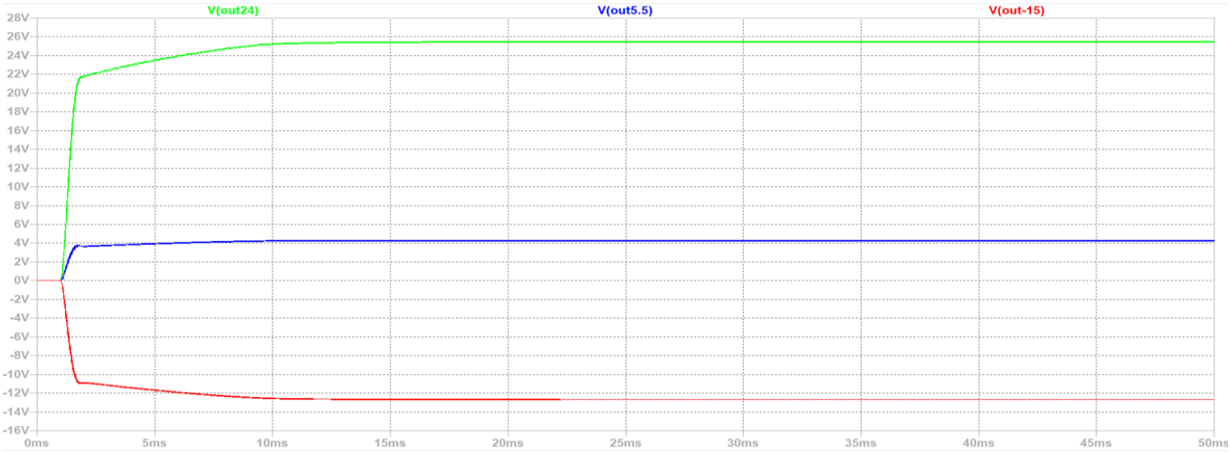


Figure 17: output voltages waveforms under full load startup-no auxiliary wind

- Primary Inductor Current

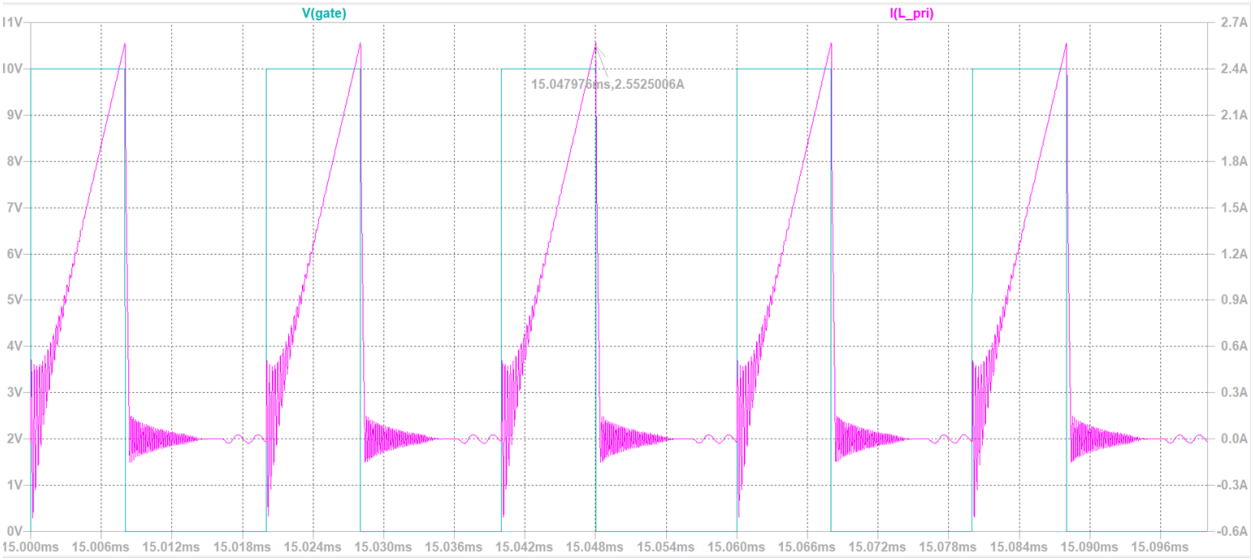


Figure 18: Primary inductor current &gate voltage-no auxiliary wind

- Voltage Stress on the MOSFET

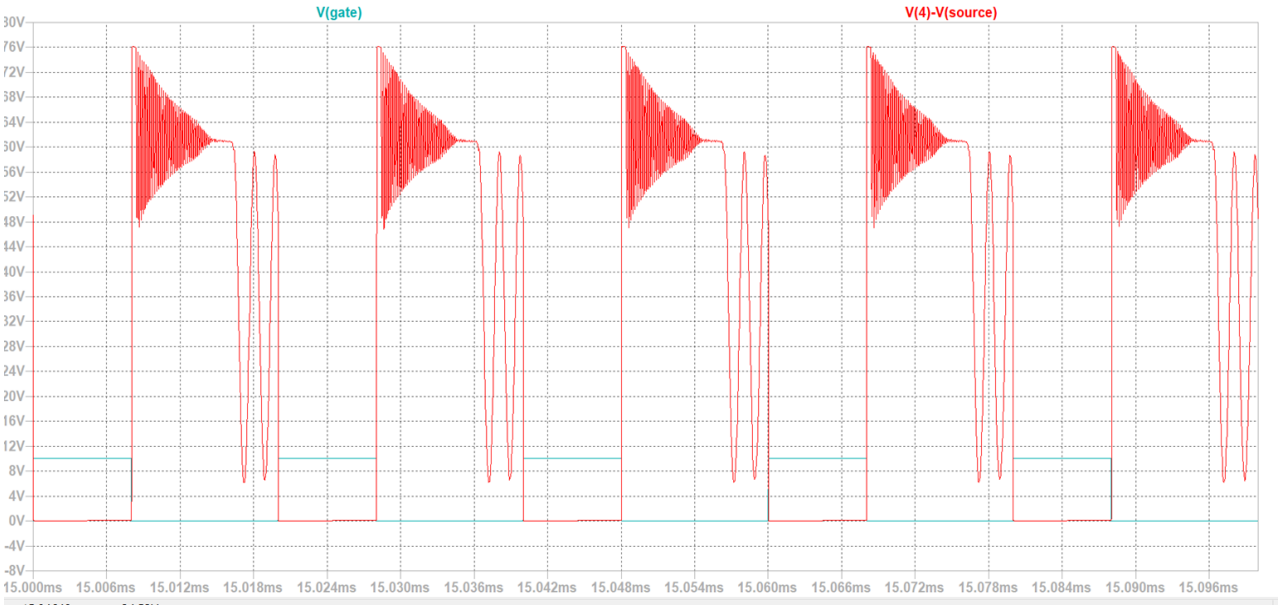


Figure 19: Vds voltage on the mosfet &gate voltage-no auxiliary wind

- Diode Stress on the outputs

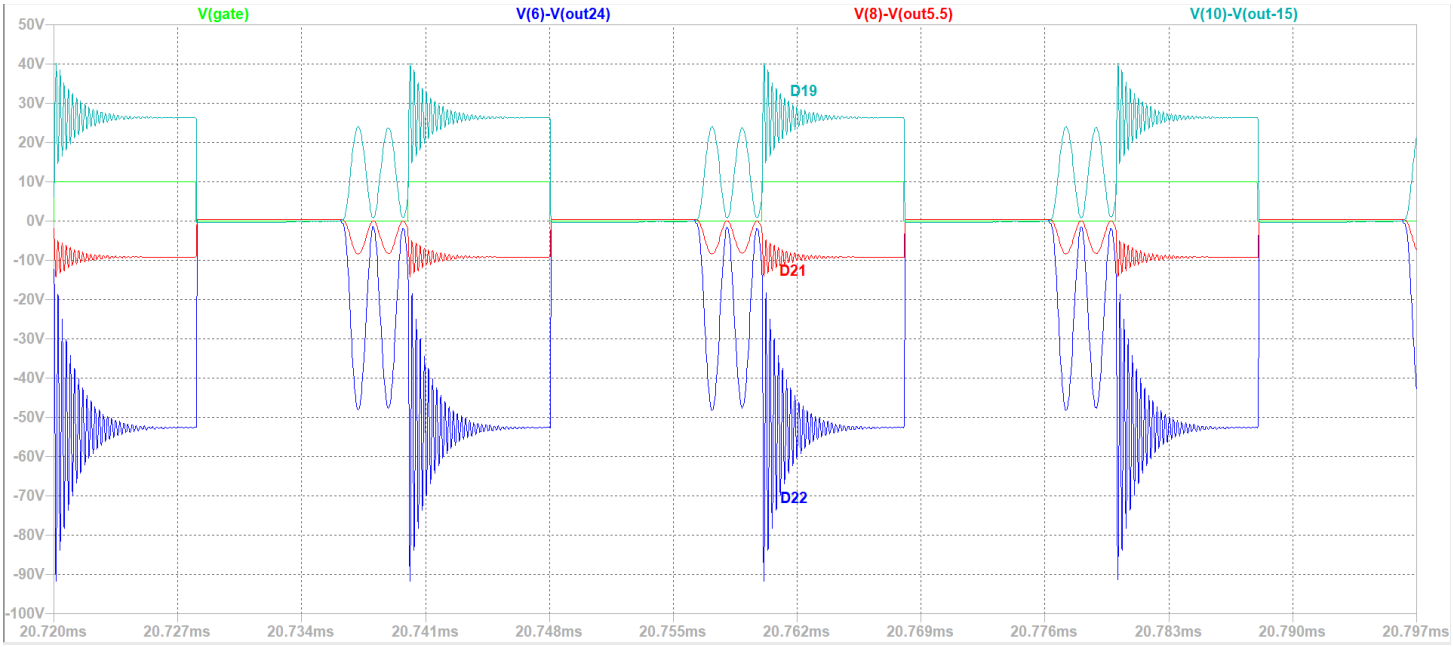


Figure 20: Diode stress on the -15V output &gate voltage-no auxiliary wind

From the waveforms we can conclude that our assumptions about the auxiliary wind are accurate. There aren't any noticeable differences in circuit behavior.

5. Discussion

This section analyzes the measured results in the context of the expected behavior described in the ADP1071-1EVALZ user guide and datasheet, with emphasis on regulation mechanisms, cross regulation, and operating limitations.

Regulation Performance and Datasheet Comparison

The experimental results demonstrate that the overall regulation behavior of the ADP1071-1EVALZ evaluation board closely matches the expected characteristics described in the datasheet and user guide.

Both the +24 V and +5.5 V rails exhibit relatively tight regulation across the tested load range. This behavior is consistent with the board's feedback architecture, in which these two rails are directly sensed and combined in the feedback network with a defined weightage ratio. As a result, load variations on these outputs produce only minor voltage deviations, in agreement with the reference performance curves presented in the documentation.

In contrast, the −15 V output demonstrates noticeably larger voltage variation under load. According to the datasheet, this rail is quasi-regulated and not directly included in the main feedback loop. Therefore, deviations observed in the measured −15 V output are expected and are inherent to the multi-output flyback topology rather than indicative of incorrect operation. The qualitative agreement between the measured trends and the reference behavior validates the design assumptions of the evaluation board.

Cross-Regulation Effects

Multi-output flyback converters inherently suffer from cross-regulation effects due to the shared transformer energy transfer among multiple secondary windings. In the ADP1071-1EVALZ design, cross regulation is mitigated by sensing both the +5.5 V and +24 V rails in the feedback loop, with a higher weight given to the +5.5 V rail.

The measured results confirm this design choice. Variations in load on one regulated output have a limited impact on the other regulated rail, while the quasi-regulated −15V rail is more sensitive to changes in load distribution. This behavior aligns with the cross-regulation discussion presented in the user guide and represents a typical trade-off in compact multi-output flyback designs.

Operating Margins and Practical Limitations

Although direct stress measurements were not performed in this project, the datasheet reports typical operating limits for the evaluation board under worst-case conditions. These include peak drain-to-source voltage on the primary MOSFET and peak primary current during full-load operation at maximum input voltage.

The measured regulation behavior indicates stable operation within the tested voltage and load ranges, suggesting that the system operates well within its designed margins.

No abnormal voltage instability, oscillation, or loss of regulation was observed during testing, which further supports the robustness of reference design.

6. Conclusion

This project presented a complete experimental evaluation of the ADP1071-1EVALZ multi-output isolated flyback converter evaluation board. The board architecture was studied in detail using the official user guide and schematics, and a series of electrical measurements were conducted to characterize its regulation behavior.

Measured output voltages were compared directly with expected behavior from the datasheet, demonstrating strong agreement for the regulated +24 V and +5.5 V rails and expected quasi-regulated behavior for the −15 V rail. The results confirm that the evaluation board performs as intended and provides stable operation across the specified input voltage and load ranges.

Furthermore, we managed to recreate the behavior of the device in LTspice without the ADP1071-1. This helped us further understand how the device works and how it could be used. The device is best suited for supplying integrated circuits that have multiple devices such as a laptop, where the 24V and -15V could be used to power up the fans, GPUs & other devices that require high voltages while the 5.5V could supply power to other devices that require smaller voltages.

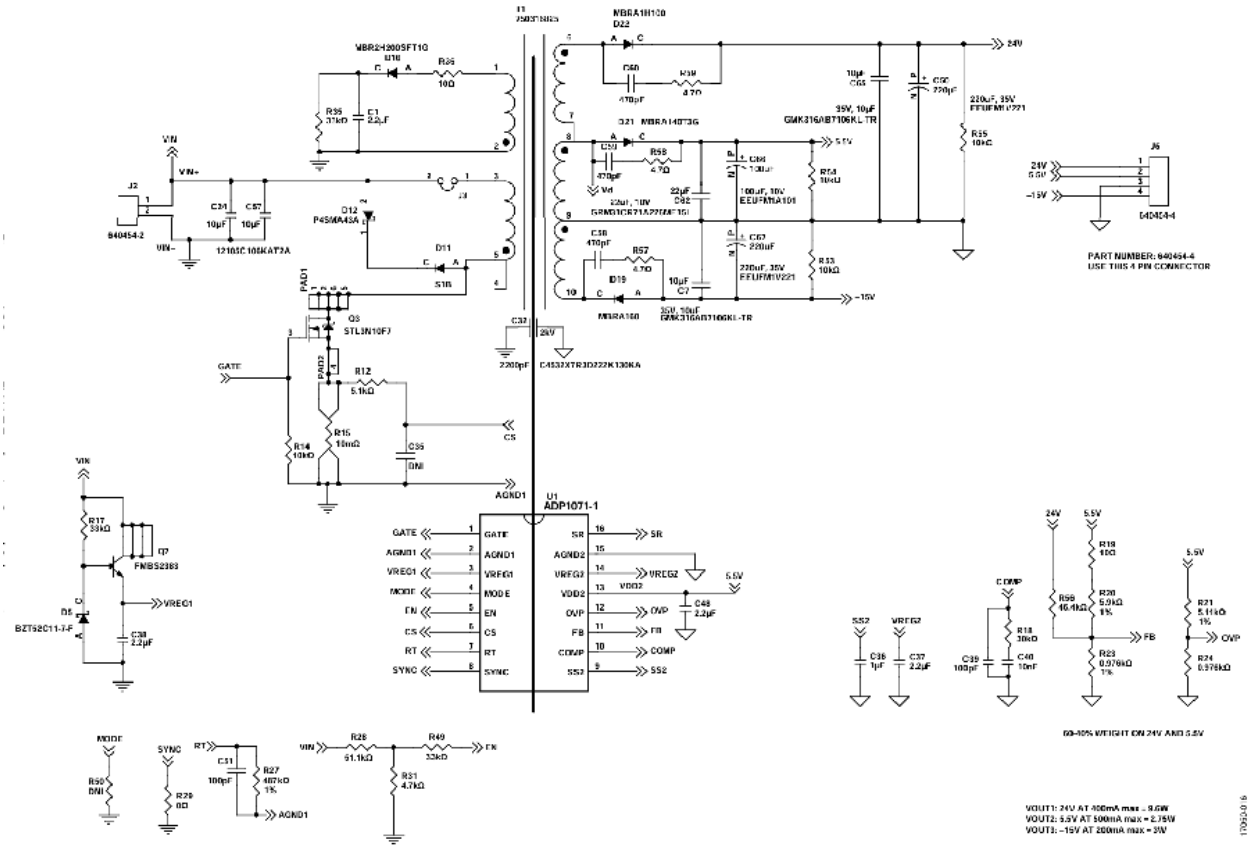
Overall, the project validates the ADP1071-1EVALZ as a reliable reference design for multi-output isolated power supplies and provides practical insight into the behavior and trade-offs of flyback converter architectures.

7. References

1. Analog Devices, ADP1071-1/ADP1071-2 Data Sheet
2. Analog Devices, ADP1071-1EVALZ User Guide (UG-1384)
3. Wurth Electronics, 750316825 Transformer Datasheet
4. Github including simulation files.

8. Appendices

Appendix A: Evaluation Board Schematic



Appendix B: Raw Test Data

Vout vs. Vin:

R_24	R_5.5	R_-15	Vout(24v)	Vout(5.5v)	Vout(-15v)	I_in	Vin
נתק	נתק	נתק	25.5	5.4	-15.6	0.5A	30
נתק	נתק	נתק	25.46	5.4	-15.57	0.5A	25
נתק	נתק	נתק	25.46	5.4	-15.57	0.5A	20
נתק	נתק	נתק	25.46	5.4	-15.57	0.5A	15
נתק	נתק	נתק	1.7	0.00006	undefined	0.5A	14
נתק	נתק	נתק	1.2	0.00005	-0.0006	0.5A	12

Cross regulation:

P_total	P_24	P_5.5	P_-15	R_24	R_5.5	R_-15	Vout(24v)	Vout(5.5v)	Vout(-15v)	I_in
16.92369	10.89708	1.830507	4.196101	60	15	75	25.57	5.24	-17.74	0.5A
15.38237	9.37692	1.823527	4.181921	70	15	75	26	5.23	-17.71	0.5A
14.23287	8.236861	1.823527	4.172481	80	15	75	25.67	5.23	-17.69	0.5A
13.33107	7.34449	1.823527	4.163052	90	15	75	25.71	5.23	-17.67	0.5A

P_total	P_24	P_5.5	P_-15	R_24	R_5.5	R_-15	Vout(24v)	Vout(5.5v)	Vout(-15v)	I_in	Vin
16.92369	10.89708	1.830507	4.196101	60	15	75	25.57	5.24	-17.74	0.5A	30
15.97211	10.71883	1.127844	4.125441	60	25	75	25.36	5.31	-17.59	0.46A	30
15.54492	10.63446	0.817786	4.092672	60	35	75	25.26	5.35	-17.52	0.45A	30
15.29883	10.584	0.64082	4.074005	60	45	75	25.2	5.37	-17.48	0.44A	30

P_total	P_24	P_5.5	P_-15	R_24	R_5.5	R_-15	Vout(24v)	Vout(5.5v)	Vout(-15v)	I_in	Vin
16.92369	10.89708	1.830507	4.196101	60	15	75	25.57	5.24	-17.74	0.5A	30
16.40601	10.88004	1.823527	3.702442	60	15	85	25.55	5.23	-17.74	0.5A	30
16.02326	10.88004	1.830507	3.312712	60	15	95	25.55	5.24	-17.74	0.5A	30
15.70592	10.88856	1.823527	2.993837	60	15	105	25.56	5.23	-17.73	0.5A	30