# Verifying Hardware Security Modules with Information-Preserving Refinement

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# Introduction

- Presenting [1]
- Hardware Security Modules (HSM)
- Theory
- Implementation
- Example: TOTP Token

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**Abstract**

Knox is a new framework that enables developers to build hardware security modules (HSMs) with high assurance through formal verification. The goal is to rule out all hardware bugs, software bugs, and timing side channels.

Knox's approach is to relate an implementation's wire-level behavior to a functional specification stated in terms of method calls and return values with a new definition called *information-preserving refinement (IPR)*. This definition captures the notion that the HSM implements its functional specification, and that it leaks no additional information through its wire-level behavior. The Knox framework provides support for writing specifications, importing HSM implementations written in Verilog and C code, and proving IPR using a combination of lightweight annotations and interactive proofs.

To evaluate the IPR definition and the Knox framework, we verified three simple HSMs, including an RFC 6238-compliant TOTP token. The TOTP token is written in 2950 lines of Verilog and 360 lines of C and assembly. Its behavior is captured in a succinct specification: aside from the definition of the TOTP algorithm, the spec is only 10 lines of code. In all three case studies, verification covers entire hardware and software stacks and rules out hardware/software bugs and timing side channels.

**1 Introduction**

A powerful approach for building secure computer systems is to factor out the core security functionality onto a separate device. For example, on the server side, certificate authorities use hardware security modules (HSMs) to store their signing key and sign certificates [10, 58]; credit card networks use HSMs for pin translation, secure re-encryption of payment requests during routing; cloud providers use HSMs to safeguard PIN-protected backup keys [9, 43, 47]; and some tax authorities require the use of an HSM to timestamp invoices. On the client side, the iPhone uses its secure enclave processor to enforce PIN guessing limits for unlocking the phone [15]; and users often rely on USB security keys to protect their authentication private key in the face of a compromised computer [65]. For simplicity, this paper refers to all of these types of devices as HSMs. These devices are in widespread use; e.g., there are hundreds of millions of deployed secure enclaves and security keys.

This approach defends against a broad class of attacks where an adversary gains access to any host computer that the HSM might be connected to, regardless of the specific attack vector (exploiting a buffer overflow, missing access control checks, or even gaining access to the administrator's SSH key). As long as the security of the overall system is rooted in the device, an adversary that controls the host cannot undermine the security of the overall system. Of course, the device must be correctly implemented to make sure that the adversary cannot compromise it, which in practice means that the device must provide simple, well-defined functionality.

Although HSMs are relatively simple, any vulnerability in their hardware or software can undermine their security. HSMs have suffered from bugs throughout the hardware/software stack, such as logic bugs, memory corruption, hardware bugs, and timing side channels [1–8, 21, 31, 45, 51, 68]. This paper presents an approach for ruling out such bugs through formal verification, with a particular focus on eliminating leakage through timing side channels.

Our approach is to relate the behavior of the HSM implementation at the wire level interface — the ground truth of what the host machine controls and observes at the digital level, which captures timing channels at a cycle-accurate level — to a functional specification of the methods that the HSM exposes. Figure 1 shows the implementation of a simplified PIN-protected backup HSM, which we use as a running example through the paper. The host connects to this HSM via two input wires and two output wires, which the host can read/write at every cycle. Figure 2 shows the functional specification for this HSM. It exposes two operations, `store` and `retrieve`. The specification does not have an operation for reading back the PIN, and it enforces a guess limit on PINs.

We relate a physical implementation to a functional specification with a new definition called *information-preserving refinement (IPR)*, inspired by definitions of zero-knowledge proofs in cryptography [40, 41]. IPR captures the notion that the implementation implements the spec, and that its wire-level I/O behavior leaks no additional information. In IPR, a *driver* describes the I/O protocol that a host computer can follow to get correct results from the HSM, describing how each spec-level operation translates to wire-level I/O with the HSM. The driver is a part of the specification (and is trusted). Its dual, an *emulator*, is a proof artifact that describes how wire-level behavior can be explained in terms of spec-level operations. The existence of an emulator shows that no matter what wire-level inputs are given to the device (including inputs that violate the I/O protocol), its outputs reveal no more information than the specification.

Applied to HSMs, IPR can capture subtle security bugs: for example, Figure 3 shows code that is correct and even crash safe but has a subtle bug involving persistence and



# Hardware Security Modules (HSM)

- Dedicated hardware for core security functionality
  - Certificate signing
  - Password hashing
  - Token generation
- May include general purpose core
- Communicates with host over wire interface



From [1]

# Thread Model

- Remote compromise of host
- Any *digital* use of wire interface
- Ensure no extra information leaks
  - Bug in implementation
  - Timing Attacks →
- Does not consider physical access
  - Overvoltage, tampering
  - Secure as the specification

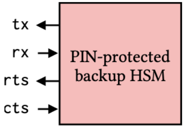
```
// return error if PIN guess limit exceeded
// ...

// check PIN guess and update guess_count accordingly
if (!constant_time_cmp(&entry->pin, guess)) {
    entry->bad_guesses++;
    uart_write(ERR_BAD_PIN);
    return;
}
entry->bad_guesses = 0;

// output secret
// ...
```

From [1]

# Information Preserving Refinement (IPR)

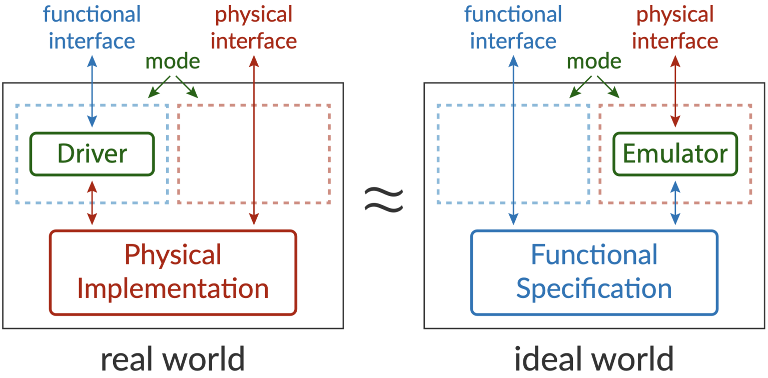
- Start with functional specification
- Device should implement this spec
- Wire-level interactions $\iff$ spec. level operations
- Based on dual views
  - Real world (uncompromised host)
  - Ideal world (compromised host

```
var bad_guesses = 0, secret = 0, pin = 0

def store(new_secret, new_pin):
  secret = new_secret
  pin = new_pin
  bad_guesses = 0

def retrieve(guess):
  if bad_guesses >= 10:
    return 'No more guesses'
  if guess == pin:
    bad_guesses = 0
    return secret
  bad_guesses = bad_guesses + 1
  return 'Incorrect PIN'
```




From [1]

# Information Preserving Refinement (IPR)




From [1]

# Proving IPR

- Developer provides $R$, relates
  - State of spec state machine
  - State of implementation
- Developer also provides
  - Driver
  - Emulator

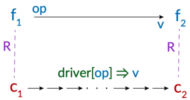



Figure 7: Functional equivalence: for all implementation states $c_1$ and spec states $f_1$ that are related by $R$, and for all spec-level operations $op$:
(1) the spec-level output $v$ matches the driver output
(2) the final states $c_2$ and $f_2$ are related by $R$

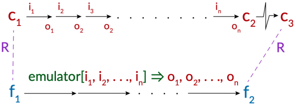



Figure 8: Physical equivalence: for all spec states $f_1$ and implementation states $c_1$ that are related by $R$, and for all wire-level inputs $i_1 \dots i_n$:
(1) the circuit outputs $o_1 \dots o_n$ match the emulator outputs
(2) the final states $f_2$ and $c_3$ ($c_2$ after a reset) are related by $R$

From [1]

# Implementation: Knox

- Knox, monolithic verification
- Targets Rosette [3]
  - Solver-aided programming language
- Generate SMT Constraints
  - Solve with Z3 [2]

Racket Z3

The Rosette Language

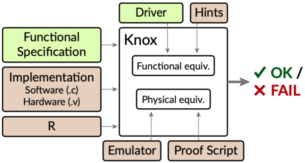



Figure 11: An overview of the Knox workflow. Trusted inputs are shown in green.

# Implementation pt. 2

TODO

## Case Studies

TODO

# Case Study: PIN-protected backup HSM

TODO

# Case Study: Password Hashing HSM

TODO

# Case Study: TOTP Token

TODO

# Discussion

- Emulator Efficiency
- Randomness
- Allowed leakage
- Monolithic Verification

# Conclusion

TODO

# References I


[1] Anish Athalye, M Frans Kaashoek, and Nickolai Zeldovich. "Verifying hardware security modules with {Information-Preserving} refinement". In: *16th USENIX Symposium on Operating Systems Design and Implementation (OSDI 22)*. 2022, pp. 503–519.

[2] Leonardo De Moura and Nikolaj Bjørner. "Z3: An efficient SMT solver". In: *International conference on Tools and Algorithms for the Construction and Analysis of Systems*. Springer. 2008, pp. 337–340.

[3] Emina Torlak and Rastislav Bodik. "Growing solver-aided languages with rosette". In: *Proceedings of the 2013 ACM international symposium on New ideas, new paradigms, and reflections on programming & software*. 2013, pp. 135–152.