Important Equations for Pipelining:

Speed Up:

$$S_n = \frac{Execution\ time_{old}}{Execution\ time_{new}} = \frac{nt_n}{(k+n-1)t_p}$$

Efficiency:

$$E = \frac{n}{(k+n-1)} = \frac{S_n}{(t_n / t_p)}$$

Where n is the number of tasks, t_n is the time to complete each task on a non-pipeline unit, k is the number of stages for each task, and t_p is the time period to complete a k-stage pipeline.

Problem 1:

Consider a machine where each task passes by 4 stages in order to be executed, each of length 20 ns, If 100 tasks to be executed:

a) On a non-pipelined machine, what is the execution time for the tasks on this machine?
b) On a 4-stage pipeline machine, what is the execution time for the tasks on this machine?
c) What is the speed up gained from pipelining?

Solution:

d) Total execution time in a non-pipelined machine = 20x4x100 = 8000 ns
e) Total execution time in a pipelined machine = (k + n-1) x t_p = (4+99) x20
f) = 2060 ns
g) Speedup = 8000/2060 = 3.88

Problem 2:

Consider a machine where each instruction passes by 5 stages, the 5 stages needs 10, 8, 10, 10, 7 ns respectively. If a pipeline is applied to the machine, it adds a latch of 1 ns between each stage and the other. If 50 tasks to be executed:

a) On a non-pipelined machine, what is the execution time?
b) On a 5-stage pipeline machine with a latch, what is the execution time?
c) What is the speed up gained from pipelining?

Solution:

a) Total execution time in a non-pipelined machine = (10+8+10+10+7)x50 = 2250 ns
b) Total execution time in a pipelined machine = $(k + n-1) \times t_p = (5+49) \times 11$
$= 594$ ns
c) Speedup = 2250/594 = 3.78

Problem 3:

Consider a non pipelined machine with 6 stages of lengths 50 ns, 50 ns, 60 ns, 60 ns, 50 ns, and 50 ns.

a) What is the execution time for an instruction on this machine?
b) How much time does it take to execute 100 instructions?

Suppose we introduce pipelining on this machine. Assume that when introducing pipelining, the clock adds 5ns latch to each execution stage.

c) What is the execution time for an instruction on this machine?
d) How much time does it take to execute 100 instructions?
e) What is the speedup obtained from pipelining for 100 instructions?

Solution:

a) Execution time per instruction = 50+50+60+60+50+50= 320 ns
b) Time to execute 100 instructions = 100*320 = 32000 ns

Remember that in the pipelined implementation, the length of the pipe stages must all be the same, i.e., the speed of the slowest stage plus overhead. With 5ns latch it comes to:

The length of pipelined stage = MAX(lengths of non-pipelined stages) + latch
$= 60 + 5 = 65$ ns

c) Execution time per instruction= 65 ns
d) Time to execute 100 instructions = (6+99) * 65 = 6825 ns
e) Speedup for 100 instructions = 32000 / 6825 = 4.69

Problem 4:

Consider the following snippet of code:

```
FOR i = 1 TO 100 DO
{
        A[i] = (B[i]xC[i]) + D[i]
}
```

Assume that each operation, multiplication and addition, requires 10 ns to complete. Consider a pipelined unit that could break this computation into two stages, the first stage performs the multiplication and the second stage performs the addition.

a) What is the total execution time for the code before pipeline?
b) What is the total execution time for the code after pipeline if no latch is added?
c) What is the total execution time for the code after pipeline if a latch of 2ns is added between stages?
d) Calculate the speedup gained from pipeline with latch.

Solution

a) Total execution time for the code before pipeline = (10+10) x 100 = 2000 ns
b) Total execution time for the code after pipeline without latch = (2+99)x10 = 1010 ns
c) Total execution time for the code after pipeline with latch = (2+99)x12 = 1212 ns
d) Speedup = 2000/1212 = 1.65

Problem 5:

Assume that the individual stages of on a machine takes the following execution time:

IF	ID	EX	MEM	WB
300ps	400ps	350ps	500ps	100ps

Assume that when pipelining, each pipeline stage costs 20ps extra between pipeline stages.

a) What is the clock cycle time in a pipelined and non-pipelined processor?
b) If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time?

Solution

a) Clock cycle time in a non-pipelined = 300 + 400 + 350 + 500 + 100 = 1650 ps
Clock cycle time in a pipelined = 500 + 20 = 520 ps
b) Splitting the longest stage is the only way to reduce the cycle time. After splitting it, the new cycle time is based on the new longest stage.
Old longest stage is MEM.
New Clock cycle time = 420ps

Problem 6:

Consider a machine where each instruction passes by 4 stages, fetch (IF), decode(ID), execute(EX), and write back (WB).

a) Fill table 1 to show 3 instructions execution on a non-pipelined machine.
b) Fill table 2 to show 3 instructions execution on a pipelined machine.

Table 1

Inst1															
Instr2															
Instr3															

Table 2

Inst1															
Instr2															
Instr3															

Solution:

Table 1

Inst1	IF	ID	EX	WB											
Instr2					IF	ID	EX	WB							
Instr3									IF	ID	EX	WB			

Table 2

Inst1	IF	ID	EX	WB											
Instr2		IF	ID	EX	WB										
Instr3			IF	ID	EX	WB									