Problem 1:

Represent the following conditional control statement by *two* register transfer statements with control functions:

If (X = 1) then (R1 ← R3) else if (Y=0 and Z = 1) then (R1 ← R4+R2)

Solution:

$\underline{X}$: R1 ← R3

$\overline{X}\,\underline{\overline{Y}\,Z}$: R1 ← R4+R2

Problem 2:

A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

a. How many selection inputs are there in each multiplexer?
b. What size of multiplexers is needed?
c. How many multiplexers are the in the bus?

Solution:

a. 4 selection lines to select one of 16 registers.
b. 16 × 1 multiplexers.
c. 32 multiplexers, one for each bit of the registers.

Problem 3:

Explain the memory operation in each of the following transfer statements.

a. M[AR]← R2
b. R3 ← M[AR]

Solution:

a. Write content of register R2 into the memory word specified by the address in AR.
b. Read memory word specified by the address in AR into register R3.

Problem 4:

If the values in AR = 500, DR = 80, R2 = 50 and R3 = 70, the content of Memory address 500 is 100 and the content of Memory address 501 is 101. Show the content of the 4 registers and the content of the memory addresses 500 and 501 after the following RTL statements.

M[AR]← DR
R2 ← M[AR]
DR ← R3
AR ← AR+1
M[AR] ← R3

Solution:

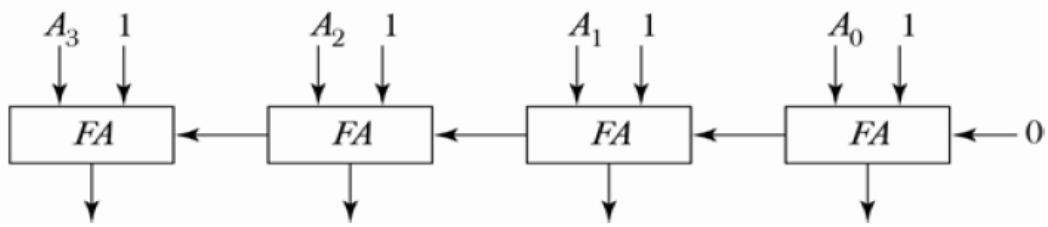
AR = 501, DR = 70, R2=80 , R3=70 , M[500]=80, M[501] =70

Problem 5:

Design a 4-bit combinational circuit decrementer using 4 full-adder circuits.

Solution:

A-1 = A + 2's complement of 1 = A + 1111

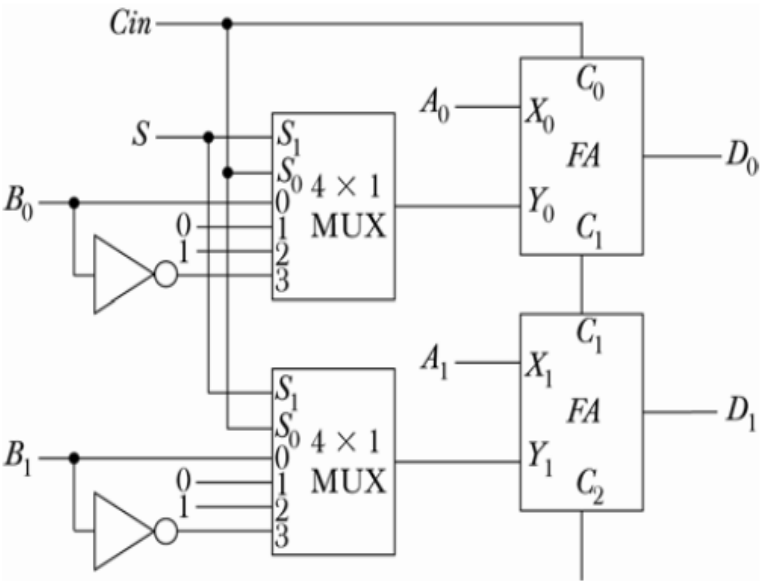


Problem 6:

Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	C_{in} = 0	C_{in} = 1
0	D= A+B (add)	D= A+1 (increment)
1	D= A-1 (decrement)	D= A+B′+1 (subtract)

Solution:



S	C_{in}	X	Y	
0	0	A	B	(A+B)
0	1	A	0	(A+1)
1	0	A	1	(A-1)
1	1	A	B′	(A-B)

Problem 7:

Register A holds the 8-bit binary value 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to:

a. 01101101
b. 11111101

Solution:

a.
$$\begin{array}{l} A=11011001 \\ B=10110100 \oplus \\ \hline A \leftarrow A \oplus B \ 01101101 \end{array}$$

Selective complement

b.
$$\begin{array}{l} A=11011001 \\ B=11111101 \ (OR) \\ \hline A \leftarrow A \vee B \ 11111101 \end{array}$$

Selective set

Problem 8:

Starting from an initial value of R = 11010111, determine the sequence of binary values of R after a logical shift left, followed by a circular shift-right, followed by a logical shift right and a circular shift right.

Solution:

R = 11010111
Logical shift left: 10101110
Circular shift-right: 01010111
Logical shift right: 00101011
Circular shift right: 10010101

Problem 9:

An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.

Solution:

R = 10011100
Arithmetic shift right: 11001110
Arithmetic shift left: 00111000 overflow because a negative number changed to positive.