Problem 1:

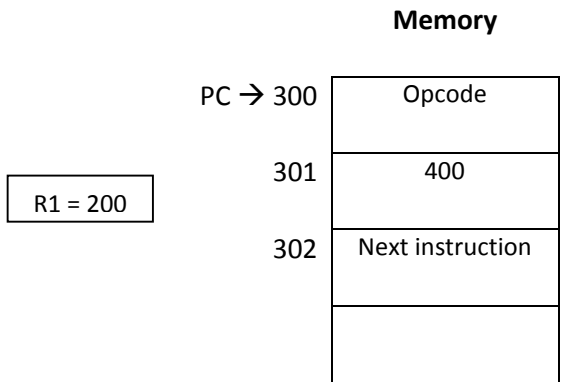
An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate effective address if the addressing mode of the instruction is

a. Direct
b. Immediate
c. PC-Relative
d. Register indirect
e. Indexed with R1 as the index register.

Solution:

Effective address

a. Direct = 400
b. Immediate = 301
c. PC-Relative = 302 + 400 = 702
d. Register Indirect = 200
e. Indexed = 200 + 400 = 600



Problem 2:

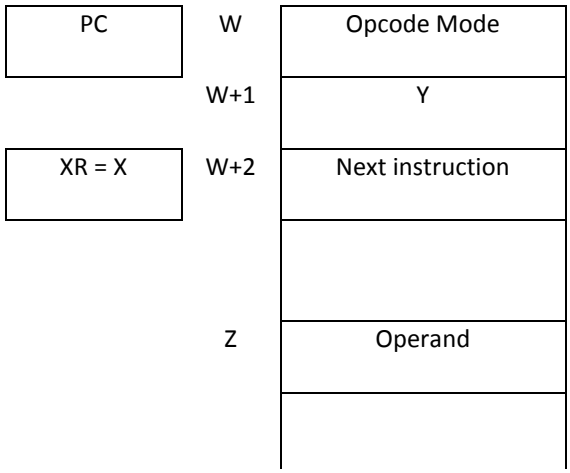
A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is:

a. Direct
b. Immediate
c. PC-Relative
d. Indexed

Solution:

Z =Effective address

a. Direct: Z=Y
b. Immediate: Z=W+1
c. PC-Relative: Z=Y+(W+2)
d. Indexed: Z=Y+X



Problem 3:

A PC-Relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750 (assume one word per instruction). The branch is made to an address equivalent to decimal 500. What should be the value of the relative address field of the instruction (in decimal)?

Solution:

Relative address = 500 – 751 = -251

Problem 4:

Consider a hypothetical 24-bit microprocessor having 24-bit instructions composed of two fields: The first byte contains the Opcode and the remainder the operand address. What is the maximum directly addressable memory capacity (in bytes)?

Solution :

Opcode one byte (8 bits) and address 2 Bytes (16 bits).

Therefore, the maximum directly addressable memory capacity (in bytes) → 2^{16} = 64 Kb

Problem 5:

A computer has a 32-bit instructions and 12-bit addresses. If the instructions on this computer are either of type one-address instructions or two-address. If there are 250 two-address instructions, how many one-address instructions can be formulated?

Solution:

8	12	12	= 32 bit
Opcode	Address 1	Address 2	Two address instructions

2^8 = 256 combinations.

256 – 250 = 6 combinations can be used for one address

For one-address instructions, one of the address fields can be used as an extension to the Opcode.

Opcode	Address	One address instructions
6×2^{12}		

Maximum number of one address instruction = 6 x 2^{12} = 24,576 instructions

Problem 6:

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a) What is the maximum directly addressable capacity (in bytes)?

b) Discuss the impact on the system speed if the microprocessor bus has:

   1. A 32 bit local address bus and a 16-bit local data bus.
   2. A 16 bit local address bus and a 16-bit local data bus.

c) How many bits are needed for the PC and the IR registers?

Solution:

a) 2^{24} = 16Mbytes

b) 1) If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, since the data bus is only 16-bits, it will require 2 cycles to fetch a 32-bit instruction or operand.

2) The 16 bits of the address is placed on the address bus can't access the whole memory. Thus a more complex memory interface control is needed to latch the first part of the address and then the second part (since the microprocessor will end in two steps). For a 32-bit address, one may assume the first half will decode to access a "row" in memory, while the second half is sent later to access a "column" in memory. In addition to the two-step address operation, the microprocessor will need 2 cycles to fetch the 32 bit instruction/operand.

c) The program counter must be at least 24 bits. Typically, a 32-bit microprocessor will have a 32-bit external address bus and a 32-bit program counter, unless on-chip segment registers are used that may work with a smaller program counter. If the instruction register is to contain the whole instruction, it will have to be 32-bit long; if it will contain the whole instruction, it will have to be 32-bit long; if it will contain only the opcode (called the opcode register) then it will have to be 8 bits long.