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CA:LAB 8

LAB SUBMISSION

TASK 1:

The screenshot shows a MIPS simulator interface. On the left, the 'Registers' window displays the following data:

Name	Width	Data
AC	16	0004
AR	12	001
DR	16	0006
E	1	1
I	1	0
IR	16	E001
PC	12	00D
S	1	1

The central assembly window, titled '*subtracta X', shows the following code:

```
1 START:
2 INP
3 STA NUM
4
5 INP
6 CMA
7 INC
8 ADD NUM
9 STA NUM
10
11 INP
12 CMA
13 INC
14 ADD NUM
15
16 OUT
17 HLT
18
19 NUM: .data 1 0
20
```

On the right, the 'MAIN' memory window shows a table of addresses and data:

Addr	Data
000	F800
001	600D
002	F800
003	E200
004	E020
005	200D
006	600D
007	F800
008	E200
009	E020
00A	200D
00B	F400
00C	E001
00D	0006
00E	0000
00F	0000
010	0000

The bottom status bar shows the execution output:

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 10
Enter Inputs, the first of which must be an Integer: 4
Enter Inputs, the first of which must be an Integer: 2
Output: 4
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

TASK 2:

The screenshot shows a MIPS simulator interface. On the left, the 'Registers' window displays the following data:

Name	Width	Data
AC	16	0002
AR	12	001
DR	16	0004
E	1	1
I	1	0
IR	16	E001
PC	12	006
S	1	1

The central assembly window, titled 'subtracta X', shows the following code:

```
1 START:
2 ADD NUM2
3 CMA
4 INC
5 ADD NUM1
6
7 OUT
8 HLT
9
10 NUM1: .data 1 4
11 NUM2: .data 1 2
12 RESULT: .data 1 0
```

On the right, the 'MAIN' memory window shows a table of addresses and data:

Addr	Data
000	2007
001	E200
002	E020
003	2006
004	F400
005	E001
006	0004
007	0002
008	0000
009	0000
00A	0000
00B	0000
00C	0000
00D	0000
00E	0000
00F	0000
010	0000

The bottom status bar shows the execution output:

```
EXECUTING...
Output: 2
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

TASK 3:

DataHex

Registers

Name	Width	Data
AC	16	0004
AR	12	001
DR	16	0006
E	1	1
I	1	0
IR	16	E001
PC	12	007
S	1	1

subtracta X

```
1 START:
2 ADD NUM2
3 CMA
4 INC
5 ADD NUM1
6 STA RESULT
7 OUT
8 HLT
9
10 NUM1: .data 1 6
11 NUM2: .data 1 2
12 RESULT: .data 1 0
13
```

AddrHexDataHex

MAIN

Addr	Data
000	2008
001	E200
002	E020
003	2007
004	6009
005	F400
006	E001
007	0006
008	0002
009	0004
00A	0000
00B	0000
00C	0000
00D	0000
00E	0000
00F	0000
010	0000

EXECUTING...

Output: 4

EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]