PCI Target Implementation using Verilog

PREPARED FOR

Dr. Ashraf Salem

TA. Tasneem Adel

PREPARED BY

Salma Hamed Ibrahim 1700616
Salma Sherif Kamel 1700619
Salma Abdelfattah Fetouh 1700622
Shorouk Ashraf Salem 1700676
Shimaa Abdelaziz Ibrahim 1700691

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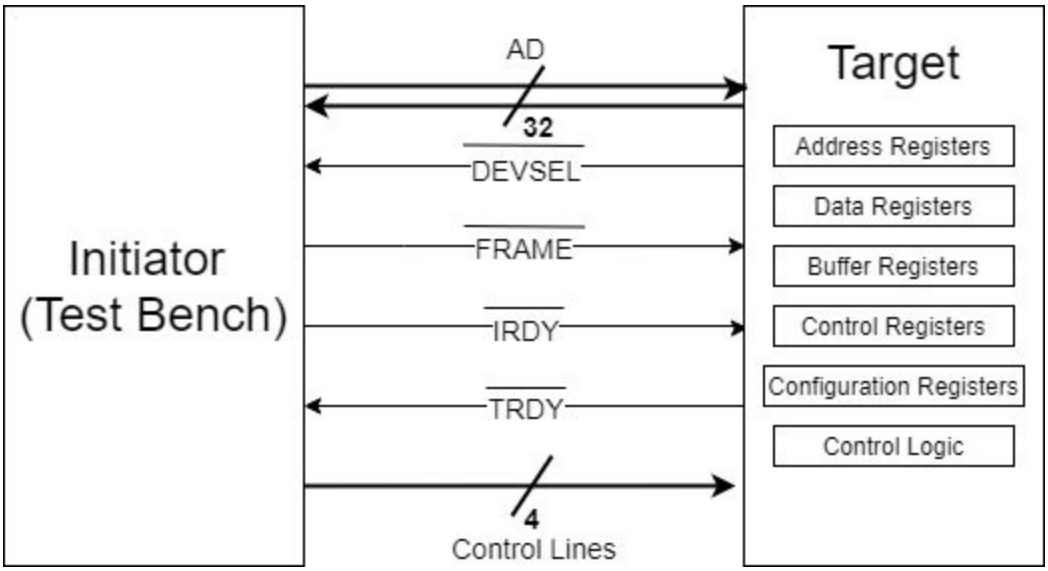
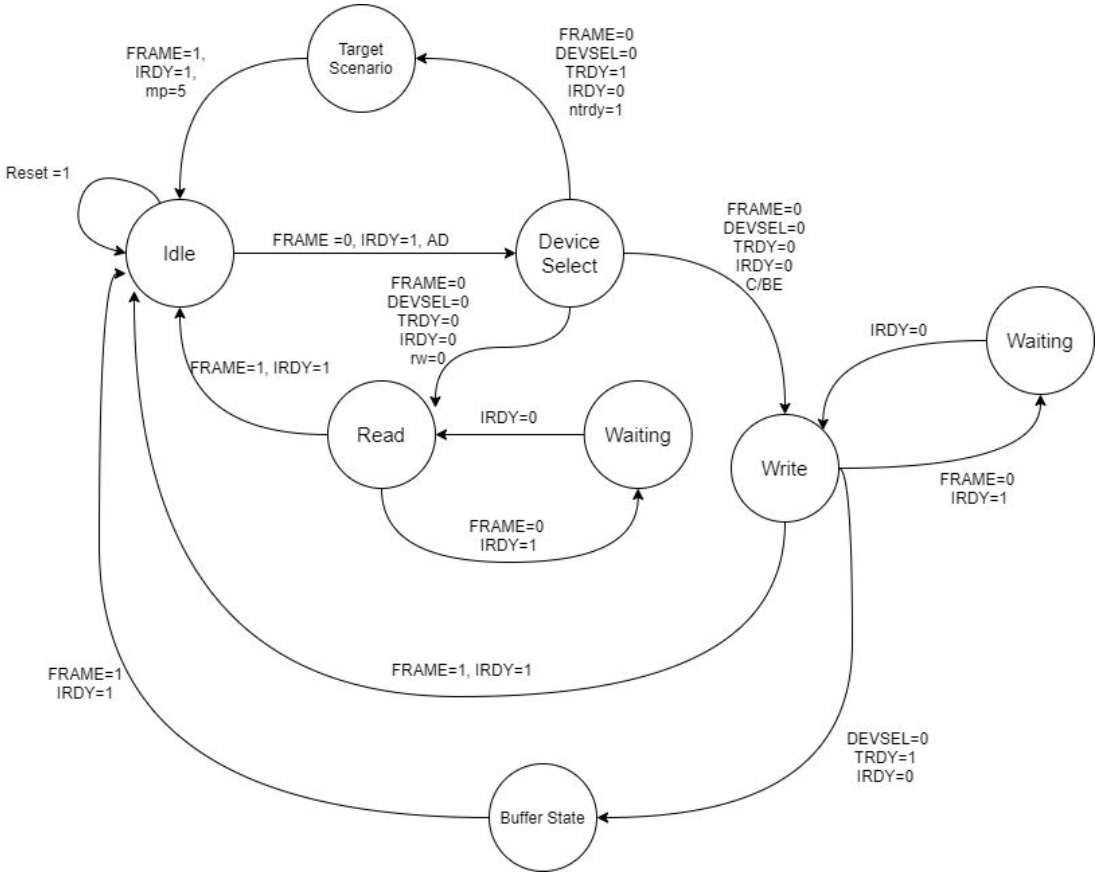
Block Diagram

1. The Whole system



[1]Fig 1.1

2. Finite State Machine diagram



[2]Fig 1.2

Description of signals

No.	Signal	Description	Type	Functional Group
1	CLK	Clock signal provides timing for all the transactions done by the PCI bus, it's an input to every PCI device.	Input	System pin
2	reset	It's a signal used to bring the PCI device to the idle state.	Input	System pin
3	FRAME	A master-driven signal to indicate the beginning and the end of a transaction.	Input	Interface Control pin
4	AD	Stands for Address/Data, as they're both multiplexed on the same lines in the PCI bus, a transaction consists of an address phase where AD is an input and a data phase where it's an output.	Input/ Output	Address and Data pin
5	DEVSEL	Stands for Device Select, it indicates that the target has decoded an address and identified it as its own.	Output	Interface Control pin
6	C_BE	Stands for Command/Byte Enable, as they're both multiplexed on the same lines in the PCI bus. During the address phase of a transaction, it defines the bus command. During the data phase of a transaction, it's used as a byte enable, which determines which byte lanes carry meaningful data.	Input	Address and Data pin
7	IRDY	Stands for Initiator ready, it indicates the master's ability to complete the current data phase of the transaction, it's asserted when the address phase is completed successfully. It's used in conjunction with TRDY. A data phase is completed when both IRDY and TRDY are asserted. During a write, IRDY indicates that the data present on AD lines are valid. During a read, it indicates that the master is prepared to accept the data to read it.	Input	Interface Control pin
8	TRDY	Stands for Target ready, it indicates the target's ability to complete the current data phase of the	Output	Interface Control pin

		transaction. It's used in conjunction with IRDY. A data phase is completed when both TRDY and IRDY are asserted. During a write, it indicates that the target is prepared to accept the data. During a read, it indicates that the data present on AD lines is valid.		
9	rw	A signal controlled by the master to determine whether the current transaction is a read or a write. It's a one-bit signal that takes the value 1 when the master wants to write and 0 when it wants to read. It's used to control the AD signal to either be input or output.	Input	
10	ntrdy	A signal that tells the target that we want to enter a scenario where the initiator will read and TRDY will not always be asserted.	Flag	

Assumptions & Notes

1. The system is composed of 3 modules; a target module, a clock generator module, a testbench which acts as an initiator.
2. We're assuming a fast response DEVSEL signal.
3. The reset signal is asynchronous.
4. A memory pointer is used to indicate which buffers that the initiator reads from or writes in.
5. We added two signals rw, and ntrdy, their descriptions are in the signals description table.
6. The code and signal definitions all apply to the PCI Local Bus Specification document of December 18, 1998.

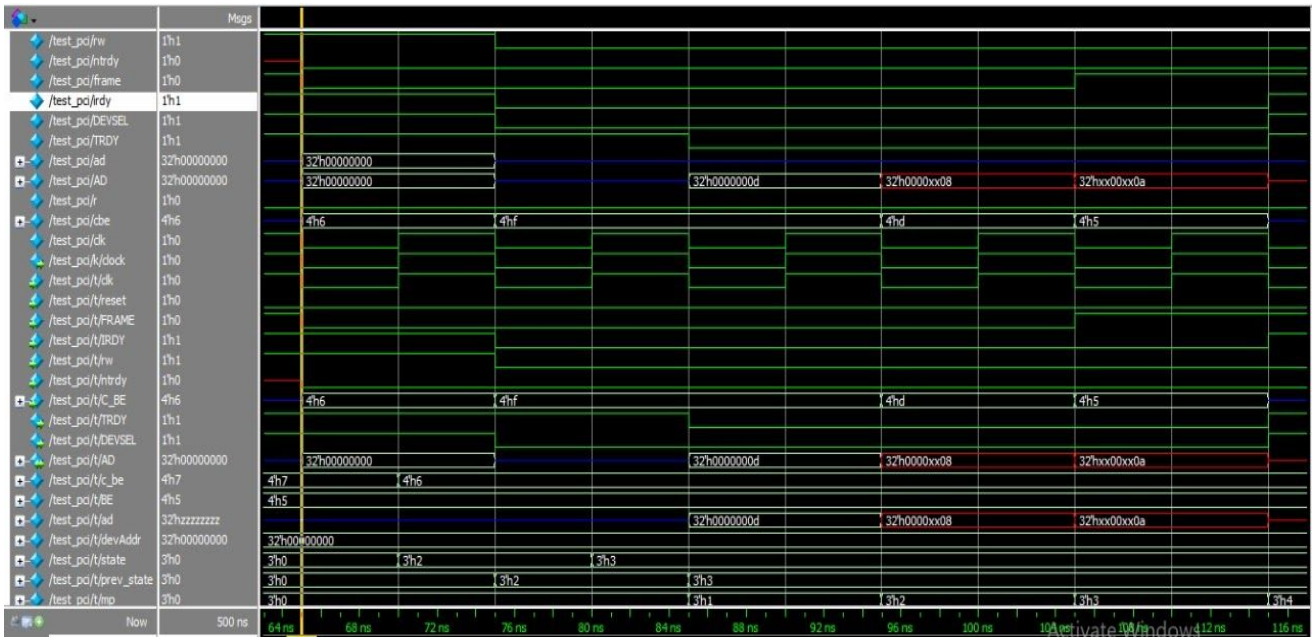
Different Scenarios

Scenario 1: Read transaction

Description

- A read transaction starts with an address phase which occurs when the FRAME is asserted. During this phase, AD contains a valid address (acts as input) and C_BE contains a valid bus command.
- A turnaround cycle is used after which the data phase starts. When IRDY, TRDY, and DEVSEL are asserted, the data phase begins.
- AD is assigned as an output using the signal rw, and it's set to high impedance.
- At the end of the transaction before the last data phase, the FRAME signal is deactivated. After that, IRDY, TRDY, & DEVSEL are deactivated.

Waveform



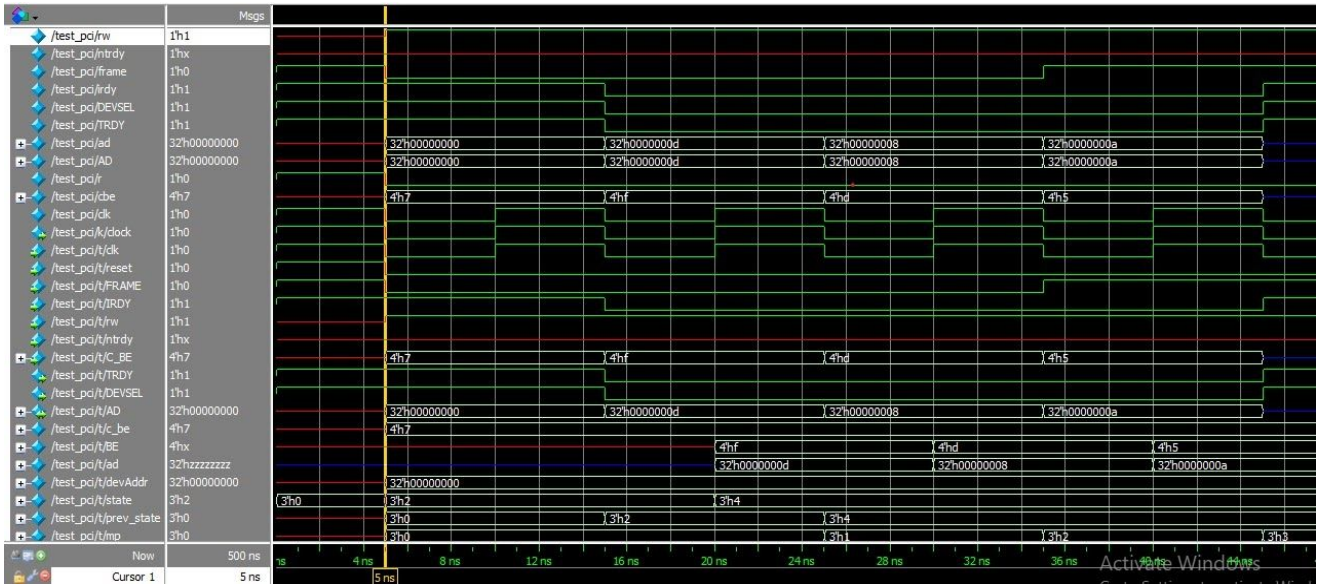
[3]Fig 4.1

Scenario 2: Write transaction

Description

- A write transaction starts with an address phase which occurs when the FRAME is asserted. During this phase, AD contains a valid address (acts as input) and C_BE contains a valid bus command.
- When IRDY, TRDY, and DEVSEL are asserted, the data phase begins.
- C_BE indicates the byte enable signals which determine which byte lanes will carry meaningful data.
- AD is assigned as an input using the signal rw, and it's set to take the value of the data from the initiator.
- At the end of the transaction before the last data phase, the FRAME signal is deactivated. After that, IRDY, TRDY, & DEVSEL are deactivated.

Waveform



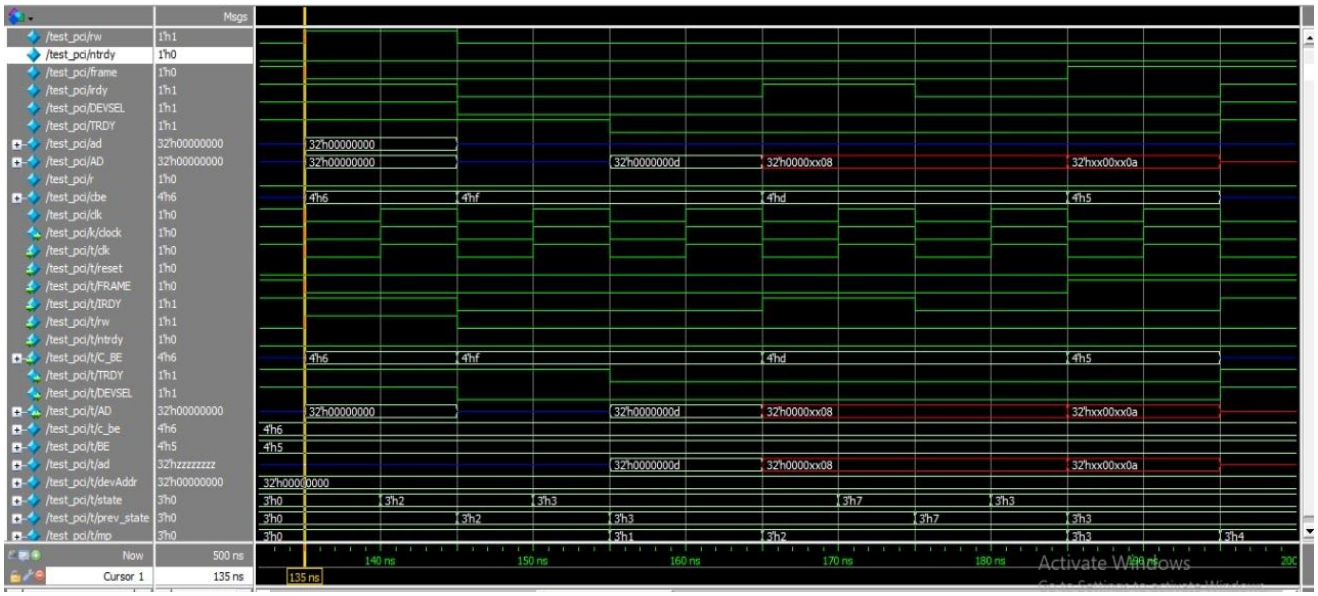
[4]Fig 4.2

Scenario 3: IRDY changes in the middle of the read transaction

Description

- A read transaction starts with an address phase which occurs when the FRAME is asserted. During this phase, AD contains a valid address (acts as input) and C_BE contains a valid bus command.
- A turnaround cycle is used after which the data phase starts. When IRDY, TRDY, and DEVSEL are asserted, the data phase begins.
- AD is assigned as an output using the signal rw, and it's set to high impedance.
- IRDY is deactivated in the middle of the data phase, which means that the initiator is busy.
- The data holds until the initiator is ready again and then it continues reading.
- At the end of the transaction before the last data phase, the FRAME signal is deactivated. After that, IRDY, TRDY, & DEVSEL are deactivated.

Waveform



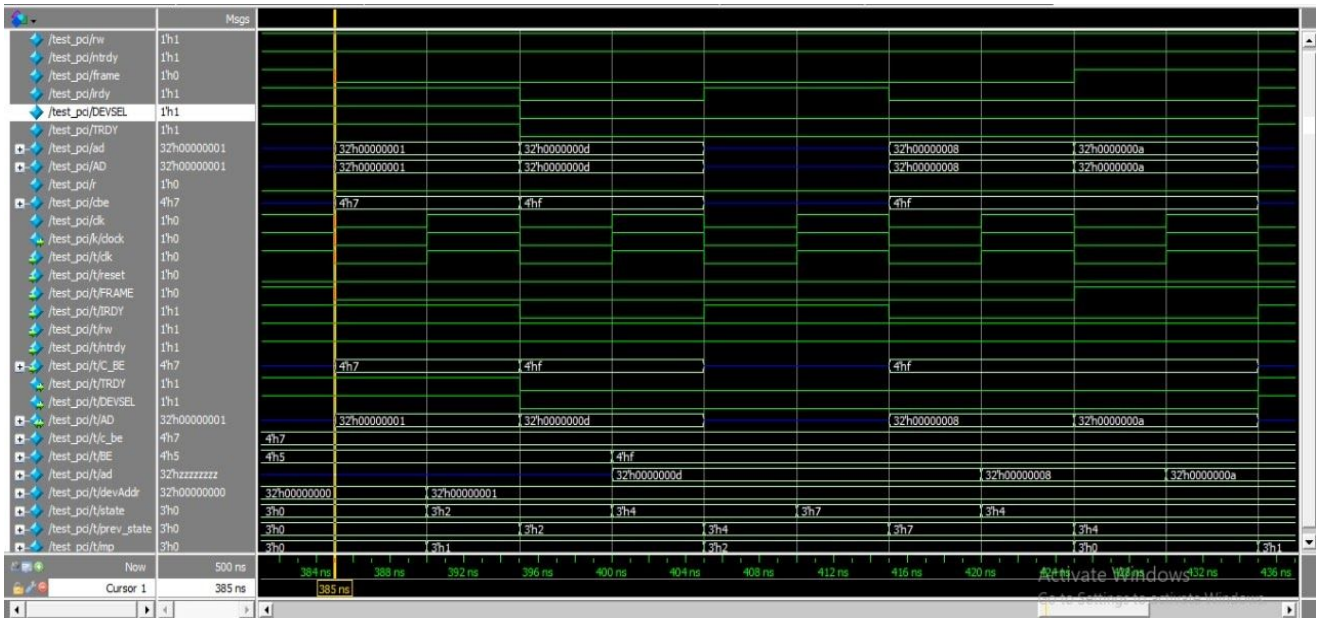
[5]Fig 4.3

Scenario 4: IRDY changes in the middle of the write transaction

Description

- A write transaction starts with an address phase which occurs when the FRAME is asserted. During this phase, AD contains a valid address (acts as input) and C_BE contains a valid bus command.
- When IRDY, TRDY, and DEVSEL are asserted, the data phase begins.
- C_BE indicates the byte enable signals which determine which byte lanes will carry meaningful data.
- AD is assigned as an input using the signal rw, and it's set to take the value of the data from the initiator.
- IRDY is deactivated in the middle of the data phase, which means that the initiator is busy.
- The data holds until the initiator is ready again and then it continues writing.
- At the end of the transaction before the last data phase, the FRAME signal is deactivated. After that, IRDY, TRDY, & DEVSEL are deactivated.

Waveform



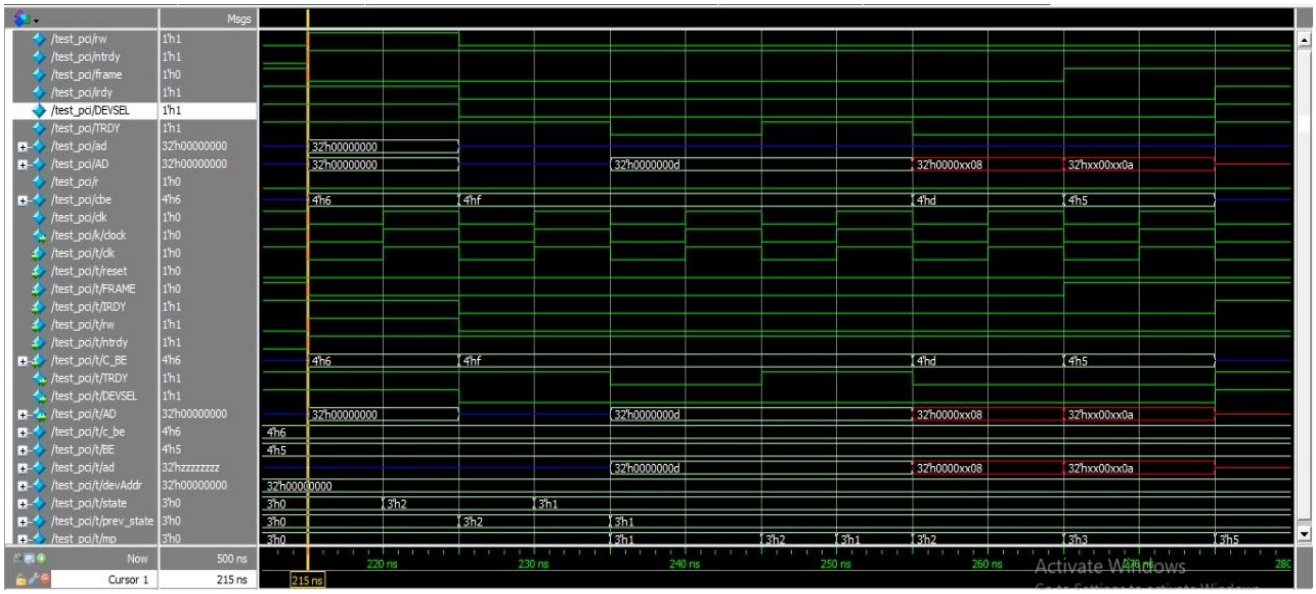
[6]Fig 4.4

Scenario 5: TRDY changes in the middle of the read transaction

Description

- A read transaction starts with an address phase which occurs when the FRAME is asserted. During this phase, AD contains a valid address (acts as input) and C_BE contains a valid bus command.
- A turnaround cycle is used after which the data phase starts. When IRDY, TRDY, and DEVSEL are asserted, the data phase begins.
- AD is assigned as an output using the signal rw, and it's set to high impedance.
- TRDY is deactivated in the middle of the data phase, which means that the target is currently unable to complete the master's request to read.
- The data holds until the target is ready again and then the initiator continues reading.
- At the end of the transaction before the last data phase, the FRAME signal is deactivated. After that, IRDY, TRDY, & DEVSEL are deactivated.

Waveform



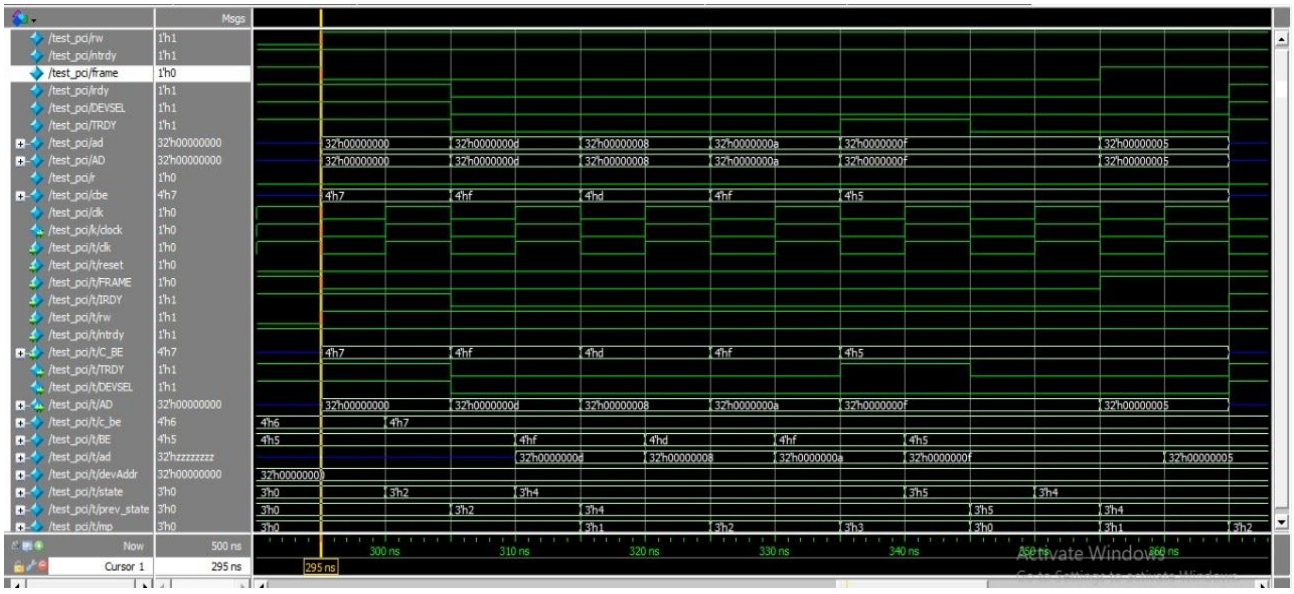
[7]Fig 4.5

Scenario 6: TRDY changes in the middle of the write transaction

Description

- A write transaction starts with an address phase which occurs when the FRAME is asserted. During this phase, AD contains a valid address (acts as input) and C_BE contains a valid bus command.
- When IRDY, TRDY, and DEVSEL are asserted, the data phase begins.
- C_BE indicates the byte enable signals which determine which byte lanes will carry meaningful data.
- AD is assigned as an input using the signal rw, and it's set to take the value of the data from the initiator.
- The target's memory was full, so an overflow occurred, which led to the deactivation of TRDY.
- TRDY is deactivated in the middle of the data phase, which means that the target is currently unable to complete the master's request to write.
- The data holds until the target is ready again and the target uses a memory buffer to empty a place for the coming data.
- TRDY is activated and the data phase completes.
- At the end of the transaction before the last data phase, the FRAME signal is deactivated. After that, IRDY, TRDY, & DEVSEL are deactivated.

Waveform



[8]Fig 4.6

Table of Contribution

Student	Code	Contribution
Salma Hamed Ibrahim	1700616	Scenario 1, prepared the presentation slides
Salma Sherif Kamel	1700619	Scenario 6, Block diagrams for the report
Salma Abdelfattah Fetouh	1700622	Scenario 2, wrote the description of scenarios 4, 5, & 6
Shorouk Ashraf Salem	1700676	Scenario 5, wrote the description of scenarios 1, 2, & 3
Shimaa Abdelaziz Ibrahim	1700691	Scenarios 3 & 4, the signals description table

Figures Reference