ESE 555 Final Project
Live demonstration: December 8
Project report in 4-page IEEE format: Due December 8

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The final project for the course is to design and verify a pipelined synchronous 8-bit carry select adder. The primary goal is to maximize the following design objective

$$Design\_Objective = \frac{f_{clock}}{PxA^{0.5}}\left(\frac{Hz}{Wm^2}\right),$$

where f_{clock} is the clock frequency, P is average power consumption, and A is the layout area.

In a multiple bit adder circuit, the carry generation is typically the critical path. Various architectures have been proposed to alleviate this issue, trading power and area with the delay of the carry generation path.

Carry select adder is a popular architecture that exploits this tradeoff. The carry-out is computed for both values of the carry-in before the actual carry-in is generated. Once the correct carry-in is generated, the corresponding carry-out is chosen utilizing a multiplexor. The primary inputs of your circuit will be carry-in, clock, reset, A0, A1,…., A7, and B0, B1, …., and B7. The primary outputs will be carry-out, S0, S1,….., S7. Each of these outputs should be able to drive an external load of 5 fF.

For this architecture, you will need to design the following building blocks:

Flip-flop
1-bit full adder
2-to-1 multiplexor

Since you will design an 8-bit adder, you should design a linear carry select adder with two blocks. Each block will have 4-bit adders where the carry ripples.

You should decide which circuit topology and circuit design technique (static or dynamic) to choose for the above blocks. Number of pipeline stages is also a design parameter that you need to decide. Objective is to maximize the design parameter mentioned above. This result will be the primary parameter that may play a role in the grading process. However, reliable operation and accurate functionality are the most important characteristics. The input data pattern and simulation time for verification are indicated at the end. The frequency of the data signals will dictate a minimum clock frequency. In other words, if the input data (A0---A7 and B0…B7) change at a frequency of *f,* the clock frequency used to sample this data should be much higher than *f*. Ensure that the design can correctly run at a clock frequency of 4 GHz. Assume that rise/fall times for clock and data signals are 25 ps.

Remember that, at the minimum, you have to place flip-flops at the primary inputs and primary outputs. In this case, the first output signals should be valid after the second rising edge of the clock signal (similar to your DFF assignments). After the first outputs emerge, every clock edge should produce the next outputs. Additional pipelining flip-flops within the circuit are upon your decision. For example, if you have 3 DFFs between the inputs and outputs, first outputs should emerge after the third rising edge. Then, every rising edge will produce an output. More pipelining will increase clock frequency at the expense of power and area. The aim is to maximize the design objective. Additional pipelining can achieve better design objective provided that the gain of higher frequency is not entirely offset by the increase in power and area. Note that the weight of the area is less than the weight of power and frequency according to the design objective defined above.

Your report, written in IEEE conference paper format (4 pages), should include the following:

Abstract – Summarize the project with several sentences mentioning your final design parameters such as speed, power, and area, and the design objective in the unit provided above.

Introduction – Discuss various adder topologies.

Carry Select Adder Design – This section should have four subsections

Block Level Architecture: Show the high level picture of the adder, describe its operation, describe your pipelining methodology, how you decided where to place the registers, and identify the critical path that determines your clock speed.

Flip-Flop: Describe the register you used.

1-Bit Adder: Describe the 1-bit adder that you used as a building block. Provide reasons for the topology you chose

2-to-1 Multiplexor: Describe the mux that you used.

Simulation Results: Show the extracted layout. Include post layout simulation results, illustrating successful operation at the clock frequency you chose. Also mention the power consumption and overall area. Report the design objective in units of $Hz/(Wm^2)$

Discussion: Discuss any points (about your design experience) that you believe is worth mentioning.

Conclusion: Conclude the project with a brief summary. Elaborate on possible improvements.

Appendix (does not count towards the 4-page limit): DRC and LVS reports.

Remember once again that correct functionality is number 1 priority. It does not matter how fast you can the circuit, if the outputs are incorrect.

PS: Report cannot exceed four pages. Page limit is strictly enforced, as in regular conference submissions.

Input pattern for testing

All signals have rise/fall times of 25 ps. You can convert the two 8-bit inputs and output signals into decimal representation to ease the verification. This setup will be used in the. Make sure your circuit works correctly.

A0: Period=4 ns, delay time=1 ns
A1: Period= 3 ns, delay time=0
A2: Period= 6 ns, delay time=5 ns
A3: Period= 2.5 ns, delay time=2 ns
A4: Period=12 ns, delay time=0
A5: Always 1
A6: Period=5 ns, delay time=12 ns
A7: Period=2.5ns, delay time= 3 ns
B0: Period=1 ns, delay time= 0
B1: Period= 9 ns, delay time=0
B2: Period= 14 ns, delay time=30 ns
B3: Period=3 ns, delay time=2 ns
B4: Period=2.5 ns, delay time=4 ns
B5: Period=5 ns, delay time=2 ns
B6: Always zero
B7: Period=4 ns, delay time=0
Cin: Always zero
Reset: High for 1ns, then always low

Simulate the circuit for 50 ns for functional verification and average power analysis.