International Institute of Information Technology, Hyderabad

(Deemed to be University)

EC2.101 - Digital Systems and Microcontrollers - Monsoon

Quiz 2: Set A Date: 19th October, 2023

All questions have ONE correct answer. Answers to be marked on the question paper itself

Max. Marks: 40

Max. Time: 30 min

+2 for correct answer, -1 for incorrect. NO CALCULATORS ALLOWED				
Name:		Roll No:		
Q1. Say we require a shift register that can perform left shift and right shift operations. How many mode selectlines are required?				
√a. 1	b. 2	c. 3	d. 4	
Q2. A shift register A h cycles?	as initial value 1011. Out	put is fed back to input. What is	the value after 1231 clock	
a. 1011	b. 1110	√ 6. 0111	d. 1101	
Q3. Say we require a se does it need to have?	quential circuit that can d	letect a unique 8-bit serial informa	ation. How many flipflops	
a. 1	b. 2	c. 3	√ 1. 4	
Q4. A binary multiplier a. 17	that can process two 16-b	oit inputs will have how many bit of c. 33	output?	
Q5. The ratio of number a. 1.6	rs that can be represented b. 1/1.6	by $4n$ -bit binary to that using BCI \checkmark . $(1.6)^n$ d.	O is: .(1/1.6) ⁿ	
Q6. A sequential circu (respectively) does its st	•	Flip-flops and k outputs. How i	many columns and rows	
a. n+m+k, 2 ^m	b. 2^n , $2^{(m+k)}$	$\sqrt{.}$ n+2m+k, 2 ^(n+m)	d. $n+m+k$, $2^{(n+m)}$	
Q7. Convert: (1.11) ₄ = (a. 1.75) ₁₀ V . 1.3125	c. 1.5	d. 2	
-	the output of a combination	onal circuit used as a multiplier for	r 3-digit BCD with 2-digit	
BCD number? a. 24-bit	b. 16-bit	c. 32-bit	✓. 20-bit	
Q9. The characteristic ed. $Q(t+1) = (S + Q(t))R'$ c. $Q(t+1) = S'R + Q(t)R$		is b. $Q(t+1) = SR + Q(t)R'$ d. $Q(t+1) = S'R + Q'(t)R'$		
Q10. We use a shift region communication?	ster, with delay of 25 ns f	For every shift, to transmit data ser	ially. What is the speed of	
√ . 40 Mbps	b. 5 Mbps	c. 5 Gbps	d. 20 Mbps	
Q11. Using a 4-bit 2's co	•	nich of the following additions wil	l result in an overflow? (i)	
a. (i) only	V. (ii) only	c. (i) and(iii)	d. All	

Q12. What is the primary char ✓. Feedback	racteristic that differen b. Input variables	tiates sequential circuits from c c. Output variable	
Q13. In a synchronous sequen a. On the rising edge c. Randomly	itial circuit, how are fli	p-flops triggered by the clock s b. On the falling edge 1. Depends on the design	signal?
Q14. In a sequential circuit, the a. The clock frequency c. The number of input variab	•	b. The circuit's power con d. The number of states th	sumption
Q15. What is the octal equival a. 355.243	lent of the binary numb . 316.514	per 11001110.1010011? c. 155.511	d. 356.121
Q16. What is the decimal equal a. 41296	ivalent of the hexadeci	mal number CAFE? c. 31786	d. 59812
Q17. Which of the following of a. One 4-input AND gate c. One 4-input AND gate, one		gates can decode binary 1101? 6. One 4-input AND gate, d. One 4-input NAND gat	
	_	th takes a single 4-bit BCD dig s, what is the minimum number 1.3	
Q19. Which of the following la. 1010	binary number is the sa b. 0101	ame as its 2's complement? 1000	d. 1001
Q20. In the octal system, was a. 45	hat is the result of su b. 71	biracting 75 from 146 ? c. 65	d. 73

Rough work