MAJOR PROJECT REPORT ON

STUDY OF

SCHOTTKY BARRIER TRANSISTOR USING BACK-GATING IN 2D CHANNEL

UNDER THE SUPERVISION OF:

Dr. Vandana Nath

(Assistant Professor)

UNIVERSITY SCHOOL OF INFORMATION

COMMUNICATION AND TECHNOLOGY

GURU GOVIND SINGH INDRAPRASTHA UNIVERSITY

SUBMITTED BY:

SALONI GUPTA

B.TECH-ECE

ENROLLMENT NO: 70216412816

DECLARATION BY CANDIDATE

This is to certify that the report entitled **"Study of Schottky Barrier Transistor using back-gating Effect in 2D channel**" is a bonafide record of project/research work done by me under supervision of **Dr.Vandana nath** and submitted to Guru Gobind Singh Indraprastha University in partial fulfillment for the award of the Degree of Bachelor of technology in Electronics and communication engineering. I Certify the content of the thesis are authentic, original and free from Plagiarism.

DATED **Signature of Student**

Saloni Gupta
B.tech (ECE)
(70216412816)

CERTIFICATE

This is to certify that the project report entitled **"Study of Schottky Barrier Transistor and back-gating Effect in 2D channel"** done by **Miss Saloni Gupta, enrollment no. 70216412816** is an authentic and original work carried out by her under my guidance. The matter embodied in this project has not been submitted earlier for the award of any degree or diploma to the best of my knowledge and belief.

Signature of the guide

Dr.Vandana Nath

ACKNOWLEDGMENT

First of all, I am grateful to The Almighty God for aiding me to complete this Major project. I feel to acknowledge my indebtedness and a deep sense of gratitude to my guide **Dr. Vandana Nath** whose valuable guidance and kind supervision given to me throughout the course which shaped the present work as its show. I would like to thank her for her assistance and insightful comments and for willingly sharing her expertise with me.

I would like to thank the Department of Electronics and Communication-USICT, GGSIPU who has played an important role in strengthening my career by providing full cooperation and encouragement throughout the tenure of the project.

Also, I am grateful to all my family members and their constant support.

TABLE OF CONTENT

Topics	Page Number
List of figures	7
List of Tables	8
List of Symbols and Abbreviations	9
1. **Chapter 1: Introduction**	10
1.1. Introduction and background	11
1.2. Working	14
2. **Chapter 2: Literature Overview**	16
2.1. Carbon nanotube	17
2.2. Growth Methods of Transition Metal Dichaleogenides	19
2.3. TMC Transistors	20
2.4. Electrical Contact on TMDCs	21
2.5. Fabrication and Characteristics of TMDC-2D-FETs	22
2.6. Characteristics of various TMDCs FET	24
2.7. Contact Effect in 2D FET	25
2.8. Device Fabrication	26
2.9. Current Injection Mechanism	27
2.10. Black Phosphorus transistors with MOSFET Analytical Barrier	28
2.11. Schottky Barrier FET Model	28
2.12. Bandgap Analysis and Extraction of Ionic Liquid Gated	31
2.13. Experimental Analysis	32
2.14. Tunnel FET in 2D TMDC	34
2.15. FET in Ambipolar Characteristics	36
2.16. FETs Silicon on insulation Schottky Barrier Utilizing dopant segregation	38
2.17. Switching Process in Transition metal Molybdenum Transistors	39
2.18. Simulated Device Characteristics	41
3. **Chapter 3: Software Required**	43
3.1. Objective	44
3.2. Introduction	44

3.3. DC Sweep 46
3.4. AC Sweep 47
3.5. Parametric Sweep 48
4. Chapter 4: Simulation and Analysis 49
Conclusion 51
Future Scope 54
References 56

List of Figures

1. Schottky Barrier 9
2. Symbol of Schottky Barrier Transistor 10
3. Schottky clamped transistor 13
4. Fabrication Process on 2D-FET 22
5. WSe_2 Phase image of the EFM 25
6. Schottky Barrier Field Effect Transistor Model 26
7. Transfer characteristics of SBFETs Model 26
8. Extracted Schottky barrier heights 30
9. Experimental device characteristics for various WSe_2 31
10. The scanning electron microscopic (SEM) image 33
11. Effect of the contact doping level and channel material 34
12. Schematics of the SB-MOSFET fabrication. 37
    a. Arsenic implantation into the contact regions,
    b. spacer formation and silicidation, and
    c. TEM image of a readily processed device.
13. Schematic view of device configurations. 42
14. DC circuit to run DC sweep analysis. 43
15. AC circuit to run AC sweep analysis. 44
16. Circuit Diagram of Schottky Barrier Transistor 45
17. Vertical nanowire SFET. 49

List of Tables

1. Comparison of TMDC-2D-FET Performance 24

2. Bandgap, Hole Effective Masses of dielectric constant 36

ABSTRACT

The failure of the conventional SB-FET model in the back gated 2D transistor domain, taking into account its success in modeling top gated transistors on 2D channels such as the ultrathin Si body, raises the question: "Is there a fundamental difference between these two structures? "Since the traditional SB-FET model treats an identical top gate and back gate, the comparison of top and bottom gated devices makes it possible to recognize their different channel effects. As in these layers Half-conductor devices touch nanometer level thicknesses, two-dimensional (2D) materials, for example Transitional metal dichalcogenides (TMDCs) are a natural alternative for use in such highly scaled materials Apparatus. One model based on physics was developed to understand how piezoelectric modulates the 2D-SFET bandgap. Landauer Simulations of ballistic transport show that an SS sub60mV / dec is achievable

3. INTRODUCTION

Schottky transistor is a combination of a transistor and a Schottky diode that prevents the transistor from saturating by diverting the excessive input current. It is also called a Schottky-clamped transistor.

Contemporary TTL logic families reduce storage time by placing a Schottky diode between the base and collector of each transistor that might saturate, as shown in the figure. The resulting transistors, which do not saturate, are called Schottky-clamped transistors or Schottky transistors for short.

When the input of a saturated transistor is changed, the output does not change immediately; it takes extra time, called storage time, to come out of saturation, which accounts for a significant portion of the propagation delay in the original TTL logic family. Storage time can be eliminated and propagation delay can be reduced by ensuring that transistors do not saturate in normal operation.

3.1 Schottky Barrier Diode

Schottky barrier is a depletion layer formed at the junction of a metal and n-type semiconductor. In simple words, Schottky barrier is the potential energy barrier formed at the metal-semiconductor junction. The electrons have to overcome this potential energy barrier to flow across the diode.

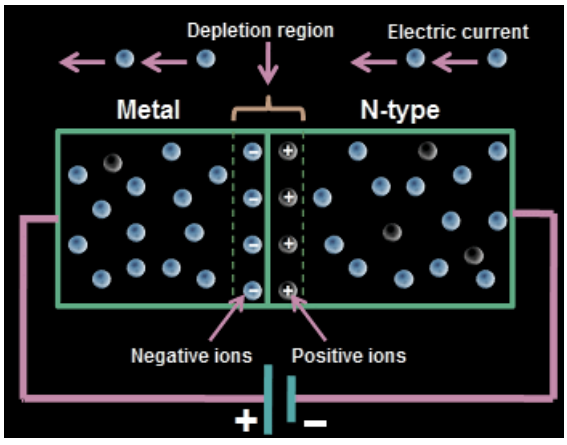


Figure 1: [1] Schottky Barrier Diode

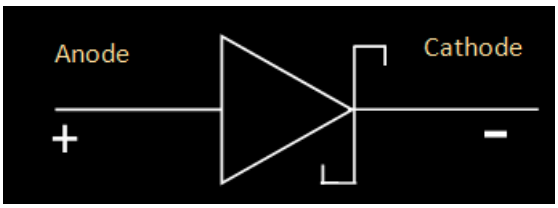


Figure 2: [2] Symbol of Schottky Barrier Transistor

The benefits of the Schottky diode are shown below:

- Because of the very limited amount of stored charge it has good recovery time. And this diode is used for use for high speed switching.
- It has low voltage turn on.
- It has poor capacitance for junction.
- Low voltage drop.

The Schottky diode's drawbacks show below-

- Present leakage invert.
- Score for low reverse voltage.

Application of Diode Schottky

- Used in power supplies which are switched-mode.
- Used in defence against reverse current.
- Designed for defence against discharges.
- Used in device for voltage clamping.
- Used in RF mixer and diode Detector.
- Used for application in solar cells

3.2 Schottky Barrier Transistor

Standard transistor-transistor logic (TTL) uses transistors as saturated switches. A saturated transistor is turned on hard, which means it has a lot more base drive than it needs for the collector current it is drawing. The extra base drive creates a stored charge in the base of the transistor. The stored charge causes problems when the transistor needs to be switched from on to off: while the charge is present, the transistor is on; all the charge must be removed before the transistor will turn off. Removing the charge takes time (called storage time), so the result of saturation is a delay between the applied turn-off input at the base and the voltage swing at the collector. Storage time accounts for a significant portion of the propagation delay in the original TTL logic family.

Storage time can be eliminated and propagation delay can be reduced by keeping the switching transistors from saturating. Schottky transistors prevent saturation and the stored base charge. A Schottky transistor places a Schottky diode between the base and collector of the transistor. As the transistor comes close to saturating, the Schottky diode conducts and shunts any excess base drive to the collector. (This saturation avoidance technique is used in the 1956 Baker clamp.) The resulting transistors, which do not saturate, are Schottky transistors. The Schottky TTL logic families (such as S and LS) use Schottky transistors in critical places.

In SB-FETs, I_{ds} have two components: thermionic emission current $I_{(Thermal)}$ over the 'top' of the SB and thermally assisted tunneling current $I_{(Tunnel)}$'through' the SB. Both of these current components depend on the applied gate bias (V_{GS}) which modulates the band movement in the semiconducting channel through the surface potential. It is assumed that a large drain bias (V_{DS}) is applied to eliminate the effect of the SB at the drain contact.

Schottky barrier is the potential energy barrier formed at the metal-semiconductor junction. The electrons have to overcome this potential energy barrier to flow across the diode. The rectifying metal-semiconductor junction forms a rectifying Schottky barrier. This rectifying Schottky barrier is used for making a device known as Schottky diode. The non-rectifying metal-semiconductor junction forms a non-rectifying Schottky barrier.

One of the most important characteristics of a Schottky barrier is the Schottky barrier height. The value of this barrier height depends on the combination of semiconductor and metal. The

Schottky barrier height of ohmic contact (non-rectifying barrier) is very low whereas the Schottky barrier height of non-ohmic contact (rectifying barrier) is high.

In non-rectifying Schottky barrier, the barrier height is not high enough to form a depletion region. So depletion region is negligible or absent in the ohmic contact diode. On the other hand, in rectifying Schottky barrier, the barrier height is high enough to form a depletion region. So the depletion region is present in the non-ohmic contact diode.

The non-rectifying metal-semiconductor junction (ohmic contact) offers very low resistance to the electric current whereas the rectifying metal-semiconductor junction offers high resistance to the electric current as compared to the ohmic contact. The rectifying Schottky barrier is formed when a metal is in contact with the lightly doped semiconductor, whereas the non-rectifying barrier is formed when a metal is in contact with the heavily doped semiconductor.

3.3 WORKING OF SCHOTTKY BARRIER TRANSISTOR

When forward biased, a Schottky diode's voltage drop is much less than a standard silicon diode, 0.25 V versus 0.6 V. In a standard saturated transistor, the base-to-collector voltage is 0.6 V. In a Schottky transistor, the Schottky diode shunts current from the base into the collector before the transistor goes into saturation.

The input current which drives the transistor's base sees two paths, one path into the base and the other path through the Schottky diode and into the collector. When the transistor conducts, there will be about 0.6 V across its base–emitter junction. Typically, the collector voltage will be higher than the base voltage, and the Schottky diode will be reverse biased. If the input current is increased, then the collector voltage falls below the base voltage, and the Schottky diode starts to conduct and shunt some of the base drive current into the collector. The transistor is designed so that its collector saturation voltage $V_{CE(sat)}$ is less than the base–emitter voltage V_{BE} (roughly 0.6 V) minus the Schottky diode's forward voltage drop (roughly 0.2 V). Consequently, the excess input current is shunted away from the base and the transistor never goes into saturation.

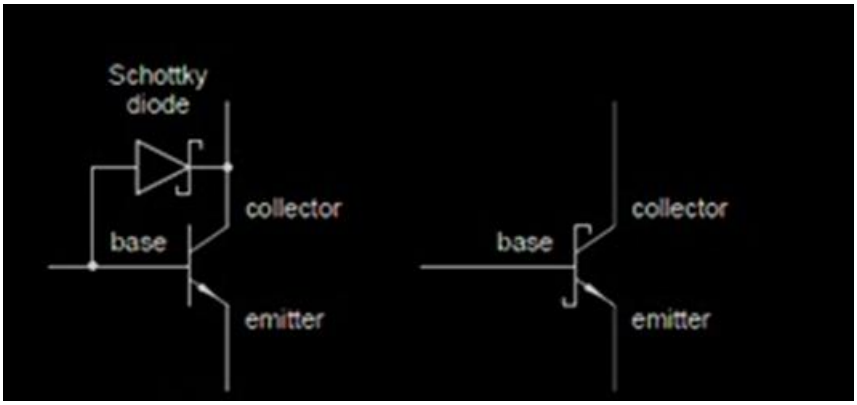


Figure 3: [2] Schottky Clamped Transistor

The first transistor was invented in 1947. Although the limits of scaling CMOS have been revised many times in recent years, there is no uncertainty that alternative design designs will at some point become relevant. There is a lot of material investigated and carbon nano tube was found to be one of the best among them for a nano technology purpose. Carbon nanotube exhibits both the metallic and semiconductor characteristics in it. Although in all cases a hollow cylinder the carbon nanotube can be formed by rolling a finite piece of a graphite sheet, the precise procedure in which the roll-up takes place has a drastic impact on the tube's dispersion interaction.

2. LITERATURE OVERVIEW

2.1 CARBON NANOTUBES

Nanotubes show one-dimensional (1-D) transport properties even at room temperature, due to the small diameter of carbon nanotubes. It suggests, for example, that because of the small phase space available, the scattering is strongly suppressed. Metallic nanotubes therefore exhibit scattering distances of many micrometers. It has been shown that semiconducting carbon nanotubes in the field-effect transistor (FET) configuration can be used as active elements. Latest electrical measurements on CNFETs and their characteristics are explored at the electrode-nanotube interface in the form of Schottky barriers (SBs). Manufacturing a carbon nanotube transistor requires a semiconducting tube to fill the gap between the source electrodes and drain them. Given that no scheme currently exists for the exclusive growth of either metallic or semiconducting carbon nanotubes, CNFETs are manufactured as follows. Next, the target dielectric film is grown or deposited on a degenerately doped silicone for a back-gated system. Then, by spinning onto the substrate, nanotubes formed by laser ablation are dispersed from a 1, 2-dichloroethane solution..

No scattering inside the carbon nanotube was included in our debate. This is based on our observation that the performance characteristics of SB-CNFETs differ significantly depending on which contact is used for the same carbon nanotube as the source and drain. This indicates that the SBs at the contacts are the primary factors in reducing the characteristics of the electrical system and not inwardly scattering.

The current is affected by the gate field through an SB-CNFET. In the source area, it is again the Schottky barrier which plays a crucial role in controlling the current through the system. Increasing the gate voltage bends the nanotube valence band closer to the source Fermi level. In doing so, the tunnelling barrier for hole injection get thinner.

With exceptional electrical properties, such as quasi-ballistic transport or high carrier mobility in the diffusive regime CNFET devices nowadays exhibit features surpassing those of state-of-the-art Si-based MOSFETs. Since it has been widely agreed that Si-based CMOS technology would hit its scaling limit in the next decade or so, the ability of carbon nanotubes will be explored as building blocks in future nanoelectronics.

Carbon nanotubes FET are fabricated using back gate geometry. A Si substratum is used with the SiO_2 as the dielectric barrier, as the back gate. E-beam lithography describes the sources

(S) and drain (D) touch patterns with a spacing of 300 nm. Three metals are used as Source and Drain contacts, namely palladium (Pd), titanium (Ti), and aluminium (Al). All metal contacts are evaporated by a typical lift-off in the same vacuum system at a base pressure of 10-8 Torr.

CNFETs have been found to be SB devices. Hole injection into the nanotube at the metal nanotube interface depends on the line-up of the Fermi metal level and the nanotube valence band, which is described here as the SB height. Transition metal dichalcogenides (TMDCs) are materials characterized by a MX_2 formula, in which M stands for a transition metal (Mo, W) and X stands for a chalcogen (S, Se or Te). Transition metal dichalcogenides are layered materials consisting of layers with an X-M-X structure. The M-X bonds are covalent within each layer, while separate layers are bonded through interaction with Van der Waals.

Recent studies have shown that micromechanical exfoliation, used to separate graphene monolayer's, is also an efficient tool for extracting thin flakes of specific TMD. Due to the thickness-dependent contrast on SiO_2/Si substrates, the layers can be identified using an optical microscope. Examples include MoS_2

Monolayer n-type field-effect transistors (FETs), MoS_2 photo-transistors, MoS_2 bilayer chemical sensors, logic gates, memory cells, and large MoS_2 flakes amplifiers. Additionally, top-gated p-type FETs is using monolayer WSe_2 and ambitious background FETs using multilayer WS_2 flakes.

To probe an exfoliated $MoSe_2$ flake electrically, we select a single terrace with uniform thickness to define the active field-effect transistor region. Combined with reactive ion etching using Cl_2 the Electron-beam lithography (EBL) is then used to identify the system active region.

2.2 GROWTH METHODS OF TRANSITION METAL DICHALCOGENIDES (TMDC)

Popular growth methods for obtaining TMDC materials that can be generally classified into three categories:

1. Chemical vapor transport

2. Powder vaporization and

3. Chemical vapor deposition.

The easiest method for obtaining few or single layer TMDC materials is by mechanical exfoliation and is the source of all the material presented in this work. While mechanical exfoliation provides material of high quality, it primarily produces material in the form of a few layers, and is not a scalable process. TMDC bulk crystals are either obtained from naturally mined crystals for mechanical exfoliation, as in the case ofMoS_2, or from chemical vapor transport (CVT). CVT is neither a new nor special technique for TMDC growth.

The compound constituents are transferred from the hot zone to the cold zone, where they gradually crystallize into a bulk crystal, with the help of a transport agent such as bromine or iodine. Both powder vaporization and deposition of chemical vapor can create wide area (> 100 μm), high yield monolayer films. The most popular methods of powder vaporization are a solid metal precursor such as MoO_3 or WO_3 and a solid S or Se chalcogen precursor with an ambient pressure carrier gas conveying the reactants to a growth substratum at a temperature of 600-950 ° C.

Although powder vaporization may generate large-scale growths (> $1cm^2$) with low variability and high mobility, e.g. 30-45 cm^2/V_s forMoS_2, process reproducibility and uniformity are relatively weak. Chemical vapor deposition with gas phase metal organic precursors (MOCVD) allows for much tighter control of the reactant chemistry.

2.3 TRANSITION METAL DICHALCOGENIDES (TMDC) Transistors

The back-gated structure is composed of a dielectric on a conductive substratum, typically 20-300 nm of thermally oxidized SiO_2 on heavily doped Si. The 2D material is exfoliated mechanically, moved onto, or grown directly on the dielectric and the contact metal is normally on top of the 2D material. The transistor is worked by having the source touch ground and applying a drain voltage. The current in the device is modulated by applying a voltage,V_{BG} , to the global back-gate.

Without prejudice at the gate, i.e., $V_{GS} = 0$, the system is in the OFF state since there are broad thermal barriers controlled by the Fermi distribution for both the injection of electrons into the conductive band (CB) and the valence band (VB) holes.

When adding a positive tension to the doors, i.e. V_{GS}>0, the energy bands in the 2D channel are displaced downwards by a quantity equal to the surface potential q believes where q is the electronic charge and where q is the channel structure. This allows electrons to be injected from the source into the 2D conductive band. Initially, this thermionic electronic current

increases exponentially with increasing magnitude of V_{GS} until the ON state, i.e. threshold voltage (V_{GS} =V_T) is reached, where the band movement almost stops.

Likewise, when a negative voltage is applied to the gate, i.e. for V_{GS}<0, the energy bands in the 2D channel are displaced upwards allowing holes from the drain to be inserted into the valence band of the 2D channel.

The hole current also increases exponentially with increasing magnitude of V_{GS} until the ON state is reached. A transistor which shows both electron and hole branches in the transfer characteristics is conventionally referred to as an ambipolar FET.

2.4 Electrical Contacts to (TRANSITION METAL DICHALCOGENIDES)TMDCS

1. Fermi Level Pinning: In traditional Si FETs, ohmic contacts are made by means of n+/p / n+ or p+/n / p+ replacement / impurity doping profiles for electron (n-type) and hole (p-type) injection, respectively. However, in the absence of these controllable doping schemes, early 2D-FET experiments were focused on the use of elemental metals with specific work functions for carrier injection into the respective band.

The energy of the conduction band,E_c, versus the vacuum level,E_{vac}, is given by the semiconductor electron affinity. A low work function metal with the Fermi level aligned close to the conduction band of the 2D material will facilitate electron injection, whereas, a high work function metal with the Fermi level aligned close to the valence band of the 2D material will allow easier hole injection.

Such metal-2D contacts are characterized by Schottky barriers (SBs) given by

$$\boldsymbol{\varphi_{sb-n} = \varphi_M - \gamma_s}$$

$$\boldsymbol{\varphi_{SB-P} = E_G + \gamma_S - \varphi_M}$$

Where $\varphi_{sb_n}$and φ_{sb_p} are, respectively, SB heights for electron and hole injection and EG is the band gap of the semiconductor.

2. Ambipolar Transport in 2D-FETs: When mechanically exfoliated on SiO_2, MoS_2 and $MoSe_2$ compounds were found to be electron-doped compounds as opposed to WS2

and WSe_2, which were found to exhibit ambipolar behaviour. Metals used for electrical contacts were alleged to play a major role in their response, probably by defining the size of the Schottky barrier associated with their function and by pinning the channel. The observed ambipolar response, or the ability to dope the conductive channel through the field effect with either electrons or holes, may make some of these TMDs suitable for complementary digital logic applications. Complementary metal-oxide semiconductors (or CMOS) are commonly used in modern electronics as well as in microprocessors, microcontrollers, static RAM and other digital logic circuits.

3.Current Injection Mechanism: The carrier injection mechanism from source / drain into the Schottky-barrier on / off-state silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistor by developing a refined extraction procedure for the Schottky barrier height estimation. This approach is applied to verify the mechanism suggested by using the dummy-gate in an underlap system with a thicker spacer and applying back-gate bias to SOI wafer. Based on their good tolerance to short-channel effects and adaptability to high-performance devices and high-speed devices, structured metallic source and drain (S / D) devices, called Schottky-barrier (SB) devices, were researched for possible applications in the nanometer regime as an alternative to traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) based on a p-n junction.

The carrier injection mechanism for SB devices based on extracted SBH was evaluated by quantifying the height of the barrier in SB units. The findings show that electron back-TU from the drain to the channel is the primary explanation for the leakage today. In addition, the extracted SBH also shows that the key mechanism of the leakage current is transferred from the TU of the electrons to the TE of holes as V_{bs} increases.

2.5 Fabrication and Characterization of TMDCs-2D-FETs

1. Substrate Preparation:

The first step is to obtain the substratum, which is either traditional thermally oxidized p++ Si with 20-285 nm SiO_2or 50 nm Al_2O_3on Pt / TiN / Si. Because the mechanical exfoliation process results in a random distribution of flakes on the surface. The wafer is protected by a layer of protective photoresis. If a thermally oxidized wafer is used, the back oxide must be etched wet in buffered oxide etch (BOE) so that the back-gate voltage can be applied to the

bottom of the substrate. Because of its HF-resistance, Shipley 1800 series photoresist is used. If Al_2O_3 is used on Pt / TiN / Si which has no back oxide, a photoresist layer of polymethyl methacrylate (PMMA) may be used instead.

2. Exfoliation

Graphene's successful exfoliation from bulk graphite paves way for the fabrication of other graphene-like 2D material through the simple “Scotch tape method”. Due to high quality monolayer’s occurring from mechanical exfoliation, this method is popularly used for intrinsic sheet production and fundamental research. Nevertheless, this method is not suitable for practical applications on a large scale due to its low yield and disadvantages in controlling sheet size. Chemical exfoliation could largely increase production than mechanical exfoliation, whereas sonification during this process would cause defects to 2D lattice structure and reduce flake size down to a few thousand nanometres, limiting the applications of 2D nanosheets in the field of large-scale integrated circuits and electronic devices.

3. CVD Synthesis:

The CVD method has drawn widespread interest as it could synthesize 2D TMDCs on a wafer scale, which demonstrates tremendous potential for practical applications such as integrated large scale electronics. This method could not only produce continuous single film with a certain thickness, but also highlight heterostructures with direct growth, which would effectively avoid contamination of the interfaces.

4. Vapor-solid growth from MoS_2 powder:

In 2013, Sanfeng Wu and his colleagues proposed a specific and straightforward method of synthesis based on a vapor-solid growth mechanism, demonstrating the preparation of monolayer MoS_2films on different isolating substrates

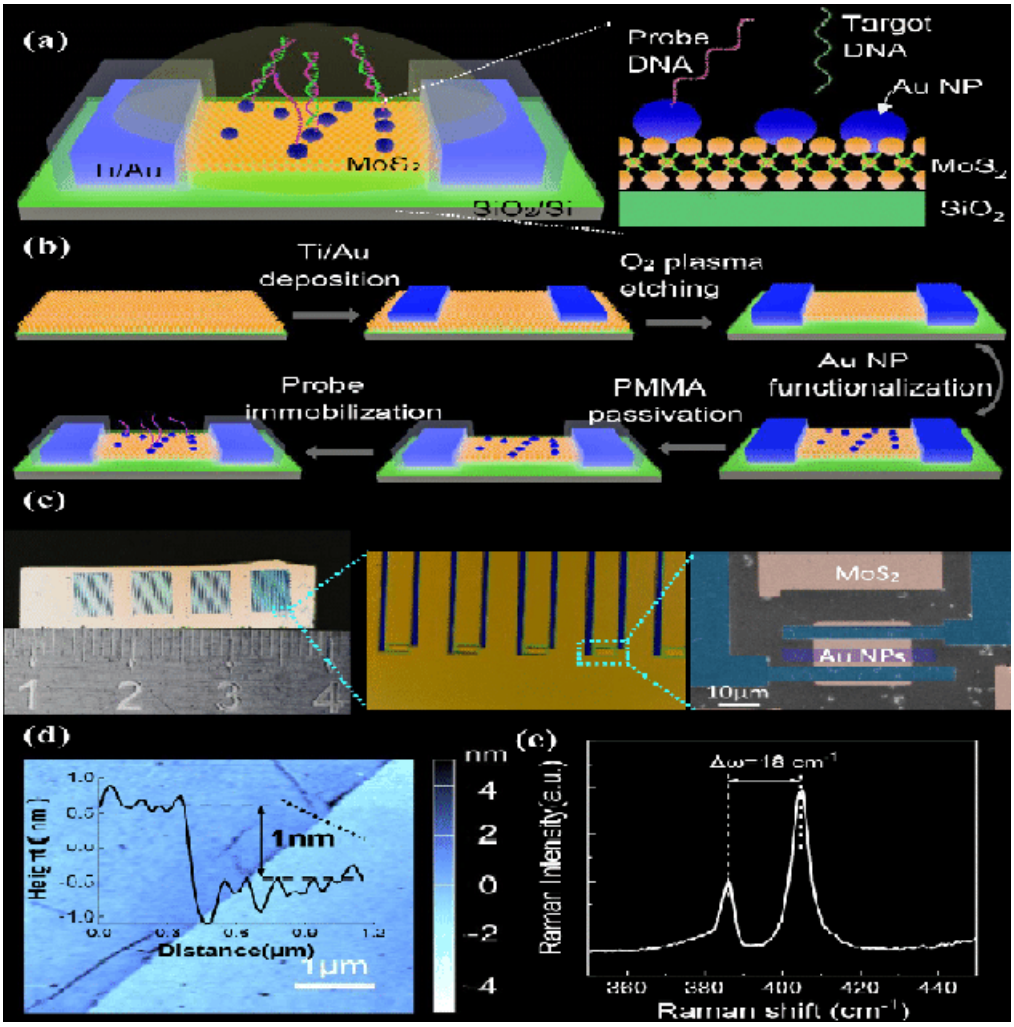


Figure 4: [3] Fabrication Process of 2D-FET.

2.6 Characteristics of various TMDCs FET

When benchmarking nanoscale FETs, the key metrics are usually the sub threshold slope (SS), contact resistance (RC), field effect mobility (μ), ON state current, and the presence of SCEs. The small EOT of 22 nm, coupled with the good high electric field characteristics of the Al_2O_3, enables steep SS, large channel carrier concentrations and thus large ON state currents. For both MoS_2 and WSe_2, large positive V_{BG}, max values still slightly shift V_T more positive but devices can still be pushed deep into the n-branch ON state.

Material	Y function	V	SS	Ion	Carrier Density	Devices
MoS_2	25.0	-7.3	362	273	2.2*10^13	13
$MoSe_2$	22.2	-0.5	216	110	10^13	19
$MoTe_2$	0.92	8.4	2560	5.1	6.6*10^12	7
WS_2	63.5	1.1	146	198	1.1*10^13	16
WSe_2	23.2	1.7	500	107	8.3*10^12	8

Table 1: Comparison of TMDCs-2D-FET Performance.

2.7 **Contact Effect in 2D-Dimensional field effect transistor**

We propose and theoretically examine a spin transistor (spin MOSFET) type of Metal – oxide – semiconductor field-effect-transistor (MOSFET) consisting of a source and drain MOS structure and half-metallic-ferromagnetic (HMF) contacts. When the HMF source and drain magnetization configuration is parallel (antiparallel), strongly spin-polarized carriers are injected from the HMF source into the channel and transported back in the HMF drain.

Our two-dimensional numerical analysis indicates that in parallel (antiparallel) magnetization, the spin MOSFET exhibits high (low) current drive capability and those extremely large magneto current ratios can be obtained. In addition, the spin MOSFET meets other essential "spintronic integrated circuits" specifications, such as high amplification capacity, low power delay product.

Contact effect in dual gate structure

For a simple BG geometry, it is not possible to separate the channel effect under the contacts from the rest of the channel, as the BG electrostatics regulates both simultaneously. This includes a dual-gated apparatus.

Back gate Characteristics:

The most common techniques adopted to extract the threshold voltage (VTB) of back gated 2D FETs are the constant current and the Y-function methods, used for Si FETs. The Y-function method is generally robust and yields accurate results independent of whether the contacts are Schottky or ohmic in nature.

Ambipolar Transport in 2D-FET

Tungsten diselenide (WSe_2) has many excellent properties and provides outstanding potential in valley-based electronics, spin-electronics and optoelectronics applications. In order to facilitate the digital and analog application of WSe_2in CMOS, an understanding of the underlying behaviour of ambipolar hole and electron transport is important. The P-type and n-type transistors are the basic elements for building complementary metal-oxide-semiconductor (CMOS) electronics based on silicon to realize digital and analog applications. Usually, high density unipolar p-type and n-type transistors are manufactured using different doping techniques and are used for the construction of logic circuits. The spatial separation requirement in circuits makes manufacturing more difficult, resulting in increased manufacturing costs. By comparison, innovative transistors, which can be conveniently switched between p-type and n-type by adding an electrical field, promise candidates to reduce the size of the circuit with simpler designs.

2.8 DEVICE FABRICATION

The WSe_2 flakes were mechanically exfoliated using adhesive tape from a bulk crystal onto a SiO_2/Si wafer. The FETs were produced using electron beam lithography on a single wafer, simultaneously displaying all the devices with the same processing phase to ensure uniformity. The source and drain electrodes were deposited by electron beam deposition with a deposit speed of 0.2 Å/s. Until evaporation of the electron beam, the samples were placed under the high vacuum of the electron beam deposition device for overnight. To ensure the same conditions all the devices were deposited simultaneously. Before measurement, devices were annealed under Ar (including 10%H_2) at 200 °C

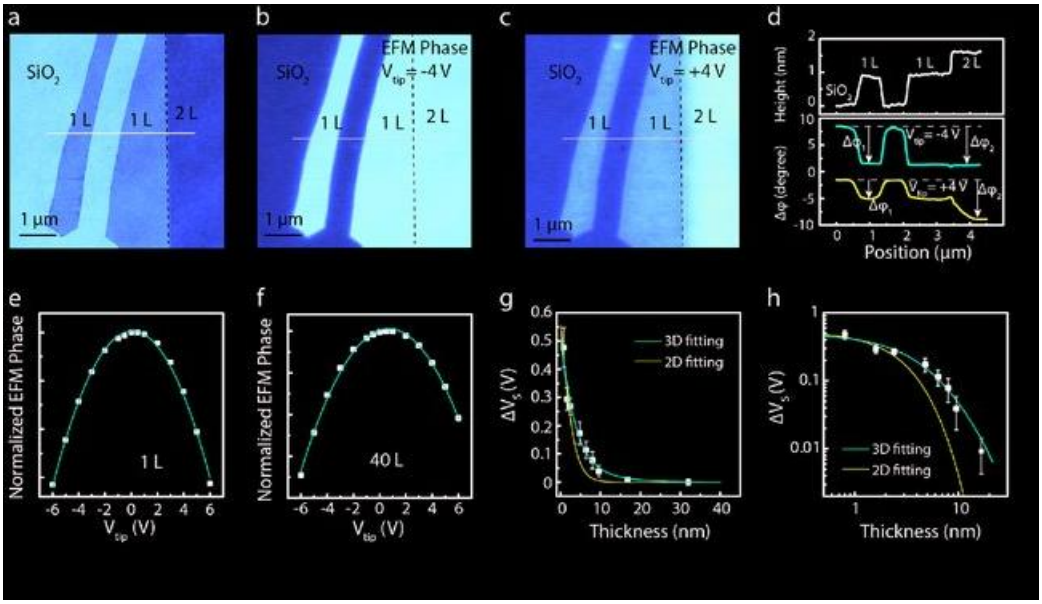


Figure 5: [4] WSe_2 phase image from the EFM. A.1L and 2L WSe_2 AFM height image and an image of the corresponding phase measured by EFM. B. V tip = −4 V. C. V tip = + 4 V. D. Profiles in line in (a-c). E, F Second-degree polynomial adjustment to 1L and 40L WSe_2 uniform EFM stages, respectively, under V tips varying from + 6 to −6 V. G. The surface potential depends on the thickness layer as well as on the thickness layer.

2.9 Current injection mechanism in Schottky-barrier metal-oxide-semiconductor field-effect transistors.

Based on their good tolerance to short-channel effects and adaptability to high-performance devices and high-speed devices, structured metallic source and drain (S / D) devices, called Schottky-barrier (SB) devices, were researched for possible applications in the nanometer regime as an alternative to traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) based on a p-n junction. This structure is very basic, and by controlling the deposited metal thickness and annealing temperature, ultra shallow junctions can be easily and precisely shaped with very low parasite S / D resistance. By leveraging the advantages of this structure, we have demonstrated a 20 nm gate-length device as well as the memory device based on an SB node.

While in previous researches the carrier injection mechanism from the S / D to the channel in SB devices was intensively investigated for the on-state, the mechanism of leakage current in the off-state has seen relatively less study. Unlike traditional systems, the height

of the barrier can be modulated at the interface by adjusting the line-up between the Fermi metal level and the Fermi semiconductor level. Consequently, the impact of the barrier height can determine the carrier injection mechanisms: on-state and off-state thermionic emissions (TE) and tunnelling (TU) associated with the gate (V_{gs}) and drain bias (V_{ds}).

We focus on the details of the carrier injection mechanism, based on the different back and drain electrode bias conditions. A refined extraction method is developed specifically to extract effective SB height (SBH). The carrier injection process is quantitatively analyzed for both on- and off-state in SB devices by the use of the refined extraction method. We manufactured a simple SB MOSFET p-channel on a silicone-on-insulator (SOI) wafer. Platinum was deposited and then annealed in a furnace at 300 ° C for 30 min to form a metallic silicided S / D. SB system manufacture information can be found elsewhere.

2.10 Black phosphorus transistors with MOSFET analytical barrier.

Much more ultra-thin body devices have been explored since the first carbon nanotube transistors were built and characterized in 1998 and found to be behaving as Schottky barrier metal-oxide-semiconductor field-effect transistors (SB-MOSFETs). Whether in the case of ultra-thin silicon slab structures, silicon nanowires, nanowires or more recently transition metal dichalcogenides (TMDs) all of these exploratory three-terminal devices with metallic source and drain contacts and a channel that is gated from the source-to-channel to the drain-to-channel interface showed a variety of characteristics that are common for SB-MOSFETs.

Due to the wealth of material and interface properties that can be extracted from the electrical characteristics of the SB-MOSFET, we recently discussed in a number of independent publications how to identify the current at threshold, flat band or at the minimum current point of the $I_{ds} - V_{gs}$ characteristics in order to determine the bandgap (Eg) involved in the current transport as well as the actuation of the current transport. One downside of this approach is the confusion associated with determining certain individual points at which to measure the existing values. The extraction method must also be changed, depending on the exact nature of the $I_{ds} - V_{gs}$ characteristics. Ideally, rather than evaluating distinct current levels of the device, the entire off-state device characteristics should be described by our Schottky barrier model.

2.11 Schottky barrier field-effect transistor model

A SB-MOSFET consists of a semiconducting channel that is contacted by metal – source / drain electrodes along with a gate terminal that modulates the channel potential. In traditional transistors the doped source / drain regions, which form a p – n junction with the channel material, are replaced by metal contacts. One consequence of this shift in the device's structure is that the MOSFET's n- or p-nature is determined by the source / drain metal Fermi level line-up to the channel's semiconductor bands, rather than the channel doping form.

Ever, the ultra-thin body nature of materials typically used for SB-MOSFETs makes the characteristic length scale π rather small over which band bending occurs at interfaces between metal and semiconductor. The $\boldsymbol{\lambda}$, which defines band shape at the metal – semiconductor interface, is controlled by the doping level of the channel for devices with bulk semiconductor channels. Increasing the semiconductor doping decreases the depletion distance and helps the electrons to tunnel with greater probability through the barrier.

Hence, λ is now defined by the body thickness. When the semiconductor channel thickness is only a few nanometres, the tunnelling probability through both electron and hole barriers becomes large and this gives rise to ambipolar transfer characteristics.

An example of the expected I_{ds}–V_{gs} at room temperature for such a line-up is plotted using open black circles. The total current I_{ds} can be decomposed into two branches: I_{hole} and $I_{electron}$. Key points in the transfer characteristic have been labelled (i)–(iv) to highlight the different regions in each branch. The I_{hole} branch can be broken up into two separate regions, the thermal region and the tunnelling region, separated by a transition point called the flatband voltage.

The band diagram at flatband voltage ($V_{fb,S}$) for I_{hole} is shown. As is evident from Figure at this gate voltage the bands on the semiconductor side of the metal–source interface side are flat. In the hole thermal region ($V_{gs}>V_{fb,S}$), I_{hole} is a pure thermionic emission current over the barrier defined by the valence band in the channel region. As the valence band in the channel is lowered by applying a higher positive V_{gs} the barrier becomes larger and the current decreases exponentially. The ideal inverse sub-threshold slope of the I_{ds}–V_{gs} in this region, when the interface trap and depletion capacitances are both zero, is $\approx$60 mV dec^{-1} at room temperature. In the hole tunnelling region ($V_{gs}<V_{fb,S}$), I_{hole} is a combination of thermionic emission and tunnelling currents.

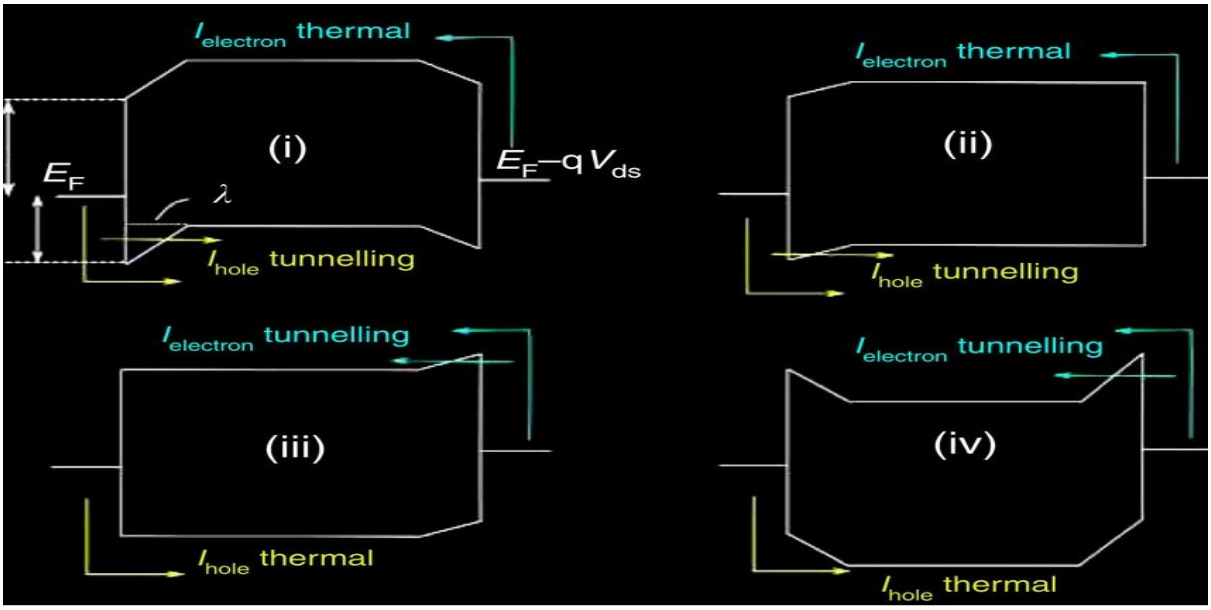


Figure 6: [5] Schottky Barrier Transistor Model

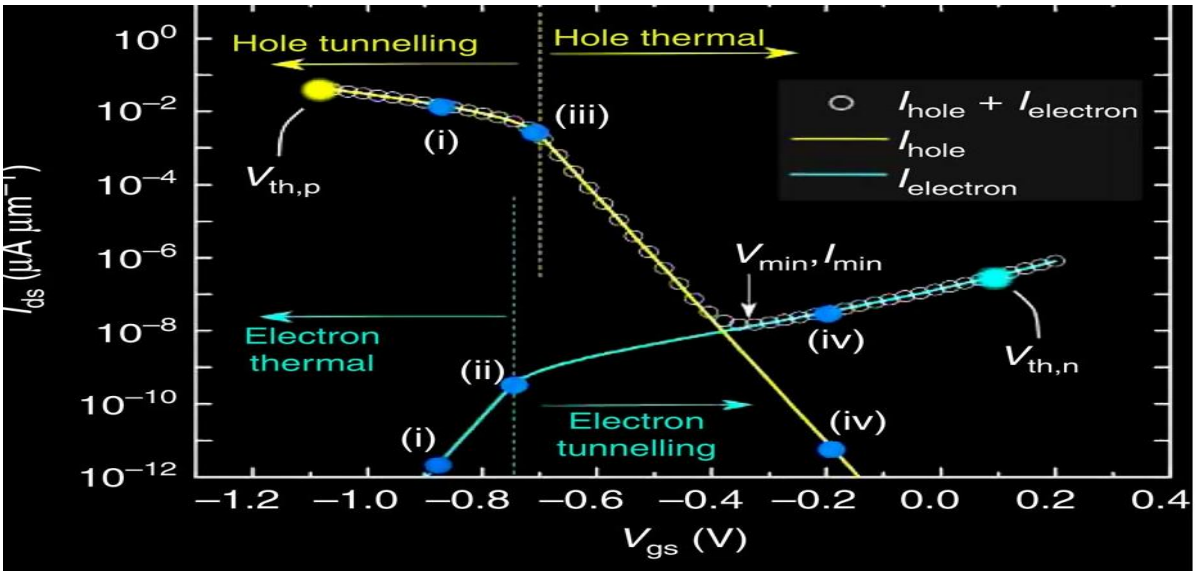


Figure 7: [5] Transfer characteristics of Schottky barrier transistor Model

So, the channel potential can be modulated linearly with gate voltage if we assume that the interface trap capacitance is approximately constant across the bandgap. The current per unit width I_{ds} through the device can be written as:

$$\boldsymbol{I_{ds} = \frac{2q}{h} \int_{x}^{E_x} T(E)\, M_V(E)\, [f(E) - f(E - qV_{ds})]\, dE}$$

Where,

$$\boldsymbol{M_v(E) = \frac{g_r}{\pi h}\sqrt{2\,m_h^*}\left(E_v(V_{gs}) - E\right)}$$

Where $E_v > E$ represents the number of modes per unit width in the 2D channel, g_v is the valley degeneracy and m_h^* is the hole effective mass. T (E) is the net transmission through the source and drain Schottky barriers and f is the Fermi–Dirac function. V_{ds} is the drain-source voltage that drives current flow in the device and E_v is the valence band edge in the gate-controlled channel region, the part of the channel that is controlled only by the gate terminal of the SB-MOSFET.

To measure the tunneling probability of the source and drain junctions separately, we used a semi-classical WKB approximation then. The transmission T (E) was calculated through the device, where Rs (d) =1−Ts (d) was calculated. The gate voltage travels up / down the flat portion of the channel region and thereby shifts the barrier form at the source and drain. Therefore, the applied gate voltage defines the channel potential, which affects the available $M_v - E$ modes in the channel and also the transmission through the tunneling barriers for source and drain.

For a triangular-shaped barrier, the probability of tunnelling through the forbidden region into the valence band is calculated using the semi-classical one-dimensional WKB approximation as:

$$\boldsymbol{T_{WKB}(E) = exp\left(-\int_{x_m}^{x_o} K(E)dx\right)}$$

$$\boldsymbol{K(E) = \frac{1}{h}\sqrt{2m_h^*}\left(E - E_v(x)\right)}$$

Where xm (at the metal-semiconductor (M – S) junction) and x_0 (x at which E = Ev) are the positions of two classical turning points at energy E, $E_v(x)$ is the maximum position-dependent valence band energy, the effective valence band mass and E is the interesting energy.

2.12 Bandgap Analysis and Extraction of Ionic Liquid Gated WSe_2Schottky Barrier Transistors.

$WSe_2$is an important member of the TMD family because of its smaller effective electron and hole masses relative to most other TMDs and, more significantly, because of the optimistic nature of its electrical characteristics, i.e. the ability to support the injection and transport of electrons and holes. For the extraction of the desired bandgap information as a function of thickness, we built so-called ultrathin body Schottky barrier (SB) FETs where the entire channel between the metallic source and drain electrodes is gated. Using a model developed by us. We quantitatively examine the characteristics of the WSe_2SB-FET to gain insight into the bandgap dependence on the number of TMD layers involved in transport.

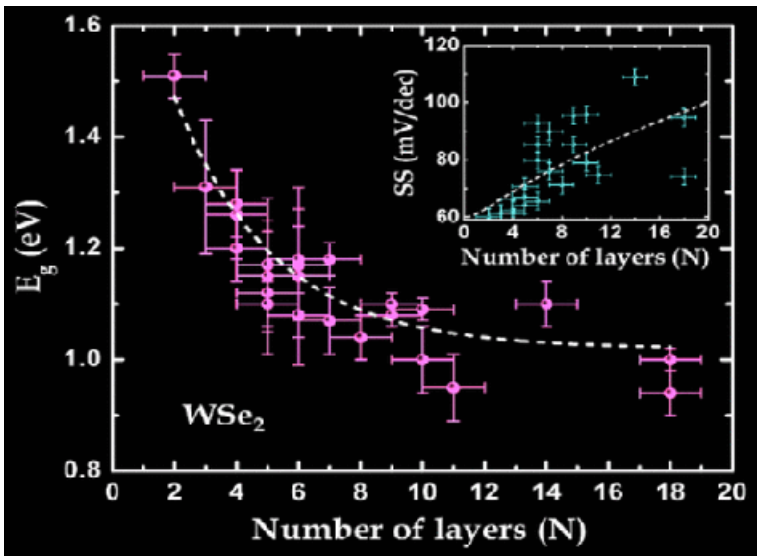


Figure 8: [4] Extracted Schottky barrier heights as a function of flake thickness for WSe_2 with Ni as the contact metal.

2.13 Experimental Analysis

Flakes were exfoliated micromechanically on substrates with 90 nm SiO_2as the top layer and heavily doped Si beneath the SiO_2. The lithography of electron beams accompanied by evaporation of electron beams was used for the description of source / drain terminals. The channel lengths shall be 1.5 μm. Ni is used as the source / drain electrode metal with a passivation of Ti / SiO_2on each electrode to protect against the ionic liquid gate used to affect the channel potentials. Following proper calibration and atomic force microscopy (AFM), flake thicknesses were determined by optical contrast.

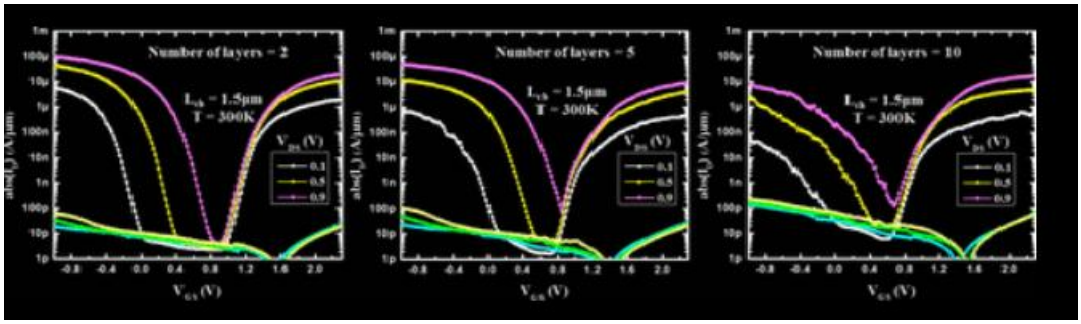


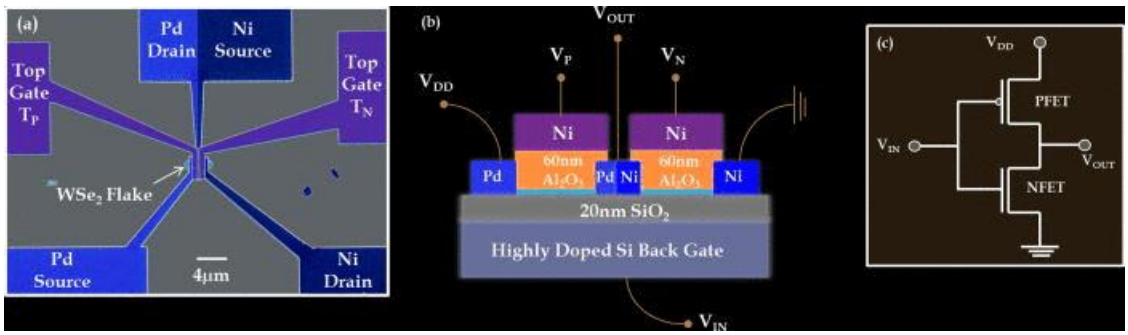
Figure 9: [6] Experimental device characteristics for various WSe_2 channel body thicknesses.

With this set of control experiments in place we are now in a position to study how the device characteristics of WSe_2 SB-FETs are impacted by the thickness of the channel, *i.e.*, t_{body}. Figure displays the dependence of device characteristics on body thickness showing two trends that are quantitatively analyzed in the following: (i) change of SS and (ii) change of V_{TN-n} and V_{TP-p} and thus bandgap.

As the revolutionary path of silicon based complementary metal oxide semiconductor (CMOS) field effect transistor (FET) nears its end of scaling, the interest in novel materials grows exponentially. One dimensional nanotube, quasi one dimensional nanowire, and two dimensional layered semiconductors are being extensively investigated in order to find the solution to the CMOS scaling challenges. Although low dimensional systems allow aggressive channel length scaling by the virtue of their excellent electrostatic integrity, there are many fundamental and technological obstacles that prevent their commercial implementation. For example, in spite of having the highest carrier mobility and the potential to reach ballistic transport, the most studied 2D material graphene is falling behind due to the absence of a bandgap while nanotubes and nanowires are suffering from sorting, placement and variability challenges. Recently, a lot of focus is being directed to transition metal dichalcogenides (TMDs) like MoS_2, $MoSe_2$, WSe_2, and others. The existence of a finite bandgap along with the ultra-thin body nature makes the TMDs extremely appealing in the context of post silicon CMOS. TMDs also offer unique and versatile electrical, optical, mechanical, and thermal properties. FET, gas sensors, photo detectors and even mechanical resonators have been demonstrated with mono and few layer TMDs. TMDs are being implemented in flexible and transparent electronic circuits as well. The progress in exploring the electronic properties of a wide range of

TMDs has been outstanding, but it also raises critical questions like which TMD would be best fitted in the CMOS platform.

In this context,WSe_2, which is another member of the semi-conducting TMD family, is more promising given the availability of both electron and hole transport. Metal Fermi levels are pinned close to the middle of the WSe_2 bandage and thus allow injection into both the conduction and the valence band. However, the performance of such WSe_2FETs on the ON state device is limited since carriers have to tunnel through a large Schottky barrier. WSe_2flakes were mechanically exfoliated onto a substratum of 20 nm thick silicon dioxide (SiO_2), with highly doped silicon as the back gate. Using 20 nm SiO_2instead of traditional 300 nm SiO_2as the dielectric back gate not only enhances electrostatic gate regulation but also increases the transparency of Schottky metal barriers to WSe_2contacts by reducing the screening length ÿ. This allows efficient injection of the carrier into both the conduction and the WSe_2valence band. Pd was used as the source / drain metal contacts for the PFET to manufacture the inverter structure, and Ni was used as the source / drain metal contacts for the NFET in accordance with our earlier findings which indicated better Pd injection of the hole and efficient Ni injection of the electron into the respective WSe_2bands. 50 nm Al2O3, deposited using atomic deposition layer technique (ALD) was used as the dielectric top gate and Ni was used as the metal top gate electrode for both PFET and NFET.



1(a) 1(b) 1(c)

Figure 10: [7] 1(a) shows the scanning electron microscopic (SEM) image of the inverter fabricated on a bi-layer WSe_2 flake. Figure 1(b) shows the device structure schematically, and Figure 1(c) shows the equivalent circuit representation of the WSe_2 complementary inverter.

2.14 Tunnel Field-Effect Transistors in 2-D TMDC.

Power consumption for future electronics is one of the main challenges. Tunnel field-effect transistors (TFETs) are among the most promising candidates for future integrated circuits (ICs) because of their slight sub-threshold swing (SS) and low OFF current. Having limited SS and OFF-current reduces both the ICs' static power consumption and dynamic power consumption one of the TFETs' main disadvantages is their low ON-current. The current in the TFETs is the result of the carrier's Band-to-Band tunnelling. The probability of tunneling is usually much lower than and as a result, the TFETs ON-current is much lower than conventional FETs. However, the likelihood of tunneling will increase considerably if the tunneling region's electric field is high enough. In this sense, atomically thin 2-D devices are very important for TFET applications, similar to nanotubes because of the tight channel gate regulation resulting in high electrical fields at the tunnel junction.

The well-known scaling length theory can be used to quantify the effect of gate control on the electric field at the tunnel junction. This theory provides a simple analytic way to understand how various device parameters affect the spatial variation of the potential along the channel described by a modified 1-D Poisson equation.

$$\frac{d^2V}{dx^2} - \frac{V}{\lambda^2} = 0$$

Where V and λ are the electrostatic potential and the natural scaling/decay length of the potential, respectively. In double-gated FETs, λ is given by

$$\lambda = \sqrt{\frac{\in_{ch}}{2 \in_{ox}}\left(1 + \frac{\in_{ox}}{4 \in_{ch}} \frac{t_{ch}}{t_{ox}}\right) t_{ch} t_{ox}}$$

Where $\in_{ch}$ and $\in_{ox}$ are the dielectric constants of the channel and oxide, respectively, while t_{ch} and t_{ox} are their thicknesses. According to given equation reducing the channel thickness reduces the natural scaling length of the potential, which results in higher electric fields and ON-currents.

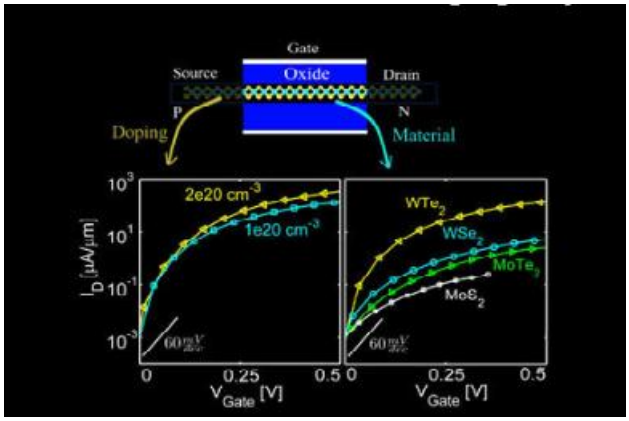


Figure 11: [8] Effect of the contact doping level and channel material on the performance of TMD TFETs

Parameters	MoS_2	WSe_2	$MoTe_2$	WTe_2
Eg[eV]	**1.68**	**1.56**	**1.085**	**0.75**
M_e^***[mo]**	**0.52**	**0.36**	**0.57**	**0.37**
M_h^***[mo]**	**0.64**	**0.5**	**0.75**	**0.3**
$E_t[in]$	**4.2**	**4.5**	**8**	**5.7**

Table 2: Bandgap, Hole Effective Masses and IN plane of plane relative dielectric constant.

2.15 Field-Effect Transistor with Ambipolar characteristics.

One of the crucial features of a semiconducting channel material for complementary logic transistor applications is the electron and hole transport symmetry, which is expressed in similar drive current capabilities for both the n-FET (field effect transistors) and the p-FET. This symmetry lies in the accessibility of the electrons in the conduction band and the holes in the valence band for transporting the charge and is determined by the relative location of the Fermi contact level with the semiconductor's energy bands.

If the Fermi contact rates coincide close to the semiconductor's conductive band, the electron injection is prevalent while a line-up close to the semiconductor's valence band converts into effective hole injection. In silicon CMOS and most of the bulk semiconductors, the Fermi contact level position can be changed by replacing the contact regions with doping. However, the lack of a controllable and sustainable substitutional doping scheme in low-dimensional systems poses serious challenges for the design of contacts. Metals with different work functions are used in such systems to inject either into the conduction band function or into the valence band. Remember that these metal-to-semiconductor contacts are almost always Schottky barrier contacts, and thus, the height of the respective Schottky barrier defines the efficiency of carrier injection. The height of this Schottky barrier can theoretically be determined from the difference of the metal's work function and the semiconductor's electron affinity. In experiments, however, effects such as Fermi level pinning, mechanical atom deformation in the contact field, and other non-idealities require specific approaches to determine the true height of the Schottky barrier.

Single layer WSe_2 consists of a stack of three hexagonally packed selenium-tungsten-selenium atomic layers with heavy intralayer covalent and ionic bonding. In comparison, bulk WSe_2 is a single-layer stack, held together by poor van der Waals interlayer interaction, and thus allows for mono or few layers to be micromechanically exfoliated.

2.16 Efficient Schottky barrier minimizing field-effect transistors in silicone-on-insulator Schottky barrier utilizing dopant segregation.

The effect on the efficiency of Schottky barrier devices with dopant segregation of varying silicon-on-insulator and gate oxide thicknesses. It is shown that due to the improved electrostatic gate control, a combination of both ultra-thin silicon bodies and gate oxides with dopant segregation yields even more enhanced device characteristics that greatly relax the need for low Schottky barrier materials to realize high-performance Schottky barrier transistors.

While field-effect scaling of transistor devices continues, Schottky barrier metal-oxide-semiconductor field-effect transistors (SB-MOSFETs) provide an enticing alternative to traditional devices with heavily doped source and drain contacts. Because of metallic electrodes in direct contact with the tube, SB-MOSFETs exhibit low extrinsic parasite

resistance, give easy processing, and require well-defined geometries of devices down to the smallest dimensions. Recent progress in silicidation has revived interest in SB-MOSFETs and they have demonstrated devices with excellent high-frequency performance because of the Schottky barrier.

Dopant segregation (DS) has recently been used during siliconization to boost Schottky contacts in SB-MOSFETs and to change the working of completely silicon gates. DS has two advantages: first, siliconization at low temperatures; thus, thermally activated dopant diffusion is suppressed resulting in steep doping profiles at the silicon-silicon interface. Second, a very thin, highly doped interface layer forms that greatly increases the probability of carrier tunneling through the SB.

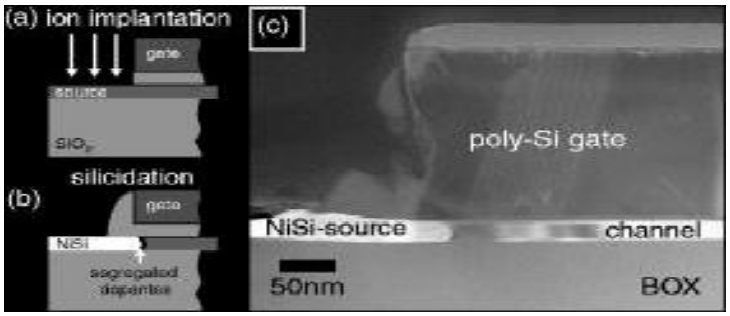


Figure 12: [9] Schematics of the SB-MOSFET fabrication. (a) Arsenic implantation into the contact regions, (b) spacer formation and silicidation, and (c) TEM image of a readily processed device.

Effect of dopant segregation on the output of SB-MOSFETs with varying SOI and gate oxide thicknesses during siliconisation. It has been shown that it can achieve a dramatic reduction of the effective SB height. Experimental devices displayed dramatically improved on- and off-state. Simulations show that the use of ultra-thin SOI body and ultra-thin gate oxides allows for even greater improvement due to a more drastic reduction of the effective SB height. Thus, DS and ultrathin body and oxide systems combine excellent intrinsic performance with the unique benefits of SB-MOSFETs.

2.17 Switching process in single-layer Transition metal Molybdenum Transistors.

The growth of 2D semiconducting crystals has provided significant potential for future electronic and photonic devices. High performance MoS_2 transistors, based on single-layer or multilayer crystals, have been demonstrated with the following properties: fair electron

mobility from several dozens to hundreds, high drive current, low sub threshold swing, and superior tolerance to short channel effects. MoS_2 Transistors provide many advantages over bulk semiconductor transistors. Firstly, MoS_2 atomically flat nature results in inherently low surface scatting, allowing the thickness of the channel to be scaled to the subnanometer regime. Conversely, at this channel width, the rough surface of ultrathin body (UTB) silicon will result in extreme surface scattering for carriers. Second, in addition to its incredibly thin structure, MoS_2 dielectric constant is relatively low making it more resilient against short-channel effects than silicon. To demonstrate, a single-layer MoS_2 transistor with 1 nm equivalent oxide thickness (EOT) will yield a characteristic screening length of 0.7 nm, a remarkably small number compared to traditional bulk semiconductor transistors. Third, high density of states, combined with the high effective mass, will result in good transistor efficiency at the scaling limit.

However, there are still many technological issues and obstacles ahead, to understand all the benefits of MoS_2 transistors. Researchers have encountered two bottlenecks for the further production of MoS_2 transistors in recent years of comprehensive studies on MoS_2 : difficulty with dielectric integration and great contact resistance. The first issue with regard to dielectric integration is crucial to achieving low EOT on top of MoS_2 . In the absence of bonds on the crystal surface, dielectric growth is dependent on physical adsorption of precursors for atomic deposition layer (ALD). This physical adsorption process interferes with the self-limiting nature of the ALD process which makes it challenging to shape a low-EOT dielectric defect-free on top. The second problem, the great contact resistance, stems from the presence of the Schottky barrier at the interface between metal and MoS_2 . A Schottky barrier is visible on all metal and semiconductor interfaces due to Fermi-level pinning. A common solution to solving this issue is to dope the semiconductor heavily, so electrons can easily tunnel from the metal to the semiconductor.

Despite the relatively low barrier height for electrons, varying from 30 to 230 meV depending on back gate bias and contact metal work function, the barrier has a profound effect on the efficiency of the device. The presence of the Schottky barrier is causing the MoS_2 transistor to work very differently from traditional Si MOSFETs. In this article, by studying the contact properties in single layer MoS_2 transistors we take a deep look at the role of the Schottky barriers in MoS_2 transistors from the device perspective. Instead of measuring the heights of the Schottky barrier, we calculate the contact resistivity and the

duration of transfer for the junctions, and see how they shift with gate voltage. Our findings show that the length of the transfer is inversely proportional to the voltage of the gate, and this relationship shows the existence of current flows in single layer MoS_2 transistors across the junction and the switching mechanism. The function of the system is dominantly regulated by tuning the effective heights at source and drain contacts of both Schottky barriers, rather than the potential barrier in the pipe.

The final device structure is illustrated in Figure. We use the global back gate to modulate these devices instead of the top gate because the global back gate can better modulate both carrier density in the channel and the Schottky barrier across the contact. This provides us a more direct view of how contact resistance and channel resistance change individually under the same gate voltage, in order to better reveal how the MoS_2 transistor operates at different bias conditions.

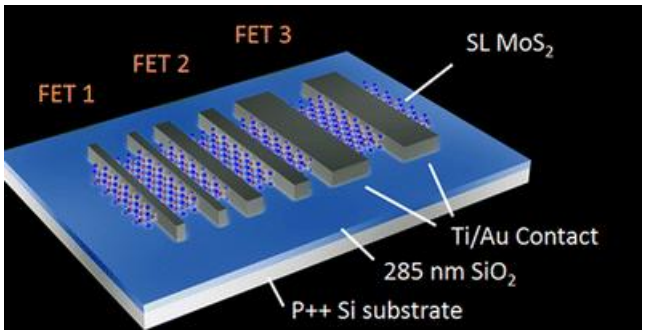


Figure 13: [10] Schematic view of device configurations. P++ silicon wafer capped with 285 nm SiO_2 was used as the global gate and gate dielectric, respectively

2.18. Simulated Device Characteristics

Landauer ballistic transport simulations the transistor 2D-SFET was simulated using a Landauer based ballistic transport model. The electrostatics and charge in the channel,Q_s , for an NMOS transistor .φ_N is the initial barrier height, φ_T is the band movement given by equation $(\varphi T = \varphi S + \varphi_{EG})$, $D_2 D(E)$, $f_{s,d}(E)$ is the Fermi function at the source or drain contact, g_v is the valley degeneracy, $m^*$is the electron effective mass, ħ is the reduced Planck's constant, ƙ is Boltzmann's constant, and T is the temperature (assumed to be 300K).

Note that bulk MoS_2 has six-fold valley degeneracy compared to twofold in monolayer, thus a 3X larger density of states. The general form for the ballistic current, i.e. assuming

no scattering and a transmission (E) =1, where (E) is the number of 2D conducting modes. W and E_c are the channel width and conduction band energy,

$$\boldsymbol{V_{GS} = \varphi_S + \frac{Q_S}{C_{ox}}}$$

$$\boldsymbol{Q_s = q\int_{\varphi_n-\sigma_T}^{\infty} D_{2D}(E)\,\frac{[f_s(E) + f_D(E+qV_{DS})]}{2}\,dE}$$

$$\boldsymbol{f_s(E) = \frac{1}{e^{\frac{E}{kT}} + 1}}$$

$$\boldsymbol{f_D\,(E) = \frac{1}{e^{E+qV_{DS}/kT} + 1}}$$

$$\boldsymbol{D_{2D}(E) = g_v\frac{m^*}{\pi h^2}}$$

$$\boldsymbol{I = \frac{2q}{h}\int_{\varphi_N-\sigma_T}^{\infty} T(E)M(E)[f_s(E) - f_d(E)]\,dE}$$

$$\boldsymbol{M(E) = \frac{g_v G}{\pi n h}\sqrt{2m^*(E-E_c)}}$$

3. SIMULATION AND ANALYSIS

3.1 SOFTWARE REQUIRED (PSPICE)

3.2 OBJECTIVE

A primary aim of this lab is to familiarize yourself with the use of PSpice and to learn how to use it to help you analyze the circuits. The program is already installed on every station's machine. Basically an introduction to PSpice. It is your duty to learn how to use it in greater depth, because you can use it during this semester and in the future.

3.3 Introduction

In PSpice the program we run is called CAPTURE in order to draw circuit schematics. PSPICE is the software that will let us run simulations and see graphical results. From the software you can run simulation, where your schematic is. There are a lot of things we can do with PSpice, but the most important things you need to know are = Design and draw circuits = Simulate circuits = Test simulation results (Probe for older versions) you won't need complete CAPTURE capability for this course.

The devices we will use are resistors, inductors, condensers and other independent / dependent sources. Knowing that CAPTURE has extensive symbol libraries and includes a fully integrated symbol editor to create your own symbols or modify existing symbols is a good idea. The main tasks in CAPTURE are

- Creating and editing designs
- Creating and editing symbols
- Creating and editing hierarchical designs
- Preparing your design for simulation

3.4 DC Sweep

Compose the schematics shown in Figure. The type of analysis you need to set up is DC Sweep. Make sure the sweep variable is Voltage source. Type in V1 as the name of the source. Make sure the sweep type is linear and use 0V, 2V and 0.01V for the start value, end value and increment, respectively. Run the simulation. We are interested in graphing the diode current versus the diode voltage. Once the simulation has finished you will see a black window with no graph in it. Select Trace/Add trace from the trace menu. You will see now a window with all the variables you can add to your plot. Select I (D1). Note that the x-axis variable is V_V1 and we need to change it to V (D1:1). Select Plot/Axis settings... from the Plot menu, Click on Axis Variable..., select V (D1:1). Now look for the value of V (D1:1) when the current I (D1) is 1mA. Select Trace/Cursor/Display from the Trace menu. A small window called probe cursor will appear. You have two cursors, A1 is controlled with the left button of your mouse and A2 is controlled with the right button of your mouse. Use one of them to find the point requested. Once you have the point, select Plot/Label/Mark from the Plot menu. The coordinates of the point will show up. Select Trace/Cursor/Display from the Trace menu and now you can move the coordinates to a better place in case they are over the curve. Click over the coordinates and hold the button down, move the mouse to place them in a better place then release the button. You can add labels to the plot just to make sure people who see your work know what you are showing. Select Plot/Label/Text from the Plot menu, type in the label "Diode's I-V characteristic" and then place wherever you want on the plot by moving the mouse and drop it by left clicking.

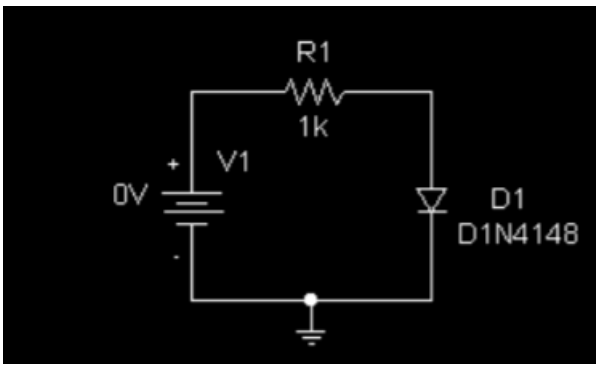


Figure 14: [11] DC circuit to run DC sweep analysis.

3.5 AC Sweep

Compose the schematics shown in Figure. Use the part VAC as your source. The type of analysis you need to set up is AC Sweep. Check logarithmic in AC Sweep type and select Decade. Use 1, 1000 and 10 for Start frequency, End frequency and Points/Decade, respectively. Run the simulation. Now we are interested in plotting the output to input ratio (i.e., the transfer function of the circuit). Select Trace/Add Trace from the Trace menu, select V (C1:2) then from the right window select / and finally select V (V1 :+). Use the cursor to find the point where the y-axis value is $1/\sqrt{2}$ (or –3dB). Mark that point and now using Plot/Label/Line, Plot/Label/Arrow and Plot/Label/Text mark the limits of the region from 1Hz to the point you found, something like this |← BW →|. This is the –3dB bandwidth of your circuit.

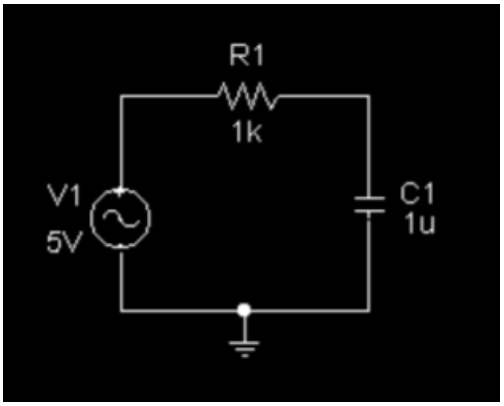


Figure 15: [11] AC circuit to run the AC sweep Analysis.

3.6 Parametric Sweep

In the schematics of Figure, replace the DC voltage source V1 by a 0V-120V square wave. You may specify a period of 10ns, a 50% duty cycle and a 1ns rise time and fall time for the square wave. Our goal is to find the values of R2 such that the current in R1 is 1A when V1 is 0V and 120V, respectively. First we need to define the sweep parameter, in this case it is the value of R2, so double-click on the value and change it to something like {Var} where Var can be any name. Now from the library Special, get a part named Param and place it on the schematics and double-click on it so you can edit its properties. Click on the New Column and type the name Var without the {}, then input the Value 50 and finally click OK. Now select the column Var and select Display, a new window called Display

Properties will appear, click on Name and Value then Ok. Close the properties window. Set up a transient simulation from 0 to 100ns with a step size of 0.1ns. Once you are in the setup window check the parametric sweep option and select Global Parameter, type Var as the name and then select linear and type 10, 20 and 1 for the start value, end value and increment, respectively. Perform the simulation.

4. SIMULATION AND ANALYSIS

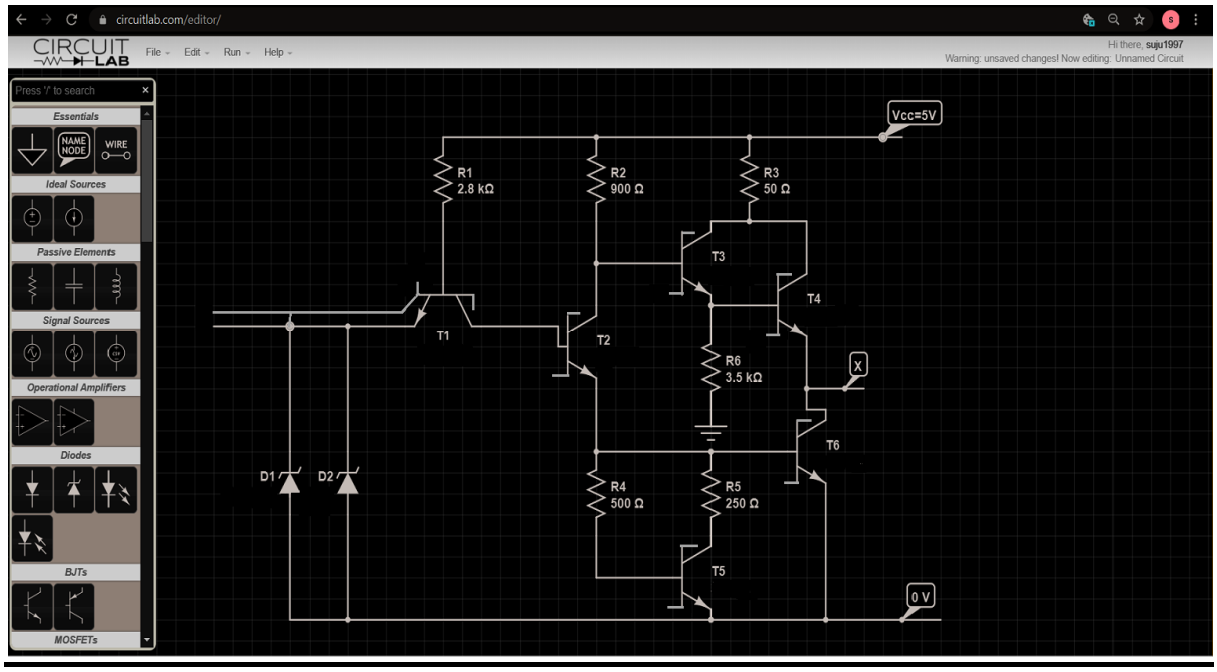


Figure 16: Circuit Diagram of Schottky Barrier Transistor

CONCLUSION

The novel devices which use these TMDC materials are generally based on a FET structure. The FET dimensions and electrostatics do need to be scaled up to maximize many of the advantages of 2D materials. The Al_2O_3/Pt / TiN / Si substratum provided in this work can serve as a platform for the investigation of these tools. It provides an enhanced 22 nm EOT which is not easily accomplished with thermally grown SiO_2.The MoS_2 contact resistances extracted are also lower than those reported on SiO_2 ; indicating that this new gate stacks might be advantageous for studying TMDC contacts. Using a Pt gate electrode could enable patterned back gates and integration on other substrates. The memristive characteristics of the Al_2O_3/Si capacitors and FETs may also have applications in devices for neuromorphic computing.

TMDC FETs on Al_2O_3/Pt/TiN/Si show prominent contact effects of both a constant and gate voltage dependent contact resistance in back-gated FETs. It is widely recognized that the FET transconductance can be reduced by a great contact resistance. The mobility extracted from the transconductance will therefore be lower than the value taken from other methods. However, as seen prominently on Al_2O_3/Pt / TiN / Si FETs in the MoS_2, the contact resistance depending on the gate voltage will yield a much greater transconductance than if the contact resistance were constant. The consequence of this turn-on touch is a drastic overestimation of mobility for field effects.

Ballistic transport simulations at Landauer expect a slight increase in the 50 meV sub threshold slope. However, the enhanced SS comes at a wide system area and expense of capacitance. This also means that basic problems like the removal of the dead layer of the piezoelectric interfaces are solved. Such problems were verified by the experimental making of a 2D-SFET. In the fabricated unit the maximum expected bandgap shift was < 50 meV. While strain was measured in-situ using Raman spectroscopy, no strain was detectable out of plane.

This work employed multilayer TMDC flakes resulting from bulk crystal mechanical exfoliation. But in their monolayer shape, these materials have very different properties. Compared to their multilayer form of indirect bandgap, the monolayers have a larger and more direct bandgap. Therefore they are advantageous for many optoelectronic applications or those requiring a semi-conductor of sub-nm thickness. The process of electro-ablation (EA) studied in this work allows the monolayer's MoS_2,WS_2 and $MoSe_2$ to be obtained from

bulk flakes after an electrochemical thinning process. Compared to high temperature, higher cost, and complex growth methods such as CVD, the EA process offers a more cost efficient and faster route to acquire these materials.

FUTURE WORK

There are still many unanswered questions concerning contacts with TMDC FETs that require a comprehensive understanding of the FET characteristics first. The virtual source model of contact gating presented in this work is an import step towards understanding how the FET characteristics of the contact effects manifest. However, the effect of various metals and substrates on the contact threshold voltage and the band movement under the contact is still unknown. Contact metals as well as the degree to which they react with the TMDC differ in their role at work.

By adopting a pyramid-type structure, the stress produced in the 2D-SFET has been shown to be significantly improved. Other types of structures should be investigated, such as the vertical nanowire core and shell structure shown in Figure 17. The 2D tube, dielectric gate, gate electrode, piezoelectric, and back electrode are deposited around a steep cylindrical core in this structure, as shown in Figure 17(b). This structure may provide an improvement in the strain transfer coefficient which is 0.2 in the pyramid structure. Ideal transfer of 1 strain would offer an improvement of 5X. Likewise, this structure can result in a lower parameter than a pyramid structure would achieve. Vertical FET structures are advantageous, as the length of the channel does not affect the area of the device. But the thickness of the PE relates to the application area for a vertical 2D-SFET.

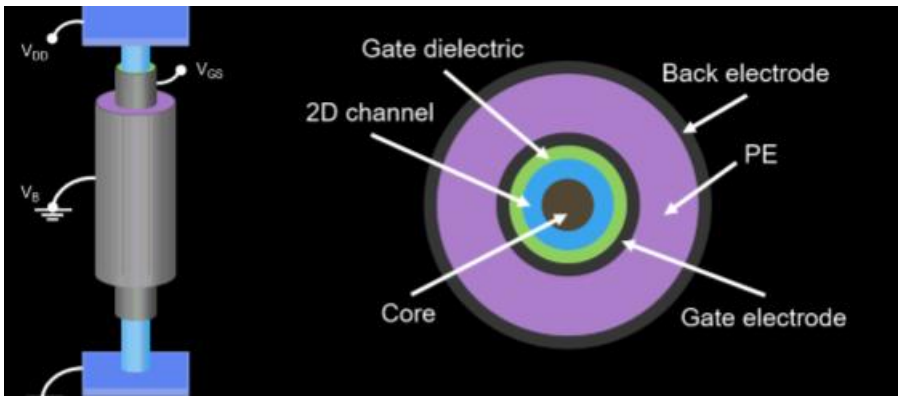


Figure 17: [12] Vertical nanowire SFET. a) Possible vertical SFET structure. b) Cross section showing a solid cylindrical core with the gate, 2D channel, gate dielectric, and piezoelectric (PE) and back electrode wrapped around the core.

REFERENCES

1. https://www.researchgate.net/publication/323685728_Special_Diodes/figures?lo
2. https://www.electrical4u.com/schottky-diode
3. Liu, Jingxia, et al. "Ultrasensitive Monolayer MoS2 Field-Effect Transistor Based DNA Sensors for Screening of Down Syndrome." *Nano letters* 19.3 (2019): 1437-1444.
4. Wang, Zegao, et al. "The ambipolar transport behavior of WSe 2 transistors and its analogue circuits." *NPG Asia Materials* 10.8 (2018): 703-712.
5. Prakash, Abhijith, and Joerg Appenzeller. "Bandgap extraction and device analysis of ionic liquid gated WSe2 Schottky barrier transistors." *Acs Nano* 11.2 (2017): 1626-1632.
6. Prakash, Abhijith, and Joerg Appenzeller. "Bandgap extraction and device analysis of ionic liquid gated WSe2 Schottky barrier transistors." *Acs Nano* 11.2 (2017): 1626-1632.
7. Das, Saptarshi, Madan Dubey, and Andreas Roelofs. "High gain, low noise, fully complementary logic inverter based on bi-layer WSe2 field effect transistors." *Applied Physics Letters* 105.8 (2014): 083511.
8. Ilatikhameneh, Hesameddin, et al. "Tunnel field-effect transistors in 2-D transition metal dichalcogenide materials." *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits* 1 (2015): 12-18.
9. Knoch, Joachim, et al. "Physics of ultrathin-body silicon-on-insulator Schottky-barrier field-effect transistors." *Applied Physics A* 87.3 (2007): 351-357.
10. Liu, Han, et al. "Switching mechanism in single-layer molybdenum disulfide transistors: An insight into current flow across Schottky barriers." *ACS nano* 8.1 (2014): 1031-1038.
11. https://personal.utdallas.edu/~yxc101000/courses/3111Lab/handouts/Lab%201.pdf
12. Schulman, Daniel Scott. "Contact, Interface, and Strain Engineering of Two-Dimensional Transition Metal Dichalcogenide Field Effect Transistors." (2019).
13. Penumatcha, Ashish V., Ramon B. Salazar, and Joerg Appenzeller. "Analysing black phosphorus transistors using an analytic Schottky barrier MOSFET model." *Nature communications* 6.1 (2015): 1-9.