ALGORITHMS FOR VLSI PHYSICAL DESIGN AUTOMATION

Second Edition

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Intel Corporation

SPRINGER SCIENCE+BUSINESS MEDIA, LLC

ISBN 978-1-4613-5997-5 ISBN 978-1-4615-2351-2 (eBook)
DOI 10.1007/978-1-4615-2351-2

Library of Congress Cataloging-in-Publication Data

A C.I.P. Catalogue record for this book is available
from the Library of Congress.

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Originally published by Kluwer Academic Publishers in 1995
Softcover reprint of the hardcover 2nd edition 1995
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Printed on acid-free paper.

To my parents
Akhter and Akram Sherwani

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Foreword

Since the invention of integrated circuits thirty years ago, manufacturing of electronic systems has taken rapid strides in improvement in speed, size, and cost. For today's integrated circuit chips, switching time is on the order of nanoseconds, minimum feature size is on the order of sub-microns, transistor count is on the order of millions, and cost is on the order of a few dollars. In fact, it was estimated that the performance/cost ratio of integrated circuit chips has been increasing at the rate of one thousand-fold every ten years, yielding a total of 10^9 for the last three decades. A combination of high product performance and low per-unit cost leads to the very pervasive introduction of integrated circuit chips to many aspects of modern engineering and scientific endeavors including computations, telecommunications, aeronautics, genetics, bioengineering, manufacturing, factory automation, and so on. It is clear that the integrated circuit chip will play the role of a key building block in the *information society* of the twenty-first century.

The manufacture of integrated circuit chips is similar to the manufacture of other highly sophisticated engineering products in many ways. The three major steps are *designing* the product, *fabricating* the product, and *testing* the fabricated product. In the design step, a large number of components are to be designed or selected, specifications on how these components should be assembled are to be made, and verification steps are to be carried out to assure the correctness of the design. In the manufacturing step, a great deal of manpower, and a large collection of expensive equipment, together with painstaking care are needed to assemble the product according to the design specification. Finally, the fabricated product must be tested to check its physical functionality. As in all engineering problems, there are conflicting requirements in all these steps. In the design step, we want to obtain an optimal product design, and yet we also want the design cycle to be short. In the fabrication step, we want the product yield to be high, and yet we also need to be able to produce a large volume of the product and get them to market in time. In the testing step, we want the product to be tested thoroughly and yet we also want to be able to do so quickly.

The title of this book reveals how the issue of enormous design complexity is to be handled so that high quality designs can be obtained in a reasonable amount of design time: We use muscles (*automation*) and we use brain

(*algorithms*). Professor Sherwani has written an excellent book to introduce students in computer science and electrical engineering as well as CAD engineers to the subject of physical design of VLSI circuits. Physical design is a key step in the design process. Research and development efforts in the last twenty years have led us to some very good understanding on many of the important problems in physical design. Professor Sherwani's book provides a timely, up-to-date integration of the results in the field and will be most useful both as a graduate level textbook and as a reference for professionals in the field. All aspects of the physical design process are covered in a meticulous and comprehensive manner. The treatment is enlightening and enticing. Furthermore, topics related to some of the latest technology developments such as Field Programmable Gate Arrays (FPGA) and Multi-Chip Modules (MCM) are also included. A strong emphasis is placed on the algorithmic aspect of the design process. Algorithms are presented in an intuitive manner without the obscurity of unnecessary formalism. Both theoretical and practical aspects of algorithmic design are stressed. Neither the elegance of optimal algorithms nor the usefulness of heuristic algorithms are overlooked. ¿From a pedagogical point of view, the chapters on electronic devices and on data structures and basic algorithms provide useful background material for students from computer science, computer engineering, and electrical engineering. The many exercises included in the book are also most helpful teaching aids.

This is a book on physical design algorithms. Yet, this is a book that goes beyond physical design algorithms. There are other important design steps of which our understanding is still quite limited. Furthermore, development of new materials, devices, and technologies will unquestionably create new problems and new avenues of research and development in the design process. An algorithmic outlook on design problem and the algorithmic techniques for solving complex design problems, which a reader learns through the examples drawn from physical design in this book, will transcend the confine of physical design and will undoubtedly prepare the reader for many of the activities in the field of computer-aided design of VLSI circuits. I expect to hear from many students and CAD professionals in the years to come that they have learned a great deal about physical design, computer-aided design, and scientific research from Professor Sherwani's book. I also expect to hear from many of them that Professor Sherwani's book is a source of information as well as a source of inspiration.

Urbana-Champaign C. L. Liu

Preface

From its humble beginning in the early 50's to the manufacture of circuits with millions of components today, VLSI design has brought the power of a mainframe computer to a laptop. Of course, this tremendous growth in the area of VLSI design is made possible by the development of sophisticated design tools and software. To deal with the complexity of millions of components and to achieve a turn around time in terms of a couple of months, VLSI design tools must not only be computationally fast but also perform close to optimal.

The future growth of VLSI systems depends critically on the research and development of Physical Design Automation tools. In the last two decades, the research in physical design automation has been very intense, and literally thousands of research articles covering all phases of physical design automation have been published. The development of VLSI physical design automation also depends on availability of trained manpower. We have two types of students studying VLSI physical design: students preparing for a research career and students preparing for a career in industry. Both types of students need to build a solid background. However, currently we lack courses and text books which give students a comprehensive background. It is common to find students doing research in placement, but are unaware of the latest developments in compaction. Those students seeking careers in industry will find that the VLSI physical design industry is a very fast paced industry. They are expected to be conversant with existing tools and algorithms for all the stages of the design cycle of a VLSI chip. In industry, it is usual to find CAD engineers who work on one aspect of physical design and lack knowledge of other aspects. For example, a CAD engineer working in the development of detailed routers may not be knowledgeable about partitioning algorithms. This is again due to the lack of comprehensive textbooks which cover background material in all aspects of VLSI physical design.

Providing a comprehensive background in one textbook in VLSI physical design is indeed difficult. This is due to the fact that physical design automation requires a mix of backgrounds. Some electrical engineering and a solid undergraduate computer science background is necessary to grasp the fundamentals. In addition, some background in graph theory and combinatorics is also needed, since many of the algorithms are graph theoretic or use other combinatorial optimization techniques. This mix of backgrounds has perhaps

restricted the development of courses and textbooks in this very area.

This book is an attempt to provide a comprehensive background in the principles and algorithms of VLSI physical design. The goal of this book is to serve as a basis for the development of introductory level graduate courses in VLSI physical design automation. It is hoped that the book provides self contained material for teaching and learning algorithms of physical design. All algorithms which are considered basic have been included. The algorithms are presented in an intuitive manner, so that the reader can concentrate on the basic idea of the algorithms. Yet, at the same time, enough detail is provided so that readers can actually implement the algorithms given in the text and use them.

This book grew out of a graduate level class in VLSI physical design automation at Western Michigan University. Initially written as a set of class notes, the book took form as it was refined over a period of three years.

Overview of the Book

This book covers all aspects of Physical Design. The first three chapters, provide the background material, while the focus of each chapter of the rest of the book is on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have also been included.

In Chapter 1, we give an overview of the VLSI physical design automation field. Topics include the VLSI design cycle, physical design cycle, design styles and packaging styles. The chapter concludes with a brief historical review of the field.

Chapter 2 discusses the fabrication process for VLSI devices. It is important to understand the fabrication technology in order to correctly formulate the problems. In addition, it is important for one to understand, what is doable and what is not! Chapter 2 presents fundamentals of MOS and TTL transistors. It then describes simple NAND and NOR gates in nMOS and CMOS. Finally, we discuss several other factors such as design rules, yield, delay, and fabrication costs involved in the VLSI process.

Basic material on data structures and algorithms involved in the physical design is presented in Chapter 3. Several different data structures for layout have been discussed. Graphs which are used to model several different problems in VLSI design are defined and basic algorithms for these graphs are presented.

Chapter 4 deals with partitioning algorithms. An attempt has been made to explain all the possible factors that must be considered in partitioning the VLSI circuits. Group migration, simulated annealing and simulated evolution algorithms have been presented in detail. The issue of performance driven partitioning is also discussed.

Placement and floorplanning are key steps in physical design. In Chapter 5, we discuss basic algorithms on placement, floorplanning and pin assignment. Several different techniques for placement such as, simulated annealing, simulated evolution, and force-directed are discussed.

Chapter 6 deals with global routing. It covers from simple routing algorithms, such as, maze routing to more advanced integer programming based methods. It also discusses Steiner tree algorithms for routing of multi-terminal nets.

Chapter 7 is the longest chapter in the book and represents the depth of knowledge that has been gained in the detailed routing area in the last decade. Algorithms are classified according to the number of layers allowed for routing. In single layer routing, we discuss general river routing and the single row routing problem. All major two-layer channel and switch box routers are also presented. The chapter also discusses three-layer and multilayer routing algorithms.

Chapter 8 discusses two ways of improving layouts after detailed routing, namely, via minimization and over-the-cell routing. Basic algorithms for via minimization are presented. Over-the-cell routing is a relatively new technique for reducing routing areas. We present two latest algorithms for over-the-cell routing.

The problems of routing clock and power/ground nets are discussed in Chapter 9. These topics play a key role in determining the layout of high performance systems. Circuit compaction is discussed in Chapter 10. One dimensional compaction, as well as two dimensional compaction algorithms are presented.

Field Programmable Gate Arrays (FPGAs) are rapidly gaining ground in many applications, such as, system prototyping. In Chapter 11, we discuss physical design automation problems and algorithms for FPGAs. In particular, we discuss the partitioning and routing problems in FPGAs. Both of these problems are significantly different from problems in VLSI. Many aspects of physical design of FPGAs remain a topic of current research.

Multi-Chip Modules (MCMs) are replacing conventional printed circuit boards in many applications. MCMs promise high performance systems at a lower cost. In Chapter 12, we explore the physical design issues in MCMs. In particular, the routing problem of MCMs is a true three dimensional problem. MCMs are currently a topic of intense research.

At the end of each chapter, a list of exercises is provided, which range in complexity from simple to research level. Unmarked problems and algorithms are the simplest. The exercises marked with (†) are harder and algorithms in these exercises may take a significant effort to implement. The exercises and algorithms marked with (‡) are the hardest. In fact, some of these problems are research problems.

Bibliographic notes can be found at the end of each chapter. In these notes, we give pointers to the readers for advanced topics. An extensive bibliography is presented at the end of the text. This bibliography is complete, to the best of our knowledge, up to the summer of 1992. An attempt has been made to include all papers which are appropriate for the targeted readers of this text. The readers may also find the author and the subject index at the back of the text. The author index provides references to all significantly discussed work of an author.

Overiew of the Second Edition

In 1992, when this book was orginally published, the largest microprocessor had one million transistors and fabrication process had three metal layers. We have now moved into a six metal layer process and 15 million transistor microprocessors are already in advanced stages of design. The designs are moving towards a 500 to 700 Mhz frequency goal. This challenging frequency goal, as well as, the additional metal layers have significantly altered the VLSI field. Many issues such as three dimensional routing, Over-the-Cell routing, early floorplanning have now taken a central place in the microprocessor physical design flow. This changes in the VLSI design prompted us to reflect these in the book. That gave birth to the idea of the second edition.

The basic purpose of the second edition is to introduce a more *realistic* picture to the reader exposing the concerns facing the VLSI industry while maintaining the theoretical flavor of the book. New material has been added to all the chapters. Several new sections have been added to many chapters. Few chapters have been completely rewritten. New figures have been added to supplement the new material and clarify the existing material.

Chapter 1 has been rewritten. New sections have been added about new trends in VLSI design cycle as well as physical design. New material has been added about verification and timing aspects of the design. Chapter 2 has been enchanced with a discussion of DRAM and SRAM cells. Several new algorithms have been added in

In Chapter 3, more examples have been added to improve presentation. Chapters 4 and 5 have been rewritten for clarity. Chapter 6 has been rewritten to provide a perspective on the three dimensional routing environment. Chapter 8 has been re-arranged for better presentation and new material has been added on OTC routing.

Chapter 9 now includes some more discussion on clock buffers, power and ground routing. Chapter 10 has been upgraded to include more discussion on constraints. Chapter 11 and 12 have been edited for clarity. We have made an attempt to update the bibliography and many new items have been added.

In summary, I have made an attempt to capture the physical design flow used in the industry and present it in the second addition. I hope that readers will find that information both useful and interesting.

To the Teacher

This book has been written for introductory level graduate students. It presents concepts and algorithms in an intuitive manner. Each chapter contains 3 to 4 algorithms that have been discussed in detail. This has been done so as to assist students in implementing the algorithms. Other algorithms have been presented in a somewhat shorter format. References to advanced algorithms have been presented at the end of each chapter. Effort has been made to make the book self contained.

This book has been developed for a one-semester or a two-semester course in VLSI physical design automation. In a one-semester course, it is recommended that chapters 8, 9, 11, and 12 be omitted. A half-semester algorithm development project is highly recommended. Implementation of algorithms is an important tool in making students understand algorithms. In physical design, the majority of the algorithms are heuristic in nature and testing of these algorithms on benchmarks should be stressed. In addition, the development of practical algorithms must be stressed, that is, students must be very aware of the complexity of the algorithms. An optimal $O(n^3)$ algorithm may be impractical for an input of size 10 million. Several (†) marked problems at the end of each chapter may serve as mini-projects.

In a two-semester class, it is recommended that all the chapters be included. Reading state-of-art papers must be an integral part of this class. In particular, students may be assigned papers from proceedings of DAC and ICCAD or from IEEE Transactions on CAD. Papers from Transactions typically require a little more mathematical maturity than the papers in DAC and ICCAD. An important part of this class should be a two-semester project, which may be the development of a new algorithm for some problem in physical design. A typical first part of the project may involve modifying an existing algorithm for a special application. Some (‡) problems may serve as projects.

In both the courses, a good background in hand layout is critical. It is expected that students will have access to a layout editor, such as MAGIC or LEDIT. It is very important that students actually layout a few small circuits. For examples see exercises at the end of Chapter 2.

For faculty members, a teaching aid package, consisting of a set of 400 overheads (foils) is available from the author. These are quite helpful in teaching the class, as all the important points have been summarized on section by section basis. In order to obtain these foils, please send an email (or a mail) to the author, at the address below.

To the Student

First and foremost, I hope that you will enjoy reading this book. Every effort has been made to make this book easy to read. The algorithms have been explained in an intuitive manner. The idea is to get you to develop new algorithms at the end of the semester. The book has been balanced to give a practical as well as a theoretical background. In that sense, you will find it useful, if you are thinking about a career in industry or if you are thinking about physical design as a possible graduate research topic.

What do you need to start reading this book ? Some maturity in general algorithm techniques and data structures is assumed. Some electrical engineering background and mathematics background will be helpful, although not necessary. The book is self-contained to a great extent and does not need any supporting text or reference text.

If you are considering a career in this field, I have one important advise for you. Research in this field moves very fast. As a result, no textbook can replace

state-of-the-art papers. It is recommended that you read papers to keep you abreast of latest developments. A list of conference proceedings and journals appears in the bibliographic notes of Chapter 1. I also recommend attending DAC and ICCAD conferences every year and a membership in ACM/SIGDA, IEEE/DATC and IEEE/TC-VLSI.

To the CAD Professional

This book provides a detailed description of all aspects of physical design and I hope you have picked up this book to review your basics of physical design. While it concentrates on basic algorithms, pointers are given to advanced algorithms as well. The text has been written with a balance of theory and practice in mind. You will also find the extensive bibliography useful for finding advanced material on a topic.

Errors and Omissions

No book is free of errors and omissions. Despite our best attempt, this text may contain some errors. If you find any errors or have any constructive suggestions, I would appreciate receiving your comments and suggestions. In particular, new exercises would certainly be very helpful. You can mail your comments to:

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or email them to `sherwani@ichips.intel.com`.

A concentrated effort has been made to include all pertinent references to papers and books that we could find. If you find omissions in the book, please feel free to remind me.

This book was typeset in Latex. Figures were made using 'xfig' and inserted directly into the text as ps files using 'transfig'. The bibliography was generated using Bibtex and the index was generated by a program written by Siddharth Bhingarde.

Portland, March, 1995 Naveed A. Sherwani

Acknowledgments

No book is a product of one person. The same is true for this book. The first edition of this book was completed in 1992 at Western Michigan University (WMU), with the help of a dedicated group of students, popularly known as the *Nitegroup*. I must thank all members of the nitegroup, who worked tirelessly for days and nights (mostly nights) for the final six months. Siddharth Bhingarde, Surendra Burman, Moazzem Hossain, Chandar Kamalanathan, Wasim Khan, Arun Shanbhag, Timothy Strunk and Qiong Yu played key roles. Thanks are also to due to senior nitegroup members, in particular Roshan Gidwani, Jahangir Hashmi, Nancy Holmes, and Bo Wu. Special thanks are due to the youngest member of nitegroup, Timothy Strunk, who made (almost) all the figures in the text and brought enthusiasm to the team. Thanks are also due to Anand Panyam, Konduru Nagesh and Aizaz Manzar for helping in the final stages of the first edition. Many students in my class CS520 (Introduction to VLSI design automation) suffered through earlier version of this book, and I would like to thank them for their constructive suggestions.

Several colleagues and friends contributed significantly by reviewing several chapters and using parts of the first edition in their courses. In this regard, I would like to thank Jeff Banker, Ajay Gupta, Mark Kerstetter, Sartaj Sahni, and Jason Cong. I would also like to especially thank Dinesh Mehta and Si-Qing Zheng. I wish to express my sincere thanks to Malgorzata Marek-Sadowska, who made very critical remarks and contributions to the improvement in the quality of the first edition.

The second edition was written at Intel and several of my colleagues at Intel helped as reviewers. In this regard, I thank Marc Rose, John Hansen, Dave Ackley, Mike Farabee, and Niraj Bindal. Several colleagues from the universities sent suggestions for improvement. In particular, Malgorzata Chrzanowska-Jeske and Dinesh Bhatia provided constructive suggestions.

Thanks are due to two special people, who have contributed very generously in my career and helped in many ways. I would like to thank Vishwani Agrawal and C. L. Liu for their constant encouragement and sound words of advise.

The second edition would not have been possible without the help of Siddharth Bhingarde, Aman Sureka, Rameshwar Donakanti and Anand Panyam. In particular, Siddharth worked with me for many many nights on this project. I am very grateful to these individuals for their help. Thanks are also due to

Srinivasa Danda and Sreekrishna Madhwapathy for their help.

I would like to thank several different organizations who have contributed directly. First, I would like to thank Ken Wan, Roshan Gidwani and the rest of the CTS group at Advanced Micro Devices for helping with many technical details. I thank ACM SIGDA for supporting my research for several years and thus helping me write the first edition. Thanks are also due to Western Michigan University (WMU), and in particular Donald Nelson and Douglas Ferraro, who, despite all costs, made the necessary facilities available to complete the first edition. The National Science Foundation, in particular Bob Grafton, deserves thanks for supporting my VLSI laboratory and research at WMU. I would also like to thank Reza Rashidi and the staff of FRC laboratory for their help in printing the text and cover design. I must also thank WMU Computer Science department secretaries Phyllis Wolf and Sue Moorian for being very helpful during all stages of the first edition. I would like to thank Intel Corporation for helping me with the second edition. In particular, I would like to thank Atiq Bajwa for making the time available for me to complete the project.

I must thank my copy editor Frank Strunk, who very carefully read the manuscript of the first edition in the short time we gave him. Several friends and family members helped by being copy editors of the second edition. Sabahat Naveed, Shazia Asif and Akram Sherwani helped by editing many revisions. Internet played a key role, as many of these revisions were done in Pakistan and then emailed to me.

Thanks are also due to Carl Harris, editor at Kluwer Academic Publishers for being understanding and going beyond his call of duty to help out with my requests. Carl is instrumental is starting and pushing the second edition. He was very patient as I missed some deadlines.

Finally, I wish to thank my parents and my siblings for supporting me throughout my life and for being there when I needed them. Lastly and most importantly, I am very thankful to my wife Sabahat Naveed for her encouragement and support. All of my family suffered as I neglected many social responsibilities to complete this book.

Portland, March, 1995 Naveed A. Sherwani

Acknowledgments for the Second Edition

The second edition project would not have been possible without the help of Siddharth Bhingarde, Aman Sureka, Rameshwar Donakanti and Anand Panyam. In particular, Siddharth worked with me for many many nights on this project. I am very grateful to these individuals for their help.

Several of my colleagues at Intel helped as reviewers of the chapters. In this regard, I would like to thank Marc Rose, John Hansen, Dave Ackley, Mike Farabee, and Niraj Bindal.

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