

## 2. Pipelining & Registers

Allow several instructions to be processed simultaneously without having to wait for the previous instructions to be completed

1. Instruction Fetch cycle (IF)
2. Instruction Decode cycle (ID)
3. Operand Fetch cycle (OF)
4. Instruction Execution cycle (IE)
5. Writeback Result process (WB)

### Explain what is meant by pipelining:

- Pipelining is instruction level parallelism
- Execution of an instruction is split into a number of stages
- When the first stage for an instruction is completed, the first stage of next instruction can start executing
- Another instruction can start executing before the previous one is finished
- Processing a number of instructions can be concurrent/simultaneous

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		Clock cycles									
		1	2	3	4	5	6	7	8	9	10
Processor stages	IF	A	B	C	D	E	F				
	ID		A	B	C	D	E	F			
	OF			A	B	C	D	E	F		
	IE				A	B	C	D	E	F	
	WB					A	B	C	D	E	F

Figure 15.1

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