Section 15.2 - Boolean Algebra and Logic Circuits

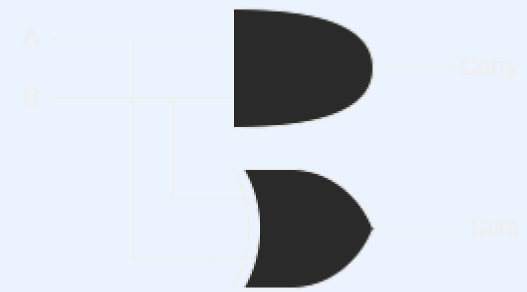
Layer 1: Logic Gates

Syllabus Content Section 15: Hardware and Virtual Machines

S15.2.1 Produce truth tables for logic circuits including half adders and full adders

- May include logic gates with more than two inputs.

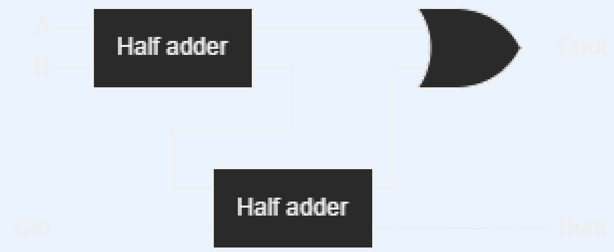
Half Adder



Truth Table:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder



Truth Table:

A	B	Cin	Sum	Cout

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S15.2.2 Show understanding of a flip-flop (SR, JK)

- Draw a logic circuit and derive a truth table for a flip-flop
- Understand of the role of flip-flops as data storage elements

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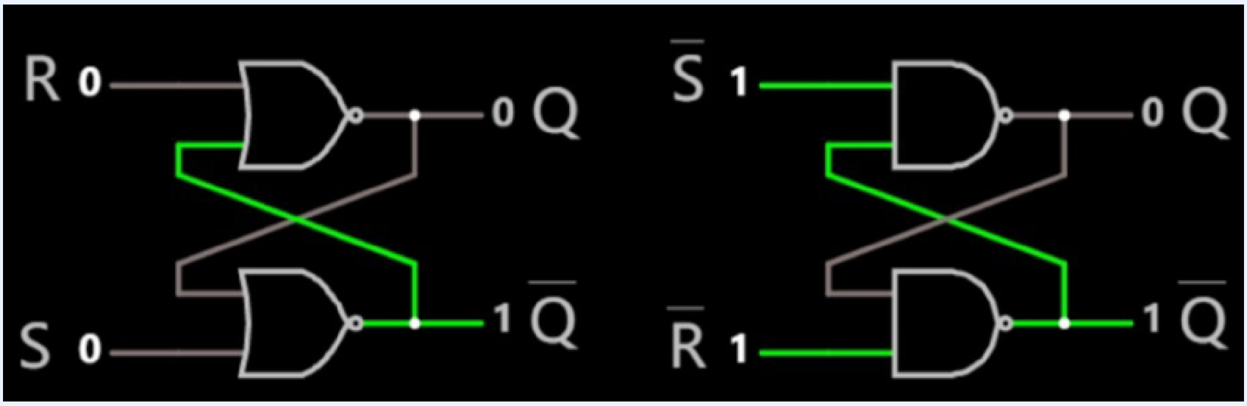
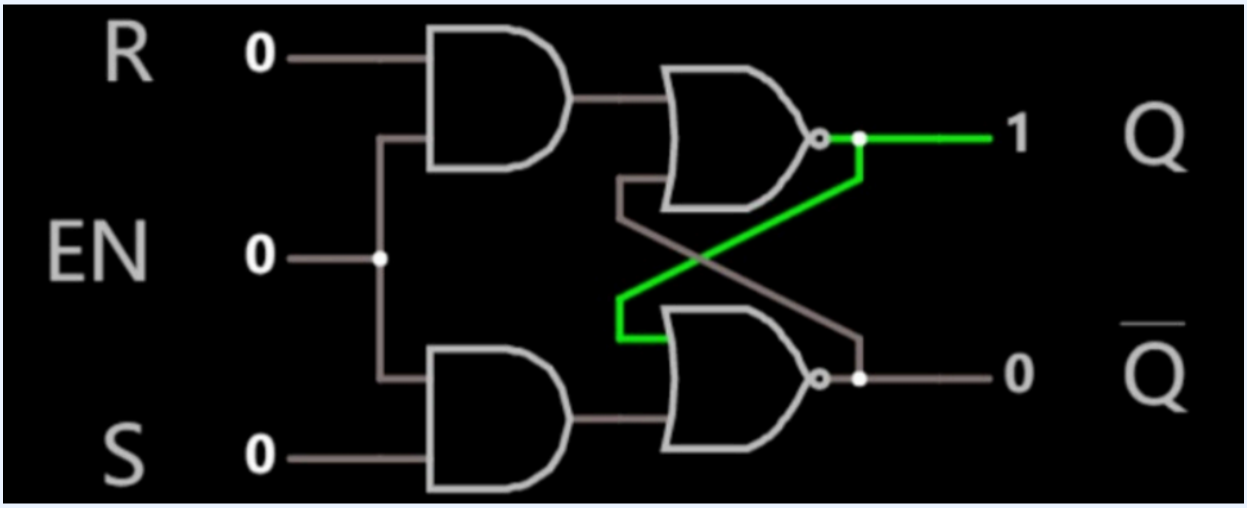
SR Latch

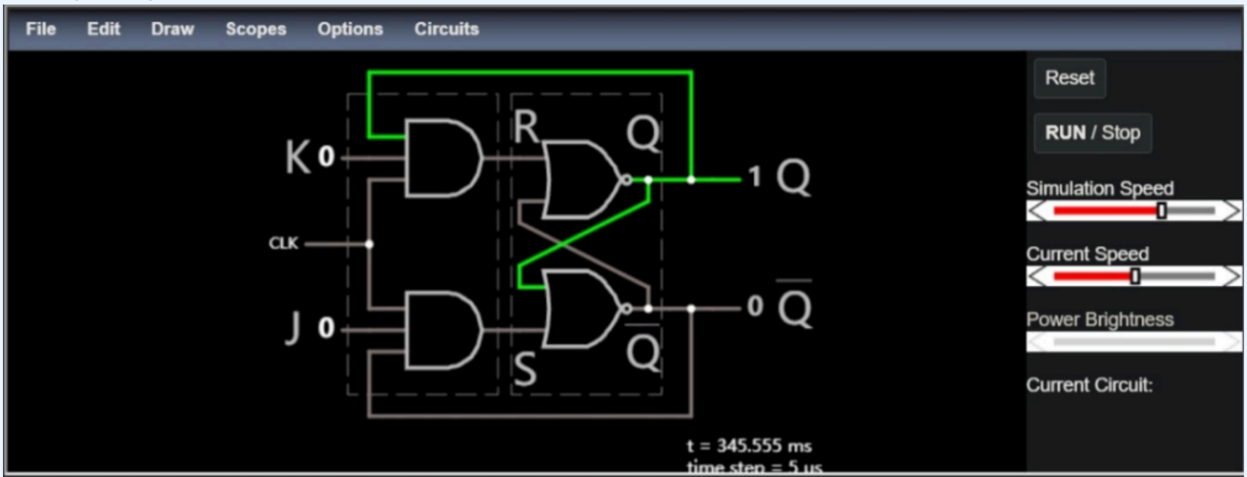




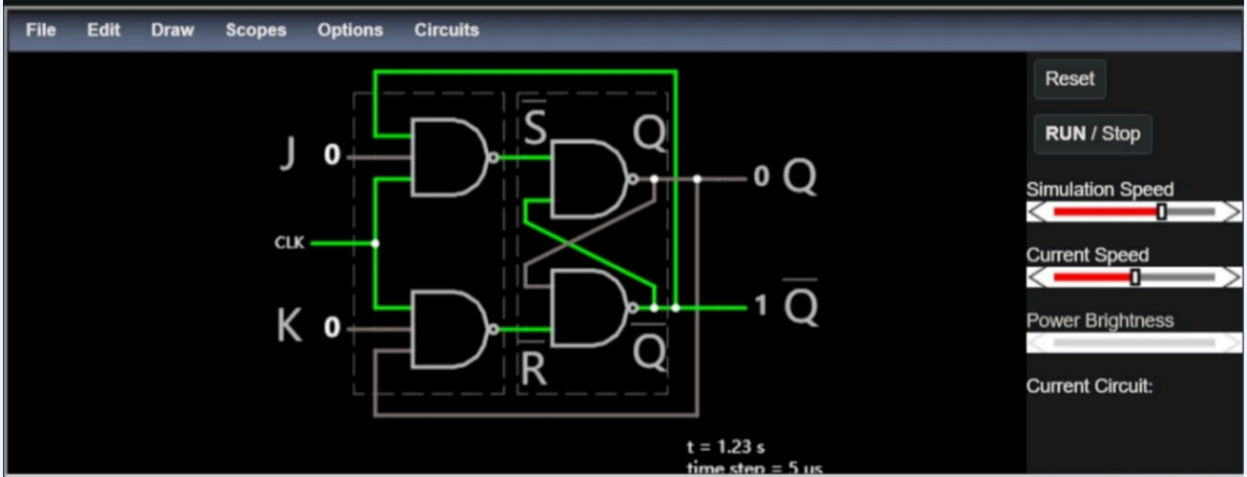
Characteristic Table

S(t)	R(t)	Q(t)	Q(t+1)	Condition
0	0	0	0	No Change
0	0	1	1	No Change
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	1	Set
1	0	1	1	Set
1	1	0	-	Not Defined
1	1	1	-	Not Defined

JK Flip-Flop



Active-HIGH SR Latch Constructed JK Filp-Flop



Active-LOW SR Latch Constructed JK Filp-Flop

Characteristic Table

S(t)	R(t)	Q(t)	Q(t+1)	Condition
0	0	0	0	No Change
0	0	1	1	No Change

S(t)	R(t)	Q(t)	Q(t+1)	Condition
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	1	Set
1	0	1	1	Set
1	1	0	1	Toggle
1	1	1	0	Toggle

S15.2.3 Show understanding of Boolean algebra

- Understand De Morgan's laws.
- Perform Boolean algebra using De Morgan's laws.
- Simplify a logic circuit/expression using Boolean algebra

Unit Property	$x + \overline{x} = 1$
Zero Property	$x\overline{x} = 0$
Double Complement	$\overline{\overline{x}} = x$
Idempotent Laws	$x + x = x$ $x \cdot x = x$
Identity Laws	$x + 0 = x$ $x \cdot 1 = x$
Domination Laws	$x + 1 = 1$ $x \cdot 0 = 0$
Commutative laws	$x + y = y + x$ $x \cdot y = y \cdot x$
Associative laws	$x + (y + z) = (x + y) + z$ $x \cdot (y \cdot z) = (x \cdot y) \cdot z$
Distributive laws	$x + (y \cdot z) = (x + y) \cdot (x + z)$ $x \cdot (y + z) = x \cdot y + x \cdot z$
Absorption laws	$x \cdot (x + y) = x \quad x + x \cdot y = x$ $x \cdot (\overline{x} + y) = x \cdot y \quad x + \overline{x} \cdot y = x + y$

Unit Property	$x + \overline{x} = 1$
Consensus Laws	$x \cdot y + \overline{x} \cdot z + y \cdot z = x \cdot y + \overline{x} \cdot z$ $(x + y) \cdot (\overline{x} + z) \cdot (y + z) = (x + y) \cdot (\overline{x} + z)$
De morgan's Law	$\overline{x \cdot y} = \overline{x} + \overline{y}$, $\overline{x + y} = \overline{x} \cdot \overline{y}$

S15.2.4 Show understanding of Karnaugh maps (K-map)

- Understand of the benefits of using Karnaugh maps Solve logic problems using Karnaugh maps

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3-VARIABLE KARNAUGH MAP

A \ BC	00	01	11	10
0	$\overline{A}\overline{B}\overline{C}$	$\overline{A}\overline{B}C$	$\overline{A}BC$	$\overline{A}B\overline{C}$
1	$A\overline{B}\overline{C}$	$A\overline{B}C$	ABC	$\overline{A}B\overline{C}$

4-VARIABLE KARNAUGH MAP

AB \ CD	00	01	11	10
00				
01				
11				
10				

5-VARIABLE KARNAUGH MAP

AB \ CDE	000	001	011	010	110	111	101	100
00								
01								
11								
10								

CELL ADJACENCY

AB \ CDE	000	001	011	010	110	111	101	100
00								
01		A						
11								
10								B

MAPPING A STANDARD SOP EXPRESSION

A \ BC	00	01	11	10
0	1	1		
1	1			1

$$\underset{000}{\bar{A}\bar{B}\bar{C}} + \underset{001}{\bar{A}\bar{B}C} + \underset{110}{AB\bar{C}} + \underset{100}{A\bar{B}\bar{C}}$$

MAPPING A NONSTANDARD SOP EXPRESSION

A \ BC	00	01	11	10
0	1	1		1
1	1	1	1	1

$$A + \bar{A}\bar{B} + \bar{A}B\bar{C}$$

A: 100, 101, 111, 110

$\bar{A}\bar{B}$: 000, 001

$\bar{A}B\bar{C}$: 010