Modelling and Control of WEDM Process for Cutting of Si-Ingots

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Abstract—Advancement in photovoltaics as an alternative energy medium is restricted due to the limitations in the manufacturing process of thin silicon wafers. Traditional abrasive methods lead to higher kerf (material) losses. Application of microdrilling process of Wire Electro Discharge Machining (WEDM) is a viable alternative to such traditional methods. However, WEDM is not as well established for cutting of semiconductors as it is for metals due to the lack of electrical characterization of metal-dielectric-semiconductor conduction. This work is directed towards the fabrication of the indigenous power supply unit for such unconventional load investigations. The pulsed power supply for this purpose is designed in this work. The state space model of this power supply is derived and controller is designed for this unit.

I. Introduction

Solar energy is a prominent source of renewable energy across the globe. India has aimed to reach for a 100 GW contribution from solar installations alone till 2022 [1]. Silicon is the most preferred material for manufacturing the photovoltaic (PV) panels. This manufacturing process is energy intensive and thereby very costly. Extracting ingots from raw silicon accounts for 20% of the total energy consumption throughout the process [2]. Hence, the initial cost of solar installation is higher. This can be reduced by finding better options for manufacturing silicon wafers.

Traditionally, the two popular methods for cutting of silicon are i) Wire loose slurry method and ii) Diamond saw cutting method. These methods, being abrasive in nature, lead to micro-fractures and cracks as deep as 20 μ m in the final product. Because of this, the wafer size gets limited to 180 μ m [3]. Also, about 50% of the ingot material is lost as kerf losses [4]. These methods have other disadvantages like contamination of the wafers due to the slurry, etc. [5].

WEDM is a non contact micro-drilling process which can be used to cut free form contours from large solid metal workpieces. Experiments have shown that kerf width can be reduced from 250 μm in abrasive saw cutting to 50 μm in WEDM resulting in net material saving of 200 - 300% [6]. This method presents a promising alternative for application to silicon wafer manufacturing. Hence, the long term goal of this project is to optimise the manufacturing process of silicon wafers. Although this process has been demonstrated for cutting of semiconductors and even ceramics [7], it is not as well established for these non conventional materials as it is for the metals.

One reason for this is the lack of electrical characterisation of metal-semiconductor-dielectric sparks. The experimentation done to investigate this has so far led to the conclusion that the spark gap VI characteristics of silicon are very different from that of the steel [8]. Hence, it is important to find a reliable model for spark gap in this setting. But, Levy and Maggi [9] demonstrated that the parameter settings given by the manufacturers are only applicable for the common steel grades.

Hence, the available machines are inadequate to carry out further experimentation as they provide discretely spaced setting ranges. An indigenously designed power supply along with a test setup is therefore required to carry out load investigations and optimise the process of Si-ingot cutting for PV applications.

This report summarizes the work done in design, modelling, and control of prototype power supply for Si-Ingot cutting by WEDM. The literature available in this regard is discussed in the first section, followed by the peak current mode control and direct duty ratio control procedures. In subsequent sections, the time averaging modelling methodology adopted for this purpose is discussed along with the practical considerations arising in such a design. The simulations carried out based on this work are found to be in agreement with the previous similar results for WEDM based cutting of steel.

II. LITERATURE SURVEY

A. WEDM Process

WEDM is a non-traditional material removal process in which a continuously travelling wire electrode made of thin tungsten, brass, or copper wire of diameter 0.05 to 0.3 mm is used. There is no direct contact between the work-piece and the wire. It is a through hole machining method capable to machine high strength and temperature resistance materials. Fig. 1 depicts the apparatus used for the experimentation hinted earlier, which mimics the arrangement in the actual WEDM machine.

In WEDM, the material is eroded from the workpiece by periodic sparks occurring between the work-piece and the wire separated by the dielectric. Electrical energy from a pulsating DC power supply operating in the frequency range 20 to 30 kHz is used to generate a channel of plasma between the cathode and the anode at temperatures ranging from 8000° to 12000°. Once turned off, the plasma channel breaks down, allowing the dielectric fluid to implore into the channel and flush away the molten particles and recover the dielectric strength of the gap. WEDM uses a thin wire continuously

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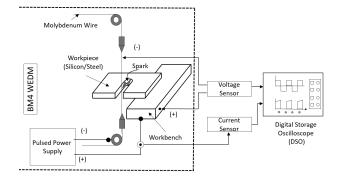


Fig. 1. Diagrammatic representation of WEDM

feeding through the work-piece to avoid wire breakage due to formation of localised hotspots.

In the final product, a taper [10] ranging from 15° for 100 mm thick to 30° for a 400 mm thick work-piece can be achieved. Typical Cutting Rates (CR) are 30 mm/min for 50 mm thick D2 tool steel and 750 mm/min for 150 mm thick aluminium.

B. Research Areas

WEDM is an extensive process with a large number of parameters like pulse duration, discharge frequency, discharge current, wire feed rate, etc., which in turn affect the output product in terms of surface roughness, cutting rates and material removal rates (MRR), etc. While a lot of literature is available for steel and other metals ranging from effects of process parameters on cutting to improve the MRR, CR and surface finish, this section is concerned with presenting the relevant material available on process modelling, monitoring and control.

- 1) Process Modelling: A theoretical model was developed by studying the influence of the work-piece material and pulse type properties of the WEDM of a work-piece with anodic property by Spur and Schönbeck [11] in 1993. Han et al. simulated the discharge phenomena of WEDM and developed a system which applies adaptive control to generate optimal machining condition for high precision in terms of the process parameters [12].
- 2) Fuzzy Control Systems: Fuzzy control systems have been a popular choice in this application because of independence from the requirement of comprehensive mathematical models. Kinoshita et al. investigated the effects of wire feed rate, wire winding speed, wire tension and electrical parameters on gap conditions during WEDM. Many control systems have been made based on these explicit mathematical and statistical models [13]. EDM pulses have been classified as open, spark, arc, off or, short on the basis of ignition delay [14]. Direct influence on the MRR and surface finish, electrode wear and accuracy of the final product dimensions has also been established.
- 3) Wire Breakage Avoidance: Kinoshita et al. observed that the rapid rise in the pulse frequency of the gap voltage before the wire breakage [15]. They developed a monitoring system that switches off the pulse generator and servo when

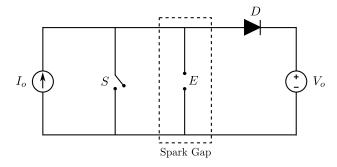


Fig. 2. Representative diagram of ideal WEDM power supply

such pulses arise thus preventing the wire from breaking. The increase in localised temperature due to a concentration of electrical discharges at certain points of wire leads to its breakage over time. An adaptive control system for detection of the spark location and reduction of discharge energy was developed [16].

- 4) Wire lag and wire vibration: Duaw and Beltrami [17] used an optical sensor for on-line monitoring the wire position and a controller for high speed. It has also been proposed to increase the gap distance to prevent wire gauging and breakage on high curvature areas of the work-piece [18] and many contour planning systems for WEDM apply this today. Several mathematical models have been derived from analysing the transient response of wire vibration based on the force acting on the tool [19].
- 5) Adaptive control systems: Much of the work uses adaptive control systems in this field for maintenance scheduling, machining variable height workpieces and predicting the thermal overload. Change in the work-piece thickness during machining leads to an increase in wire thermal density and breakage [15]. An adaptive control system was proposed with a multiple input model that monitors and controls sparking frequency according to on-line identified work-piece height by Rajurkar et al. [20]

III. POWER SUPPLY DESIGN

Power supply for the WEDM process delivers intermittent current and voltages across the electrode-dielectric-silicon ingot assembly. The pulsed nature of this power supply makes the design for such circuit difficult. This section describes the working of an ideal power source for the WEDM process of which the practical implementation is discussed in the subsequent sections.

A. Working Principle

Fig. 2 represents the functional configuration of a pulsed power supply in which an ideal current source I_o and ideal voltage source V_o are connected in parallel across the spark gap load E. The current and voltage waveforms across the load are shown in Fig. 3

I) t_0 to t_1 : During times $t=t_0$ and $t=t_1$, the current source causes the diode D to turn on and I_o flows through D to the ideal voltage source V_o . The voltage across the load terminals is V_o because D remains in a conduction state

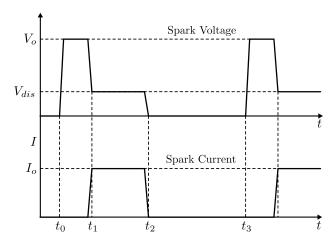


Fig. 3. Load voltage and current of WEDM power supply operation

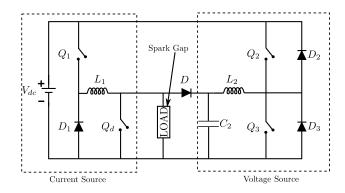


Fig. 4. Converter topology for WEDM power supply

from t_0 to t_1 . This application of voltage across the spark gap terminals causes the gap to break down at $t=t_1$. This breakdown delay time depends on the dielectric strength and the magnitude of the applied voltage.

- 2) t_1 to t_2 : Due to breakdown of dielectric, current I_o starts flowing through the spark gap E and the diode D turns off. If the spark gap is modelled as resistive, the voltage across terminals is V_{dis} and is equal to $I_o r_{gap}$. The silicon ingot now erodes along the length of moving wire electrode.
- 3) t_2 to t_3 : To increase the material removal rate, the spark is not allowed to become a sustained arc. This is achieved closing the switch S at time $t=t_2$. When S is closed, the current I_o flows through current source and switch and dielectric strength of the medium is recovered by flushing fresh dielectric over the gap.

When the gap is fully recovered, a new machining cycle is started at time $t=t_3$ by opening the switch S. The erosion takes place for about 10% of the entire machining period. Thus, the power is supplied to load only for this fraction of the machining period.

B. Converter Topology

This section describes the practical implementation of the ideal current and voltage sources depicted in Fig. 2. One realisation of such power supply is proposed by Tastekin et al. in [21] in which a single quadrant and a two quadrant DC-DC converter is connected to the same DC link. A single

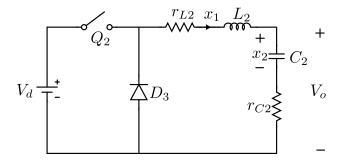


Fig. 5. Simplified circuit of two quadrant converter which is used as voltage source

quadrant converter is used as current source by controlling the inductor current and removing the filter capacitance. The voltage source is realised by controlling the output voltage of the two quadrant converter. Fig. 4 depicts this configuration using high frequency MOSFETs.

Constant voltage of V_o is maintained at the load terminals of the two quadrant converter. However, when switch S in Fig. 2 is opened, the current I_o goes through D to the capacitor of the two quadrant converter. This acts as a disturbance to the voltage source controller and must be rejected at the earliest to maintain the constant voltage across the load terminals.

This implementation does not use transistors and resistors, hence the only losses incurred are the switching and conduction losses of the MOSFETs, and the inductor copper losses.

IV. CONVERTER MODELLING

The power supply depicted in Fig. 4 is composed of three components viz. single quadrant converter acting as current source, two quadrant converter acting as voltage source, and the ignition switch. A controller is required for single quadrant and two quadrant converters, hence the state space model for these converters is found out. This section explains the time averaging method to arrive at the small signal models between the output voltage or current and the duty ratio of the switches for both the converters.

A. Voltage Source

Fig. 5 represents the simplified circuit for the two quadrant converter which is to be, hence the small signal transfer function $\frac{\hat{v}_o}{\hat{d}}$ is to be found out. The current through the inductor L_2 and the voltage across capacitor C_2 are considered as the state variables.

When the switch Q_2 is on i.e. for time DT_s , current flows though V_d , Q_2 , r_{L_2} , L_2 , r_{C_2} and C_2 . Applying Kirchhoff's Voltage Law along this path gives

$$V_d - L_2 \dot{x}_1 - r_{L_2} x_1 - r_{C_2} x_1 - x_2 = 0 \tag{1}$$

From current through the inductor and the capacitor is same, therefore

$$x_1 = C_2 \dot{x_2} \tag{2}$$

The output voltage is

$$V_o = r_{C_2} x_1 + x_2 \tag{3}$$

Therefore,

$$\dot{x}_1 = -\frac{r_{L_2} + r_{C_2}}{L_2} x_1 - \frac{1}{L_2} x_2 + \frac{1}{L_2} V_d$$

$$\dot{x}_2 = \frac{1}{C_2} x_1$$

$$V_o = r_{C_2} x_1 + x_2$$
(4)

When Q_2 is off i.e. for time $(1-D)T_s$, current flows through D_3 , r_{L_2} , L_2 , r_{C_2} and C_2 . Applying Kirchhoff's Voltage Law along this path gives

$$-L_2\dot{x}_1 - r_{L_2}x_1 - r_{C_2}x_1 - x_2 = 0 (5)$$

Also.

$$x_1 = C_2 \dot{x_2} \tag{6}$$

The output voltage is

$$V_o = r_{C_2} x_1 + x_2 (7)$$

Therefore,

$$\dot{x}_1 = -\frac{r_{L_2} + r_{C_2}}{L_2} x_1 - \frac{1}{L_2} x_2$$

$$\dot{x}_2 = \frac{1}{C_2} x_1$$

$$V_o = r_{C_2} x_1 + x_1$$
(8)

Constructing the state vector x as

$$x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{9}$$

In equation (40), let

$$A_1 = \begin{bmatrix} -\frac{r_{L_2} + r_{C_2}}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_2} & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L_2} \\ 0 \end{bmatrix} \quad C_1 = \begin{bmatrix} r_{C_2} & 1 \end{bmatrix}$$
 derived by introducing small perturbations in x , V_o , and d and treatment is described in appendix A. The small signal transfer function for this representation is derived by introducing small perturbations in x , V_o , and d and treatment is described in appendix A. The small signal transfer function of the output voltage of two quadrant converter with

Therefore,

$$\dot{x} = A_1 x + B_1 V_d$$

$$V_o = C_1 x \tag{11}$$

In equation (81), let

$$A_{2} = \begin{bmatrix} -\frac{r_{L_{2}} + r_{C_{2}}}{L_{2}} & -\frac{1}{L_{2}} \\ \frac{1}{C_{2}} & 0 \end{bmatrix} \quad B_{2} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad C_{1} = \begin{bmatrix} r_{C_{2}} & 1 \end{bmatrix}$$
(12)

Therefore,

$$\dot{x} = A_1 x + B_1 V_d$$

$$V_0 = C_1 x$$
(13)

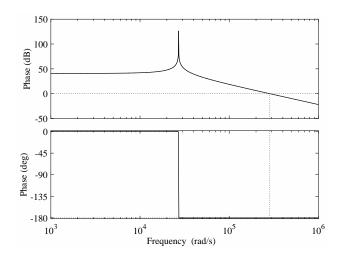


Fig. 6. Bode plot of uncompensated transfer function of voltage source; Gm $= \infty$, Pm = 0.0166° (at 2.85e+05 rad/s)

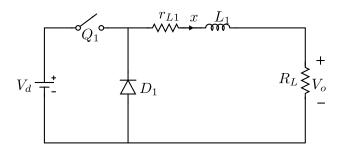


Fig. 7. Simplified circuit of single quadrant converter which is used as current

Equation (11) is valid for dT_s and equation (13) is valid for $(1-d)T_s$. Time averaging equations (11) and (13) leads to

$$\dot{x} = [dA_1 + (1-d)A_2]x + [dB_1 + (1-d)B_2]V_d$$

$$V_o = [dC_1 + (1-d)C_2]x$$
(14)

Small signal transfer function for this representation is function of the output voltage of two quadrant converter with respect to the duty ratio of the switch Q_2 turns out to be

$$\therefore \frac{\hat{v}_o(s)}{\hat{d}(s)} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X \quad (15)$$

The bode plot for this transfer function when the values of inductors and capacitors are chosen as described in section VI is shown in Fig. 6

B. Current Source

Similar approach is applied for finding out the transfer function of the output current with respect or the duty cycle of the switch Q_1 for the single quadrant converter. Fig. 7 shows the simplified circuit diagram for the same. The current through the inductor L_1 is the only state variable in this case.

When the switch Q_1 is on i.e. for time dT_s , current flows though V_d , Q_1 , r_{L_1} , L_1 and R_L . Applying Kirchhoff's Voltage Law along this path gives

$$V_d - L_1 \dot{x} - r_{L_1} x - R_L x = 0 \tag{16}$$

The output current is

$$I_o = x \tag{17}$$

Therefore.

$$\dot{x} = -\frac{r_{L_1} + R_L}{L_2} x + \frac{1}{L_2} V_d$$

$$I_0 = x$$
(18)

When Q_1 is off i.e. for time $(1-d)T_s$, current flows through D_1 , r_{L_1} , L_1 and R_L . Applying Kirchhoff's Voltage Law along this path gives

$$-L_1\dot{x} - r_{L_1}x - R_Lx = 0 (19)$$

The output current is

$$I_o = x \tag{20}$$

Therefore,

$$\dot{x} = -\frac{r_{L_1} + R_L}{L_2} x \tag{21}$$

$$L_2 = x$$

Therefore,

$$A_{1} = -\frac{r_{L_{1}} + R_{L}}{L_{1}} = A_{2}$$

$$B_{1} = \frac{1}{L_{1}} \quad B_{2} = 0$$

$$C_{1} = 1 = C_{2}$$
(22)

The transfer function $\frac{\hat{i}_o}{\hat{d}}$ is obtained using equations (22) in

$$\frac{\hat{i}_o(s)}{\hat{d}(s)} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X \quad (23)$$

where

$$A = A_1 d + A_2 (1 - d) (24)$$

(25)

The bode plot for this transfer function when the values of inductors and capacitors are chosen as described in section VI is shown in Fig. 8

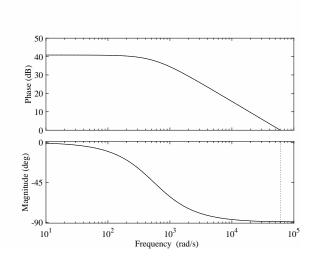


Fig. 8. Bode plot of uncompensated current source transfer function; Gm = ∞ , Pm = 90.5° (at 6.05e+04 rad/s)

V. CONTROLLER DESIGN

The dielectric strength of deionized water is around 70 MV/m. Therefore, if the gap is 1μ m, minimum voltage of 70 V is required to ensure the sparking. Keeping a sufficient margin, the control objectives for the power supply are as follows

- 1) Voltage source must maintain a voltage $V_{\rm ref}$ i.e. 80 V across its load terminals while rejecting load current disturbances up to $I_{\rm ref}$ i.e. 10 A.
- 2) Current source must provide a current of 10 A.
- 3) Generating switching signal for Q_d to control the erosion time during each machining cycle

The control objectives mentioned above are to be achieved by designing a scheme for switching the appropriate devices such that the aforementioned criteria is satisfactorily met. A PI controller was implemented and tuned using trial and error initially. However, this section describes a more systematic approach of compensator design based on the frequency response of the small signal transfer functions derived earlier. Automated K Factor approach [22] used conventionally for power electronic converters was found inadequate in this case. The removal of capacitor in current source and the load from the voltage source lead to different models than those for which this approach has been tested. Hence, the compensator design criteria is discussed in this section. This section also describes a relatively advantageous technique of current mode control.

A. Direct Duty Ratio Control

A simple method to achieve this goal is varying the duty cycle of a pulse width modulated (PWM) signal with fixed frequency F_s . F_s is the switching frequency of the MOSFETs used in the converters. A feedback loop is constructed by using a lead-lag compensator for this purpose as shown in Fig. 9.

For two quadrant converter, since the control objective is tracking the reference voltage $v_{\rm ref}$, the output voltage v(t) is sensed. v(t) is compared with $v_{\rm ref}$ to obtain the error signal.

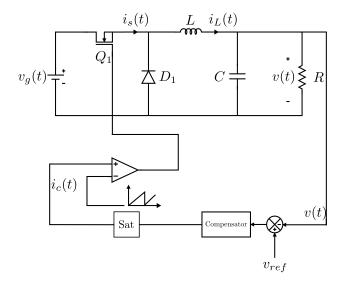


Fig. 9. Block diagram of direct duty ratio control of single quadrant converter

This error signal is the representative of the deviation of current state of the system from the desired state. The design procedure followed is described next.

To improve the transient response gain crossover frequency ω_{gc} should be as high as possible but approximately an order on magnitude below the switching frequency to allow the power supply to respond quickly to the transients. This was chosen as

$$\omega_{\rm cross} = \frac{2\pi F_s}{10} \tag{26}$$

Also, the desirable range of phase margin is 45 to 60° [23]. Let the desired phase margin be PM_{des} . Phase that has to be added to the system is

$$\phi_{m_1} = PM_{des} - \left(180 + \phi_{\rm OL}\Big|_{\omega = \omega_{\rm cross}}\right) \tag{27}$$

The general form of compensator is

$$G_{\text{lead}} = \frac{1 + a_1 T_1 s}{1 + T_1 s} \tag{28}$$

where $a_1 > 1$

The maximum phase lead due to this compensator is given by

$$\phi_{m_1} = \sin^{-1} \left(\frac{a_1 - 1}{a_1 + 1} \right) \tag{29}$$

This phase lag is added in between the corner frequencies $\frac{1}{T_1}$ and $\frac{1}{a_1T_1}$ and is maximum at

$$\omega_{m_1} = \frac{1}{T_1 \sqrt{a_1}} \tag{30}$$

Thus, to make phase margin as desired at the gain crossover frequency as decided, T_1 and a_1 are chosen as

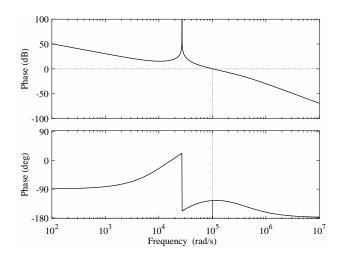


Fig. 10. Bode plot of compensated transfer function of voltage source Gm = ∞ , Pm = 54.3° (at 1.02e+05 rad/s)

$$a_{1} = \frac{1 + \sin(\phi_{m_{1}})}{1 - \sin(\phi_{m_{1}})}$$

$$T_{1} = \frac{1}{\omega_{m_{1}}\sqrt{a_{1}}}$$
(31)

To reduce the steady state error, a lag compensator G_{lag} is required such that $\omega_{m_2} << \omega_{\text{cross}}$. In the general form

$$G_{\text{lag}} = \frac{1 + a_2 T_2 s}{1 + T_2 s} \tag{32}$$

where $0 < a_2 < 1$.

The steady state gain added by this compensator is

$$\lim_{s \to \infty} \frac{1 + a_2 T_2 s}{1 + T_2 s} = \frac{1}{a_2} \tag{33}$$

Choosing a small enough a_2 , T_2 was found as

$$T_2 = \frac{1}{\omega_{m_2} \sqrt{a_2}}$$
 (34)

Finally, the loop gain was balanced by taking K as

$$K = \left| \frac{1}{G_{\text{lao}} G_{\text{lead}} G_{\text{OL}}} \right|_{\omega = \omega_{\text{cross}}}$$
 (35)

The final controller is

$$G_c(s) = KG_{\text{lag}}G_{\text{lead}} \tag{36}$$

The bode plot for compensated open loop transfer function of the voltage source is shown in Fig. 10

For the current source, phase margin is already sufficient, so closing the negative feedback loop with unity should be enough. This was verified in the simulation.

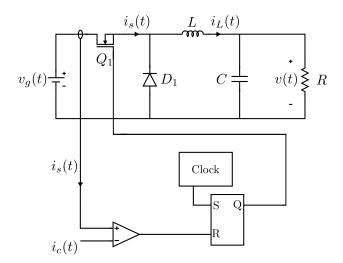


Fig. 11. Block diagram of current mode control of single quadrant converter

B. Current Mode Control

Converters employing direct duty ratio control require a separate protection against over current for each switch. However, if the control method is based on the peak current through switch, then the requirement for such a protection effort is eliminated as the current is not allowed to rise above a particular threshold in each switching cycle. Also, the dynamics of such a controller are much simple than the direct duty ratio control. This section describes peak current mode control [24], loosely referred to as current mode control, which employs this method to achieve the output current or voltage tracking objective.

Fig. 11 represents the block diagram for current mode control of a single quadrant converter. At the start of each switching cycle of frequency F_s , Q_1 is switched on by a clock pulse which sets the latch in a high state. The switch remains in the on state until a reset pulse is applied to the latch. During on time, the current $i_s(t)$ through Q_1 rises with slope m_1 as shown in Fig. 12. When $i_s(t)$ reaches the control current $i_c(t)$, the comparator, being non inverting in nature, generates a reset pulse for the latch which turns the switch off. For the remainder of the switching period, the current through switch is zero. If inductor L is chosen such that the converter operates in continuous conduction mode around $i_c(t)$, then the current through the inductor decreases at a rate of $-m_2$ during the off time to a value of $i_L(T_S)$ at T_s as shown in Fig. 13.

The slopes m_1 and $-m_2$ are given by

$$m_1 = \frac{v_g - v}{L} \quad \text{and} \quad -m_2 = \frac{v}{L} \tag{37}$$

where v_g is the dc link voltage, v is the output voltage, and L is the value of inductor of the buck converter. During on time, inductor current at $t=dT_s$, $\hat{i}_L(dT_s)$ in terms of slope m_1 is given by

$$i_L(dT_s) = i_C = i_L(0) + m_1 dT_S$$
 (38)

During off time, inductor current at $t = T_s$ is

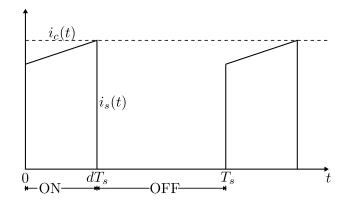


Fig. 12. Switch current in current mode control of single quadrant converter

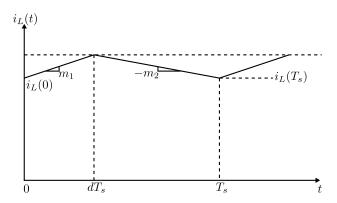


Fig. 13. Inductor current in current mode control of single quadrant converter

$$i_L(T_s) = i_L(dT_s) - m_2(1-d)T_S$$

Substituting $i_L(dT_s)$ from equation (37) in this relation results in

$$i_L(T_s) = i_L(0) + m_1 dT_S - m_2(1-d)T_S$$
 (39)

At steady state, $i_L(0) = i_L(T_s)$, d = D, $m_1 = M_1$, and $m_2 = M_2$. From equations (38) and (39), at steady state

$$0 = M_1 D T_S - M_2 (1 - D) T_S$$

$$\frac{M_2}{M_1} = \frac{D}{1 - D} \tag{40}$$

This method requires additional current sensing circuit as compared to duty ratio control methods, but in practice, duty ratio control methods also require current sensing circuit for protection against over currents. This method exploits the available current sensors which would otherwise be operating independently from the control scheme to achieve the control objective. Switch failures due to excessive currents are avoided by limiting the maximum value of control signal $i_c(t)$ thus ensuring that the switch will turn off when excessive current flows through it during each switching period.

The only disadvantage of current mode control is its high susceptibility to noise. Perturbations in sensed switch current can cause premature turn off of the switch. Also, converter becomes unstable even for small perturbations in switch

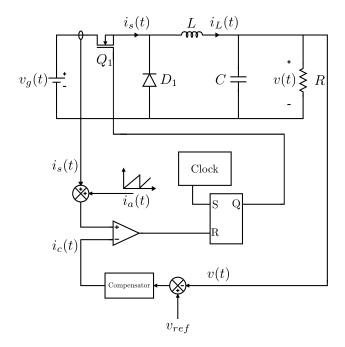


Fig. 14. Controlled voltage source using current mode control

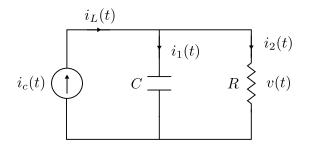


Fig. 15. Current mode control replaced as current source in buck converter

current when operating on duty cycles greater than 50% as the perturbation increases in magnitude in each subsequent switching cycle. However, this can be remedied by adding an artificial ramp to the sensed switch current. The intuition behind this is explained in appendix B.

For the two quadrant converter, an outer voltage feedback loop is constructed on top the current mode controller as shown in Fig. 14. A small signal model of the converter is derived under a justifiable assumption for this purpose. It is assumed that the current mode controller operates ideally, and hence causes the average inductor current i_L to be identical to the control i_c . This approximation is justified whenever the inductor current ripple and artificial ramp have negligible magnitudes. The inductor current then is no longer an independent state of the system because $\frac{i_L}{i_c} \approx 1$. The current mode control part of this controller can be replaced by an ideal current source of magnitude $i_c(t)$ and an equivalent circuit can be constructed as shown in Fig. 15

From Kirchhoff's Current Law, the output current of the current source is

$$i_c(t) = C\frac{dv(t)}{dt} + \frac{v(t)}{R} \tag{41}$$

Let the steady state value of the output current and output voltage be I_c and V respectively. If a small perturbation of magnitude $\hat{i}_c(t)$ is introduced in the current $i_c(t)$, the output voltage v(t) gets perturbed by a magnitude of, say, $\hat{v}(t)$, then

$$i_c(t) = I_c + \hat{i_c}(t) \tag{42}$$

$$v(t) = V + \hat{v}(t) \tag{43}$$

From (41),

$$I_c + \hat{i_c}(t) = C \frac{d}{dt} (V + \hat{v}(t)) + \frac{V + \hat{v}(t)}{R}$$
 (44)

At the steady state,

$$\frac{dV}{dt} = 0 \quad \text{and} \quad I_c = \frac{V}{R} \tag{45}$$

Therefore,

$$\hat{i_c}(t) = C\frac{d\hat{v}(t)}{dt} + \frac{\hat{v}(t)}{R}$$
(46)

Taking Laplace transform

$$\hat{i}_c(s) = sC\hat{v}(s) + \frac{\hat{v}(s)}{R} \tag{47}$$

$$\frac{\hat{v}(s)}{\hat{i}_c(s)} = \frac{R}{1 + sRC} \tag{48}$$

This transfer function represents first order dynamics. Thus, the simpler dynamics in comparison to models required for direct duty ratio control. A PI controller was used to complete the feedback loop to derive a controlled voltage source from a current mode controlled converter.

VI. PRACTICAL CONSIDERATIONS

This section deals with the methodology used to arrive at the capacitor and inductor sizes used for the simulation described in next section.

A. Inductor Selection

The purpose of inductor in DC-DC switched power supplies is to maintain the current when the DC link switch is off i.e. to reduce the ripple in output voltage or current depending on the converter. With this criteria, the inductor value should be high, but when a large inductor is used, the rise time of converter is more as it takes more time for the current to rise. Hence, the selection of inductor is trade-off between the current ripple and transient response of the converter.

For the single quadrant converter which is used as current source, criteria for selection of inductor value is taken to be the the output current ripple of the converter. The relation between inductor value and the output current ripple [23] is

$$\Delta I_L = \frac{V_{o1}}{L_1} (1 - D) T_s \tag{49}$$

where $V_{o1} = I_{ref}R_L$ is the output voltage of the single quadrant converter, L_1 is the value of the inductor, D is the

steady state duty cycle of the converter, ΔI_L is the ripple in in inductor current and $T_s=\frac{1}{F_s}$ is the switching period.

$$L_1 \ge \frac{V_{o1}(V_d - V_{o1})}{\Delta I_L F_s V_d} \tag{50}$$

Based on these calculations, inductor L_1 was chosen to be of 2 mH.

For the voltage source, the boundary condition for continuous conduction mode operation governs the choice of inductor. Because the output current need not be controlled here, the ripple criteria is relaxed in favour of inductor selection on the basis of continuous conduction mode operation. A buck converter operates in continuous conduction mode when the average inductor current satisfies [23]

$$I_{L_2} \ge \frac{DT_s}{2L_2} (V_d - V_{o2}) \tag{51}$$

If the average inductor current $I_{L_{\rm avg}}$ becomes less than this boundary value, the converter will operate in discontinuous mode. To extend the range of operation of the converter to lower average currents, the inductor is chosen such that continuous conduction mode is ensured at the lowest extreme of the intended range of operation. For satisfactory operation [22] at $\frac{1}{5}I_{L_2}$, the condition in inequality (49) is

$$\frac{1}{5}I_{L_2} \ge \frac{DT_s}{2L_2}(V_d - V_{o2}) \tag{52}$$

where $I_{L_2} = V_d/R_L$, D is the steady state duty cycle, $T_s = 1/F_s$ is the switching period, L_2 is the inductor value, and V_d and $V_o = V_{\rm ref}$ are the DC link and converter output voltages respectively. Therefore,

$$L_2 \ge 2.5 \frac{DT_s}{I_{L_2}} (V_d - V_{\text{ref}})$$
 (53)

Based on this relation the inductor for voltage source was chosen to be 1.5 mH.

B. Capacitor Selection

Capacitor is required in the output stage of two quadrant converter to filter out the output voltage ripple. For a ripple of ΔV_{o2} , the value of capacitor required is given by [23]

$$C_2 \ge \frac{\Delta I_{L_2} T_s}{8\Delta V_{o2}} \tag{54}$$

The current ripple is given by,

$$\Delta I_{L_2} \ge \frac{V_{o2}}{L_2} (1 - D) T_s \tag{55}$$

Here, $V_{o2} = V_{ref}$ and $T_s = 1/F_s$,

$$C_2 \ge \frac{1 - D}{8\frac{\Delta V_{o2}}{V_{ref}} L_2 F_s^2} \tag{56}$$

The capacitor was chosen to be of the value $100\mu F$.

C. Snubber Design

Snubber is required across the ignition switch Q_d to limit the over-voltage arising due to opening of the switch. In highly inductive circuits, when switch is opened, the path for current flow is broken. Therefore, a high voltage spike appears on the switch terminals due to large magnitude of $L\frac{di}{dt}$. Energy absorbing circuit like the snubber circuit, reduces these spikes. This section explains the design procedure for a R-C snubber used in parallel with the ignition switch Q_d .

The peak current through the snubber circuit is given by

$$I_p = \frac{V_{oc}}{R_c} \tag{57}$$

where V_{OC} is the open circuit voltage across the switch, R_s is the snubber resistance and I_p is the peak current through the snubber.

The current flowing through Q_d before interruption is $I_{\rm ref}$ and the maximum voltage across the terminals of Q_d is $V_{\rm ref}$. Hence, the snubber resistance R_s should be minimum of

$$R_s \ge \frac{V_{\text{ref}}}{I_{\text{ref}}} \tag{58}$$

The snubber capacitance should be such that

 Energy that is allowed to be stored in the capacitor should be greater than the energy stored in the inductor i.e.

$$\frac{1}{2}C_s V_{oc}^2 \ge \frac{1}{2}L_{eq}I_p^2 \tag{59}$$

$$\therefore C_s \ge \frac{L_{eq} I_p^2}{V_{oc}^2} \tag{60}$$

2) The time constant of the snubber circuit should be small as compared to the shortest on time of Q_d . So, for time constant of snubber circuit to be 10% of the on time of Q_d

$$R_s C_s \le \frac{T_{on}}{10} \tag{61}$$

$$\therefore C_s \le \frac{T_{on}}{10R_s} \tag{62}$$

From equations (58), (60), and (62), R_s was chosen 8Ω and C_s was chosen as $2\mu F$

VII. RESULTS

The values of components derived in above section were used in a simulation of the converter with 50 kHz switching frequency and 5 kHz machining frequency. The voltage and current waveforms across the load when direct duty ratio control is used are shown in Fig. 16.

The output waveforms thus obtained are in well agreement with the results in [21].

Fig. 17 shows the voltage across Q_d and current through Q_d waveforms when direct duty ratio control is used. The maximum voltage across Q_d is $V_{\rm ref}$ i.e. 80 V and and the maximum current through Q_d is 11 A during the rise time.

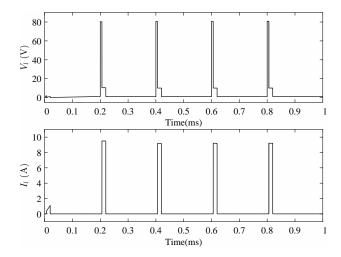


Fig. 16. Load voltage and current - direct duty ratio control

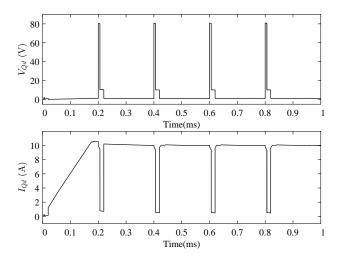


Fig. 17. Voltage and current of Qd - direct duty ratio control

Fig. 18 shows the voltage across D and current through D waveforms when direct duty ratio control is used. The maximum reverse voltage across D is 83 V and the maximum forward current through it is 0.8 A.

Fig. 19 shows the voltage across Q_1 and current through Q_1 waveforms when direct duty ratio control is used. The maximum voltage across Q_1 is V_d i.e 110 V and the maximum current through it is 11 A.

Fig. 20 shows the voltage across D_1 and current through D_1 waveforms when direct duty ratio control is used. The maximum reverse voltage across diode D_1 is V_d i.e. 110 V and the maximum forward current through it is 11 A.

Fig. 21 shows the voltage across Q_2 and current through Q_2 waveforms when direct duty ratio control is used. The maximum voltage across Q_2 is V_d i.e 110 V and the maximum current through it is 21 A. This maximum occurs during the rise time of the voltage source.

Fig. 22 shows the voltage across D_2 and current through D_2 waveforms when direct duty ratio control is used. The maximum reverse voltage across D_2 is V_d i.e. 110 V and the maximum current through it is 4.5 A.

Fig. 23 shows the voltage across Q_3 and current through

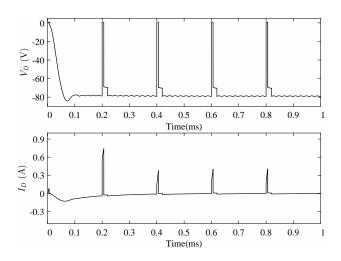


Fig. 18. Voltage and current of D - direct duty ratio control

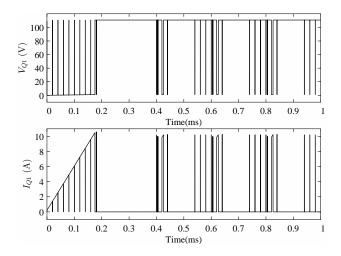


Fig. 19. Voltage and current of Q1 - direct duty ratio control

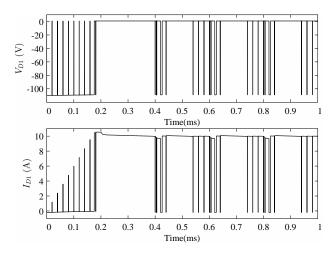


Fig. 20. Voltage and current of D1 - direct duty ratio control

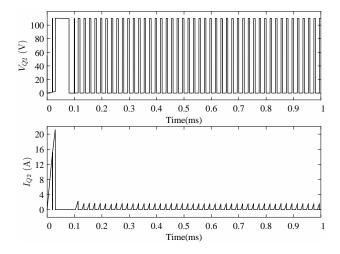


Fig. 21. Voltage and current of Q2 - direct duty ratio control

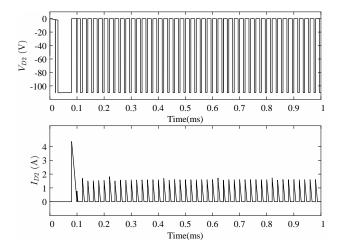


Fig. 22. Voltage and current of D2 - direct duty ratio control

 Q_3 waveforms when direct duty ratio control is used. The maximum voltage across Q_3 is 110 V and the maximum current through it is 4.5 A.

Fig. 24 shows the voltage across D_3 and current through D_3 waveforms when direct duty ratio control is used. The maximum reverse voltage across D_3 is 110 V and the maximum current through it is 21 A.

Fig. 25 shows the load voltage and current waveforms when current mode control is used.

VIII. FUTURE PLAN

A. Fabrication of Power Supply

The power supply design has been completed and the next step would be designing the PCBs and Gate drivers. Once these are done, the power supply could be assembled. The testing of power supply is to be done with the spark gap jar available in the Insulation Diagnostics lab. The X-Y slides were ordered previous to match the specifications required for further experimentation. These have now arrived and and can be used to make a desktop EDM setup for further experimentation.

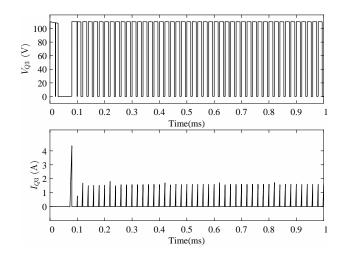


Fig. 23. Voltage and current of Q3 - direct duty ratio control

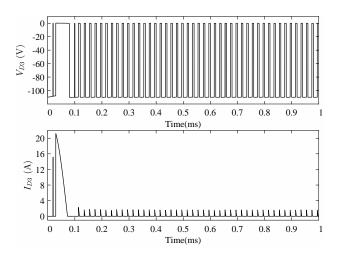


Fig. 24. Voltage and current of D3 - direct duty ratio control

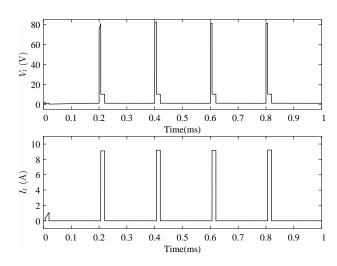


Fig. 25. Load voltage and current - current mode control

B. Load Modelling

The electrical characterisation of the spark gap load is to be done. Previous research has established that spark gaps can be represented as parallel combination of R, L and C elements. The further experimentation would be directed towards fitting a model or approximating these values directly to obtain a load model. This will help in better understanding and also to highlight any scope for improvement in the power supply.

REFERENCES

- [1] Report, "Office memorandum," Ministry of New and Renewable Energy, Government of India, 2016. [Online]. Available: http://mnre.gov.in/file-manager/UserFiles/Tentative-State-wise-break-up-of-Renewable-Power-by-2022.pdf
- [2] C. Del Canizo, G. Del Coso, and W. Sinke, "Crystalline silicon solar module technology: Towards the 1 euro per watt-peak goal," *Progress* in photovoltaics: research and applications, vol. 17, no. 3, pp. 199–209, 2009.
- [3] B. Sopori, S. Devayajanam, S. Shet, D. Guhabiswas, P. Basnyat, H. Moutinho, L. Gedvilas, K. Jones, J. Binns, and J. Appel, "Characterizing damage on Si wafer surfaces cut by slurry and diamond wire sawing," in 39th Photovoltaic Specialists Conference (PVSC). IEEE, 2013, pp. 0945–0950.
- [4] G. G. Dongre, C. Vesvikar, R. K. Singh, and S. S. Joshi, "Efficient dicing of silicon ingots for photovoltaic applications," in 35th IEEE Photovoltaic Specialists Conference, June 2010, pp. 3629–3634.
- [5] H. J. Moeller, "Chapter two-wafering of silicon," Semiconductors and Semimetals, vol. 92, pp. 63–109, 2015.
- [6] G. Dongre, S. Zaware, U. Dabade, and S. S. Joshi, "Multi-objective optimization for silicon wafer slicing using wire-edm process," *Materials Science in Semiconductor Processing*, vol. 39, pp. 793–806, 2015.
- [7] J. Sanchez, I. Cabanes, L. L. de Lacalle, and A. Lamikiz, "Development of optimum electrodischarge machining technology for advanced ceramics," *The International Journal of Advanced Manufacturing Technology*, vol. 18, no. 12, pp. 897–905, 2001.
- [8] M. Kane, "Annual progress seminar report," Indian Institute of Technology Bombay, August 2017.
- [9] G. Levy and F. Maggi, "Wed machinability comparison of different steel grades," CIRP Annals-Manufacturing Technology, vol. 39, no. 1, pp. 183–185, 1990.
- [10] K. Ho, S. Newman, S. Rahimifard, and R. Allen, "State of the art in wire electrical discharge machining (WEDM)," *International Journal of Machine Tools and Manufacture*, vol. 44, no. 12, pp. 1247–1259, 2004.
- [11] G. Spur and J. Schönbeck, "Anode erosion in wire-edm-a theoretical model," CIRP Annals-Manufacturing Technology, vol. 42, no. 1, pp. 253–256, 1993.
- [12] F. Han, M. Kunieda, T. Sendai, and Y. Imai, "High precision simulation of wedm using parametric programming," CIRP Annals-Manufacturing Technology, vol. 51, no. 1, pp. 165–168, 2002.
- [13] N. Kinoshita, M. Fukui, H. Shichida, and G. Gamo, "Study of edm with wire electrode–gap phenomena," in *CIRP Annales*, vol. 25, no. 1, 1976, pp. 141–145.
- [14] H. De Bruyn and A. Pekelharing, "Has the delay time influence on the edm-process?" CIRP Annals-Manufacturing Technology, vol. 31, no. 1, pp. 103–106, 1982.
- [15] N. Kinoshita, M. Fukui, and G. Gamo, "Control of wire-edm preventing electrode from breaking," CIRP Annals-Manufacturing Technology, vol. 31, no. 1, pp. 111–114, 1982.
- [16] M. Kunieda, H. Kojima, and N. Kinoshita, "On-line detection of edm spark locations by multiple connection of branched electric wires," CIRP Annals-Manufacturing Technology, vol. 39, no. 1, pp. 171–174, 1990.
- [17] D. Dauw and I. Beltrami, "High-precision wire-edm by online wire positioning control," CIRP Annals-Manufacturing Technology, vol. 43, no. 1, pp. 193–197, 1994.
- [18] J. Wang and B. Ravani, "Computer aided contouring operation for traveling wire electric discharge machining (edm)," *Computer-Aided Design*, vol. 35, no. 10, pp. 925–934, 2003.
- [19] N. Mohri, H. Yamada, K. Furutani, T. Narikiyo, and T. Magara, "System identification of wire electrical discharge machining," CIRP Annals-Manufacturing Technology, vol. 47, no. 1, pp. 173–176, 1998.
- [20] K. Rajurkar, W. Wang, and W. Zhao, "Wedm-adaptive control with a multiple input model for indentification of workpiece height," CIRP Annals-Manufacturing Technology, vol. 46, no. 1, pp. 147–150, 1997.

- [21] D. Tastekin, H. Krotz, C. Gerlach, and J. Roth-Stielow, "A novel electrical power supply for electrothermal and electrochemical removal machining methods," in *Energy Conversion Congress and Exposition*, 2009. ECCE 2009. IEEE. IEEE, 2009, pp. 2682–2688.
- [22] N. Muhamad, M. Sahid, A. Yatim, N. Idris, and M. Ayob, "Design of power stage and controller for dc-dc converter systems using pspice," in Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on, vol. 2. IEEE, 2005, pp. 903–908.
- [23] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. John Wiley & Sons, Inc., 2002.
- [24] R. W. Erickson and D. Maksimovi, Fundamentals of Power Electronics, 2nd ed. Springer US, 2004.

APPENDIX A

TIME AVERAGING MODELLING TECHNIQUE

The large signal representation of voltage source in Fig. 5 as derived in equation (14)

$$\dot{x} = [dA_1 + (1 - d)A_2]x + [dB_1 + (1 - d)B_2]V_d$$

$$V_o = [dC_1 + (1 - d)C_2]x$$

Introducing small perturbations in x, V_o and d as

$$x = X + \hat{x}$$

$$v_o = V_o + \hat{v_o}$$

$$d = D + \hat{d}$$
(63)

Since the transfer function is to be determined between $\hat{v_o}$ and \hat{d} , perturbations in v_d are assumed to be zero for simplicity, therefore

$$v_d = V_d \tag{64}$$

Using the fact that at steady state $\dot{X}=0$ and the equations (63) in equation (14)

$$\dot{\hat{x}} = AX + BV_d + A\hat{x} + [(A_1 - A_2)X + (B_1 - B_2)V_d]\hat{d}$$
+ terms with products of \hat{x} and \hat{d} (neglected) (65)

where

$$A = A_1 D + A_2 (1 - D) (66)$$

$$B = B_1 D + B_2 (1 - D) (67)$$

At steady state, the perturbations in equation (65) are zero, therefore

$$AX + BV_d = 0 (68)$$

Hence, when perturbations are introduced in a converter operating under steady state

$$\dot{\hat{x}} = A\hat{x} + [(A_1 - A_2)X + (B_1 - B_2)V_d]\hat{d}$$
 (69)

Similarly, for output voltage, using equations (63) in equation (14)

$$V_o + \hat{v}_o = CX + C\hat{x} + [(C_1 - C_2)X]\hat{d}$$
 (70)

where

$$C = C_1 D + C_2 (1 - D) (71)$$

At steady state

$$V_o = CX \tag{72}$$

Hence, when perturbations are introduced in a converter operating under steady state

$$\hat{v}_o = C\hat{x} + [(C_1 - C_2)X]\hat{d} \tag{73}$$

Taking Laplace transform of equation (69)

$$s\hat{x}(s) = Ax(s) + [(A_1 - A_2)X + (B_1 - B_2)V_d]\hat{d}(s)$$
 (74)

$$\therefore \hat{x}(s) = [sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d]\hat{d}(s)$$
 (75)

where I is a unity matrix Taking Laplace transform of equation (73)

$$\hat{v}_o(s) = C\hat{x}(s) + [(C_1 - C_2)X]\hat{d}(s) \tag{76}$$

Substituting in $\hat{x}(s)$ from equation (75)

$$\hat{v}_o(s) = \{C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X\}\hat{d}(s)$$
 (77)

$$\therefore \frac{\hat{v}_o(s)}{\hat{d}(s)} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X \quad (78)$$

This is the small signal transfer function of the output voltage of two quadrant converter with respect to the duty ratio of the switch \mathcal{Q}_2

APPENDIX B INSTABILITY IN CURRENT MODE CONTROL

Consider the waveform of steady state switch current as shown in Fig. 26 for a buck converter operating at duty cycle D>0.5. A small perturbation $\hat{i}_L(0)$ such that $|\hat{i}_L(0)|<<<|i_L(0)|$ is introduced in inductor current $i_L(t)$ which same as the switch current $i_s(t)$ at time t=0. During on time, the perturbed inductor current rises with slope of m_1 till time $(D+\hat{d})T_s$. At this instant, perturbed $i_L(t)=i_c(t)$ and the switch turns off. For the remainder of switching signal, $i_L(t)$ decreases with slope $-m_2$, and at $t=T_s$ the perturbation in inductor current is $\hat{i}_L(T_s)$.

Fig. 27 is the expanded view of perturbed and steady state inductor current between times $(D + \hat{d})T_s$ and T_s . Inductor current at time t = 0 is given by

$$i_L(0) = i_{L0} + \hat{i}_L(0)$$

The perturbation in inductor current at t=0 and $t=T_s$ are given by

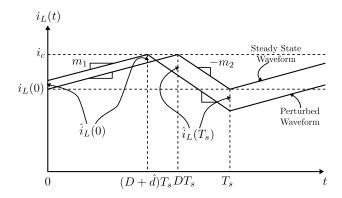


Fig. 26. Inductor current in presence of disturbance

$$\hat{i}_L(0) = -m_1 \hat{d}T_s \tag{79}$$

$$\hat{i}_L(T_s) = m_2 \hat{d}T_s \tag{80}$$

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{m_2}{m_1}\right)$$
 (81)

From relation governing slopes m_1 and m_2 in equation (40),

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{D}{1-D} \right) \tag{82}$$

At each cycle the perturbation will magnify by a factor of $\frac{D}{1-D}$, therefore, after n such switching cycles, the perturbation in inductor current is

$$i_L(nT_s) = i_L(0) \left(-\frac{D}{1-D}\right)^n \tag{83}$$

Thus, the magnification of initial perturbation depends on the duty ratio of the switch operation. If D < 0.5, then the magnification factor $|\frac{D}{1-D}| < 1$, and any initial perturbations in the inductor or switch current will eventually die down. But, if D > 0.5, then $|\frac{D}{1-D}| > 1$, the perturbations will only increase in magnitude with time, irrespective of the initial magnitude of the perturbation. Thus,

$$|\hat{i}_L(nT_s)| \longrightarrow \begin{cases} 0 & \text{when } \left| -\frac{D}{1-D} \right| < 1 \\ \infty & \text{when } \left| -\frac{D}{1-D} \right| > 1 \end{cases}$$
 (84)

In this form, the satisfactory operation of converter is limited to a range $0 \le D \le 0.5$. To overcome this limitation, an artificial ramp $i_a(t)$ with slope m_a and frequency equal to the switching frequency F_s is added with the switch current as shown in Fig. 28. Due to the addition of this ramp, the controller causes the switch to turn off when

$$i_a(t) + i_L(t) = i_c$$

i.e.

$$i_L(t) = i_c - i_a(t) \tag{85}$$

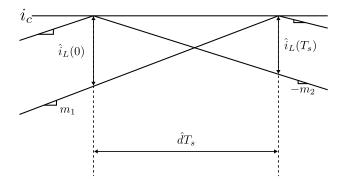


Fig. 27. Expanded view of perturbed inductor current

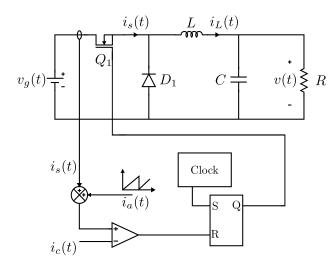


Fig. 28. Block diagram of current mode control with artificial ramp compensation

Fig. 29 shows the steady state and perturbed current waveforms for buck converter operating at duty D>0.5 in presence of initial perturbation $\hat{i}_L(0)$. From Fig. 30, the initial disturbance in terms of slopes m_1 and m_a is

$$\hat{i}_L(0) = -\hat{d}T_s(m_1 + m_a) \tag{86}$$

$$\hat{i}_L(T_s) = -\hat{d}T_s(m_a - m_2) \tag{87}$$

Therefore,

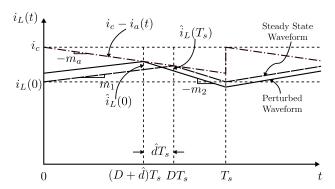


Fig. 29. Inductor current with artificial ramp in presence of disturbance

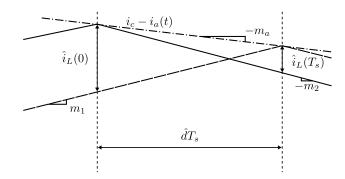


Fig. 30. Expanded view of inductor current with artificial ramp in presence of disturbance

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{m_2 - m_a}{m_1 + m_a} \right)$$
 (88)

The magnification in perturbation after n switching cycles is Therefore,

$$\hat{i}_L(nT_s) = \hat{i}_L(0) \left(-\frac{m_2 - m_a}{m_1 + m_a} \right)^n \tag{89}$$

When $n \longrightarrow \infty$,

$$|\hat{i}_L(nT_s)| \longrightarrow \begin{cases} 0 & \text{when} \quad |\alpha| < 1\\ \infty & \text{when} \quad |\alpha| > 1 \end{cases}$$
 (90)

where

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a}$$

For stable operation of converter, the slope of the artificial ramp m_a such that the magnification factor $|\alpha|<1$. α from can be rearranged as

$$\alpha = -\frac{1 - \frac{m_a}{m_2}}{\frac{1 - D}{D} + \frac{m_a}{m_2}} \tag{91}$$

If m_a is chosen such that $m_a=\frac{1}{2}m_2$, then from equation (91) $\alpha=-1$ at D=1 and $|\alpha|<1$ for $0\leq D<1$. This is the minimum slope required for artificial ramp to stabilise the operation of converter over all operating duties. If m_a is chosen such that $m_a=m_2$, then α is zero for all D. Therefore, $\hat{i}_L(T_s)$ is 0 for any $\hat{i}_L(0)$. Thus, the system has finite settling time and removes any perturbation after one switching period T_s .