Modelling and Control of WEDM Process for Cutting of Si-Ingots

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Introduction

Introduction

- Solar energy: prominent source of renewable energy
- Extracting silicon wafers accounts for 20% of total energy consumption throughout process [1]
- Popular methods for silicon cutting:
  i) Wire loose slurry method
  ii) Diamond saw cutting method
- Abrasive nature - lead to micro-fractures up to 20 μm deep
- Wafer size gets limited to 180 μm [2]
- 50% of ingot material is lost as kerf losses [3]
- Contamination of wafers due to slurry, etc. [4]

Wire Electro-Discharge Machining

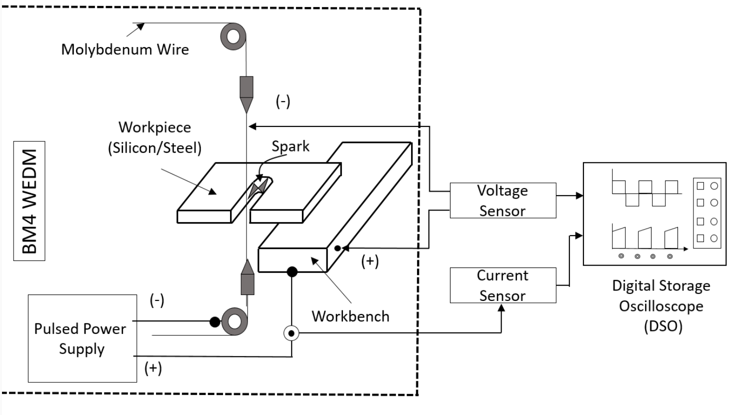


Figure 1: Diagrammatic representation of WEDM

Wire Electro-Discharge Machining

- Non contact micro-drilling process
- Cuts free form contours from large solid metal workpieces
- No force exerted on workpiece – Thinner wires can be used
- Reduced kerf width [5]
  250 μm – Abrasive saw cutting
  50 μm – WEDM
- Net material saving of 200 – 300% [5]
- WEDM: A promising alternative for silicon wafer manufacturing
- Goal: Optimise WEDM process for silicon wafers

Wire Electro-Discharge Machining

- WEDM is not as well established for silicon
- Electrical characterisation of metal-semiconductor-dielectric sparks
- VI characteristics of silicon are very different from that of steel [6]
- Settings on commercial WEDM machines are only applicable for steel [7]
- Available machines have discrete setting ranges
- Indigenously designed power supply required
- Completed: Design, modelling and control of such power supply

Literature Survey

Research areas

Process Modelling	
Spur and Schönbeck [8]	Influence of work-piece material and pulse type
Han et al. [9]	Simulated discharge phenomena of WEDM, developed adaptive control system
Fuzzy Control Systems	
Kinoshita et al. [10]	Investigated effects of wire feed rate, winding speed, tension and electrical parameters
De Bruyn et al. [11]	Classified EDM pulses as open, spark, arc, off or, short on basis of ignition delay
Wire Breakage Avoidance	
Kinoshita et al. [12]	Rapid rise in pulse frequency of voltage before wire breakage, developed a monitoring system that switches off pulse generator
N. Kinoshita, M. Fukui, and G. Gamo [13]	Increase in localised temperature at certain points of wire leads to its breakage, system for detection of spark location

Research areas

Wire lag and wire vibration	
Duaw and Beltrami [14]	Used optical sensor for monitoring and control of wire position
N. Mohri et al. [15]	Several mathematical models – transient response of wire vibration – force acting on tool
Adaptive control systems	
Kinoshita et al. [12]	Change in work-piece thickness – increase in wire thermal density
Rajurkar et al. [16]	Adaptive control & multiple input model – monitors & controls sparking frequency according to on-line identified work-piece height

Power Supply Design

Working Principle

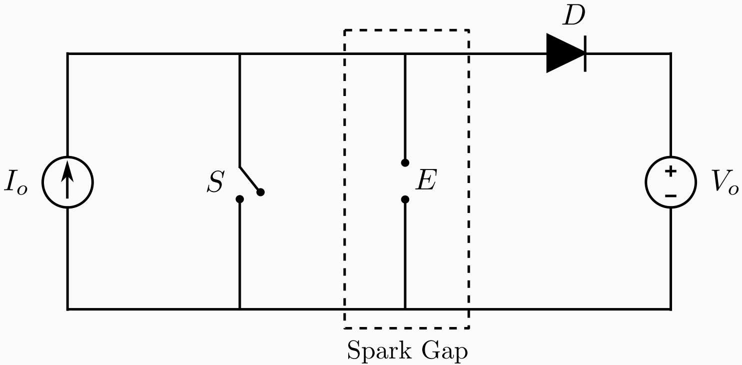
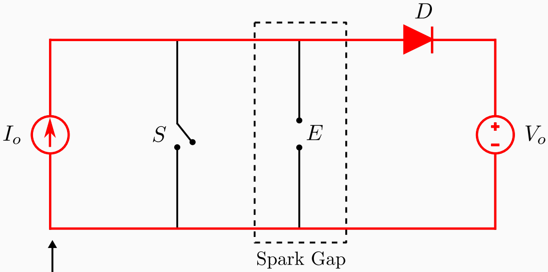
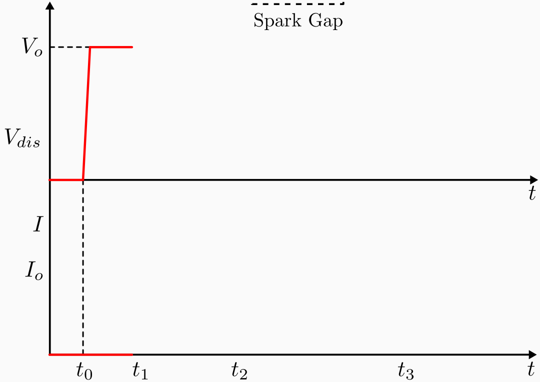


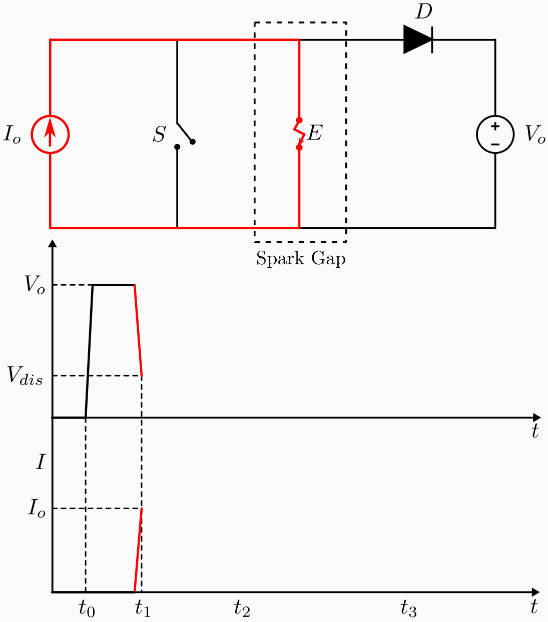
Figure 2: Representative diagram of ideal WEDM power supply

Working Principle

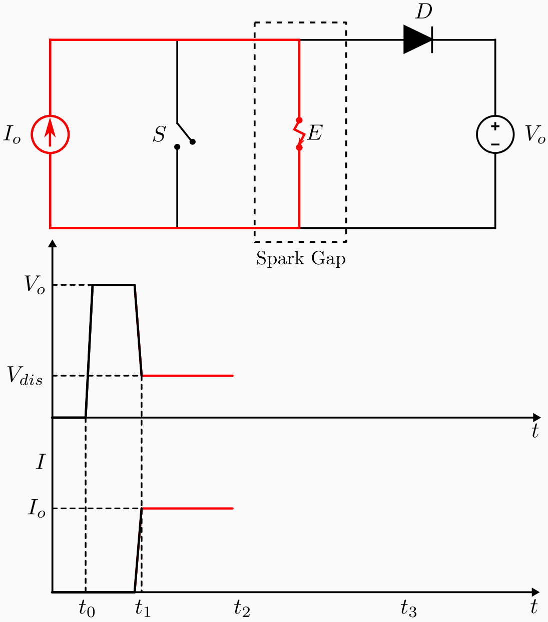




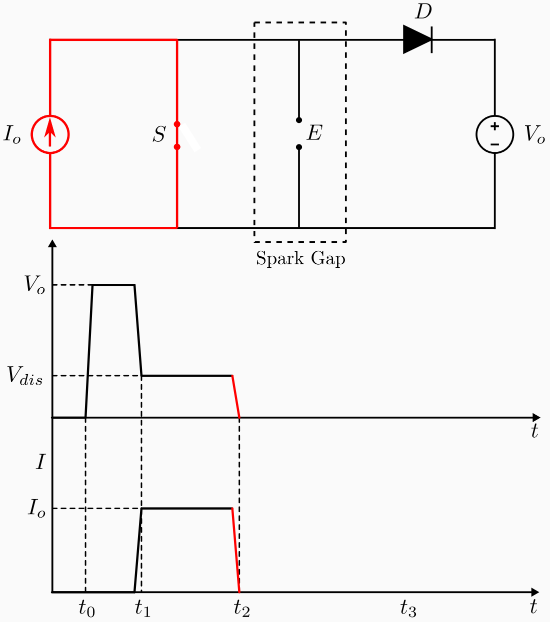
Working Principle



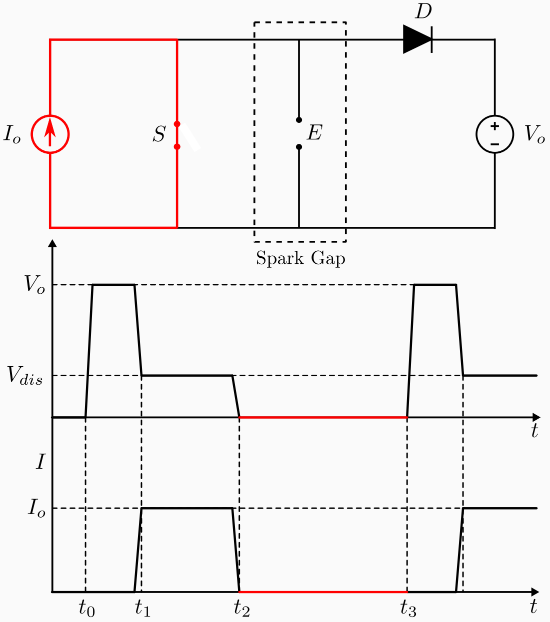
Working Principle



Working Principle



Working Principle



Converter Topology

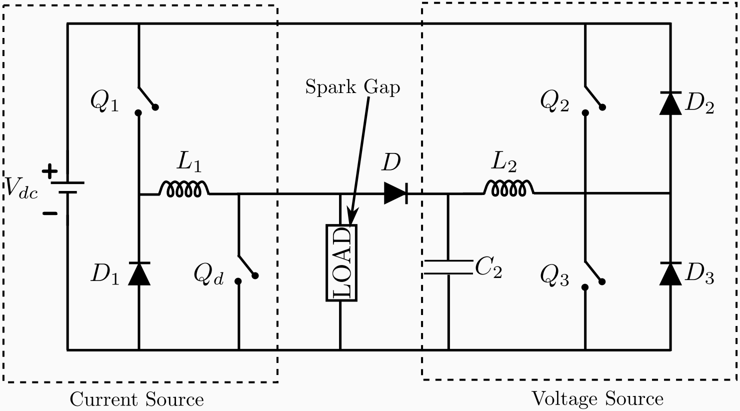


Figure 3: Converter topology for WEDM power supply [17]

Converter Modelling

Voltage Source Modelling

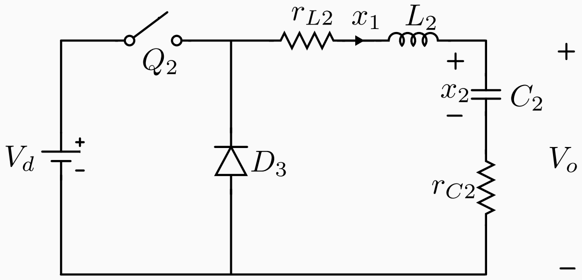


Figure 4: Simplified circuit of two quadrant converter used as voltage source

Voltage Source Modelling

1. State variables: $i_{L_2} \rightarrow x_1$, $v_{c_2} \rightarrow x_2$
2. Switch ON state $\rightarrow$ State equations (E1)
3. Switch OFF state $\rightarrow$ State equations (E2)
4. Time averaging (E1) and (E2)

$$\begin{aligned} \dot{x} &= [dA_1 + (1-d)A_2]x + [dB_1 + (1-d)B_2]V_d \\ V_o &= [dC_1 + (1-d)C_2]x \end{aligned} \tag{1}$$

5. Small signal perturbation in d
6. Get $\dfrac{\hat{v}_o(s)}{\hat{d}(s)}$

Voltage Source Modelling

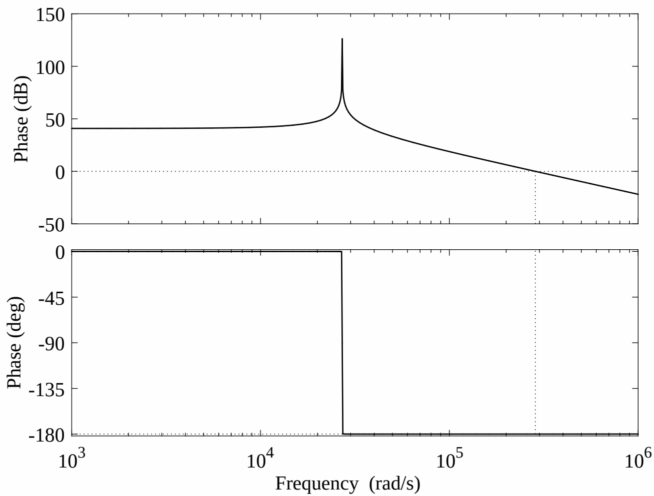


Figure 5: Bode plot of uncompensated transfer function of voltage source; Gm $= \infty$, Pm $= 0.0166^\circ$ (at 2.85e+05 rad/s)

Current Source Modelling

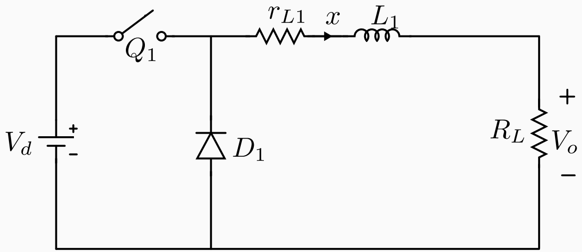


Figure 6: Simplified circuit of single quadrant converter used as current source

1. State variable: $i_{L_1} \to x$
2. Same steps as voltage source

$$\begin{aligned} \dot{x} &= [dA_1 + (1-d)A_2]x + [dB_1 + (1-d)B_2]V_d \\ I_o &= [dC_1 + (1-d)C_2]x \end{aligned} \tag{2}$$

3. Small signal perturbation in d
4. Get $\dfrac{\hat{i}_o(s)}{\hat{d}(s)}$

Current Source Modelling

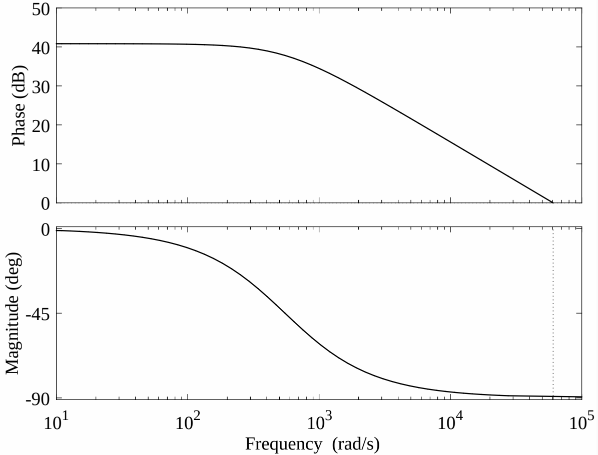


Figure 7: Bode plot of uncompensated current source transfer function; Gm $= \infty$, Pm $= 90.5^\circ$ (at 6.05e+04 rad/s)

Controller Design

Direct Duty Ratio Control

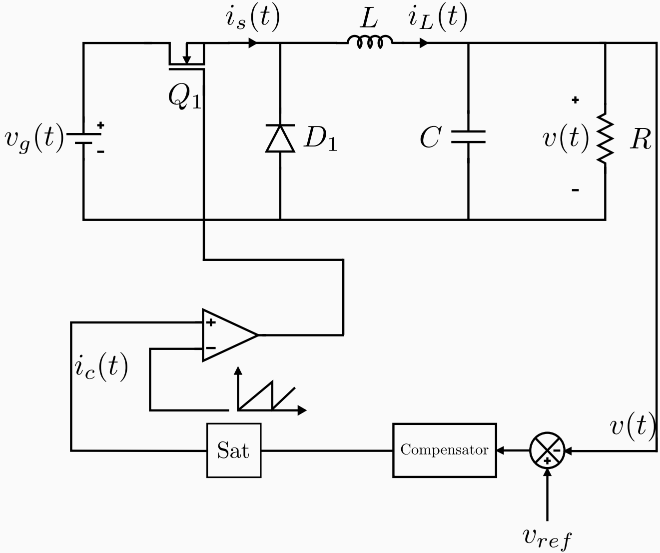


Figure 8: Direct duty ratio control of single quadrant converter

Direct Duty Ratio Control

1. Design lead compensator s.t.
   1.1 Gain crossover freq – high, less than F_s
   1.2 Phase margin between 45° to 60 $^\circ$
2. Check steady state error
3. Design lag compensator s.t.
   3.1 Max phase lag frequency $<<$ gain crossover frequency
   3.2 Sufficient gain is added at lower frequency
4. Balance loop gain at gain crossover

Direct Duty Ratio Control

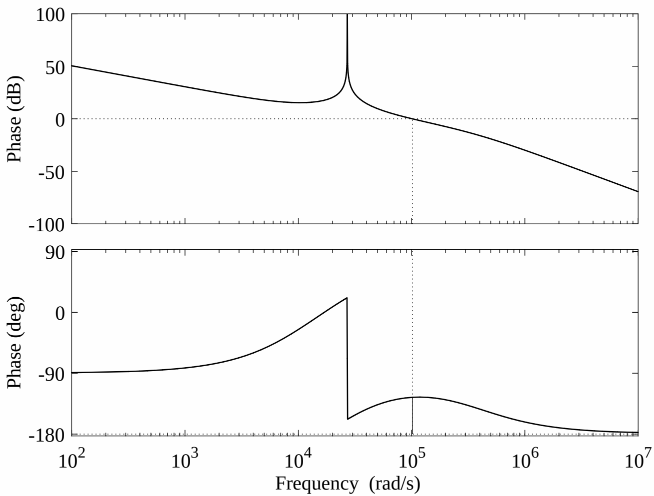


Figure 9: Bode plot of compensated transfer function of voltage source
Gm $= \infty$, Pm $= 54.3^\circ$ (at 1.02e+05 rad/s)

Result

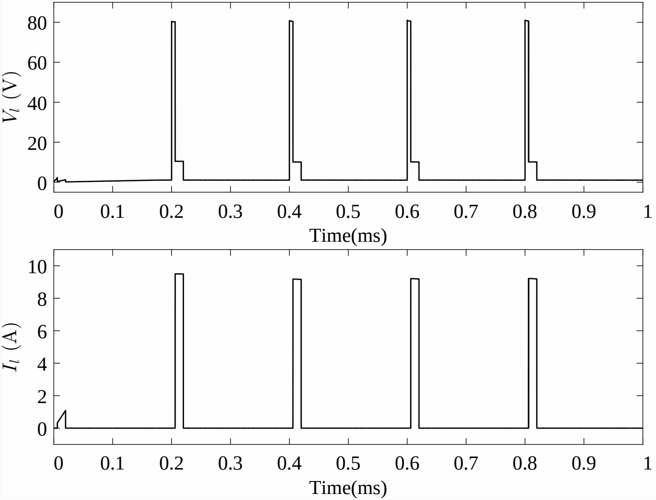


Figure 10: Load voltage and current - direct duty ratio control

Alternatives

Disadvantages of direct duty ratio control

- Separate protection circuit required
- Current sensors not utilized for control

Advantages of current mode control

- Inherent protection against over current
- First order model for voltage control

Disadvantages of current mode control

- Susceptible to noise

Current Mode Control

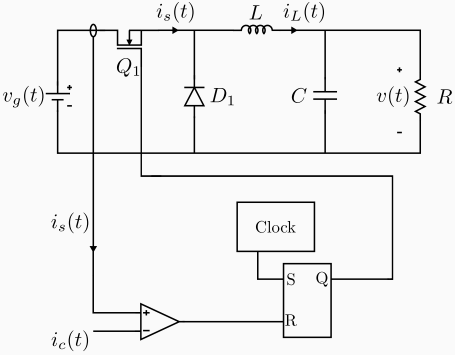


Figure 11: Current mode control of single quadrant converter

$$\frac{m_2}{m_1} = \frac{d}{1-d} \tag{3}$$

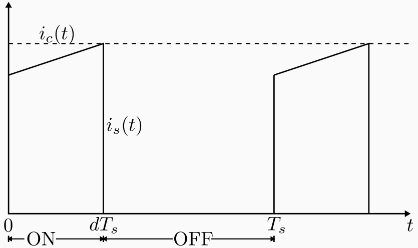


Figure 12: Switch current in current mode control

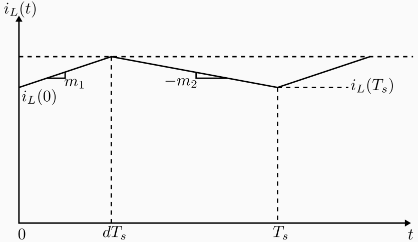


Figure 13: Inductor current in current mode control

Duty > 0.5

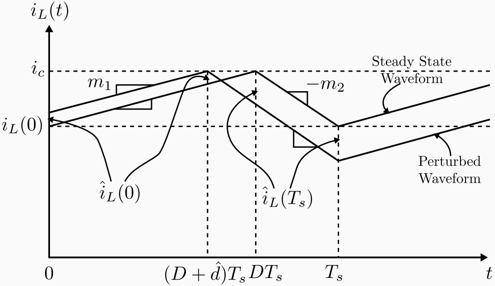


Figure 14: Inductor current in presence of disturbance

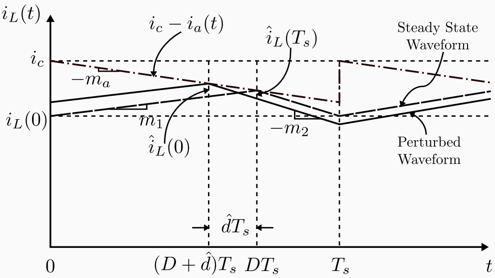


Figure 15: Inductor current with artificial ramp in presence of disturbance

Voltage control using current mode control

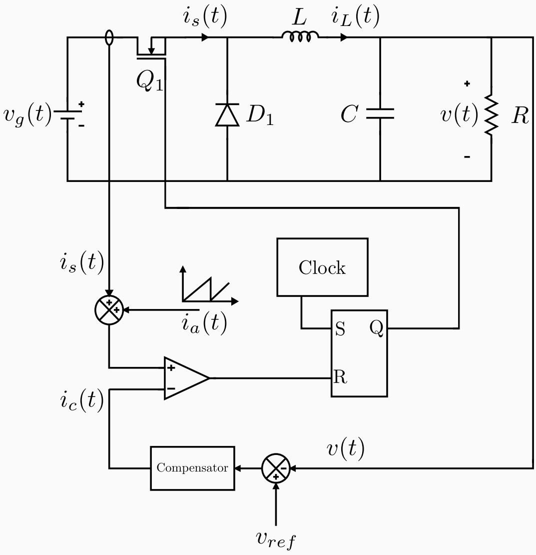


Figure 16: Controlled voltage source using current mode control

Modelling of voltage source

Assumption

Current mode controller operates ideally i.e average inductor current i_L to be identical to control i_c

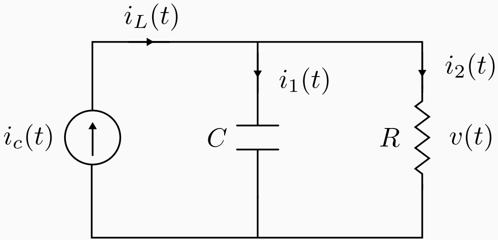


Figure 17: Current mode control replaced as current source in buck converter

$$\frac{\hat{v}(s)}{\hat{i}_c(s)} = \frac{R}{1 + sRC} \tag{4}$$

Current mode control

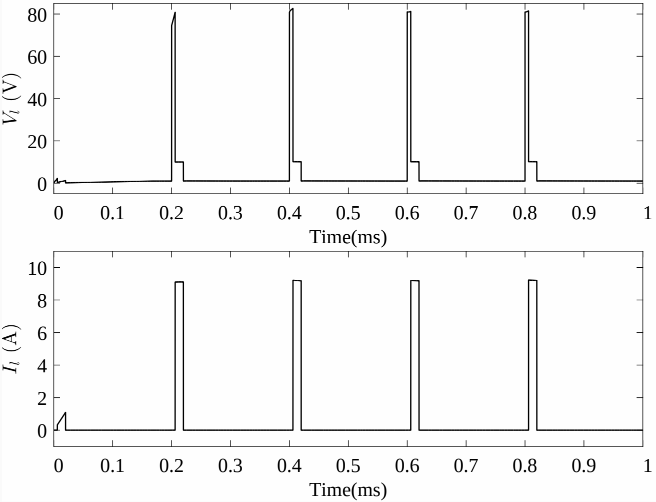


Figure 18: Load voltage and current - current mode control

Practical Considerations

Selection of inductors and capacitor

1. Inductor for current source → Output current ripple

$$\Delta I_L = \frac{V_{o1}}{L_1}(1-D)T_s \tag{5}$$

2. Inductor for voltage source → Maintaining continuous conduction mode

$$L_2 \geq 2.5\frac{DT_s}{I_{L_2}}(V_d - V_{\mathsf{ref}}) \tag{6}$$

3. Capacitor for voltage source → Output voltage ripple

$$C_2 \geq \frac{\Delta I_{L_2} T_s}{8\Delta V_{o2}} \tag{7}$$

Required device ratings

Device	V_{max}	I_{max}	P_{max}
Q_d	80 V	11 A	880 W
D	83 V	0.8 A	66.4 W
Q_1	110 V	11 A	1210 W
D_1	110 V	11 A	1210 W
Q_2	110 V	21 A	2310 W
D_2	110 V	4.5 A	495 W
Q_3	110 V	4.5 A	495 W
D_1	110 V	21 A	2310 W

Summary and Future Plan

Work Done

- Power supply topology fixed
- Converter modelled using time averaging
- Controller designed using
  - Direct duty ratio control – PI controller, lead-lag compensator
  - Current mode control
- Ratings passive components determined
- Snubber circuit designed for Q_d
- Simulated power supply
- Approximate ratings of switches determined

Future plan

Fabrication of Power Supply

- Designing gate drivers
- Designing and PCBs
- Fabricating power supply
- Testing of power supply – metal, silicon

Load Modelling

- Electrical characterisation of spark gap load
- Physical model R, L and C elements
- Fitting mathematical model

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Small signal transfer function of voltage source

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X \quad (8)$$

Small signal transfer function of current source

$$\frac{\hat{i}_o(s)}{\hat{d}(s)} = C[sI - A]^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X \quad (9)$$

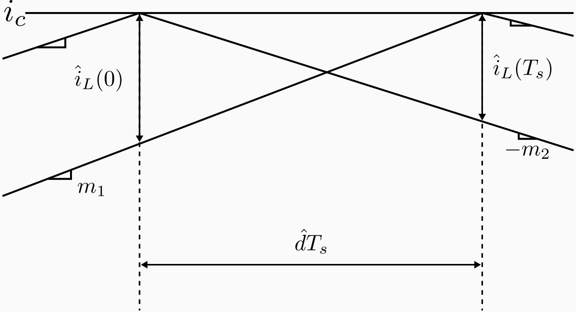

Figure 19: Expanded view of perturbed inductor current

$$i_L(nT_s) = i_L(0)\left(-\frac{D}{1-D}\right)^n \tag{10}$$

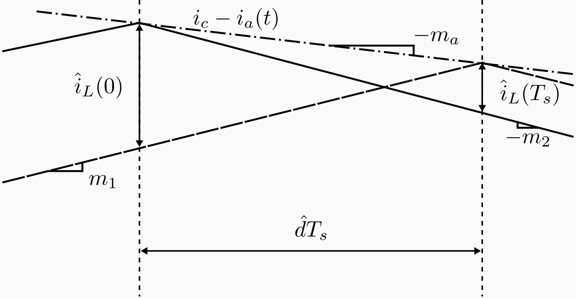

Figure 20: Expanded view of inductor current with artificial ramp in presence of disturbance

$$\hat{i}_L(nT_s) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n \tag{11}$$

$$\alpha = -\frac{1 - \dfrac{m_a}{m_2}}{\dfrac{1-D}{D} + \dfrac{m_a}{m_2}} \tag{12}$$