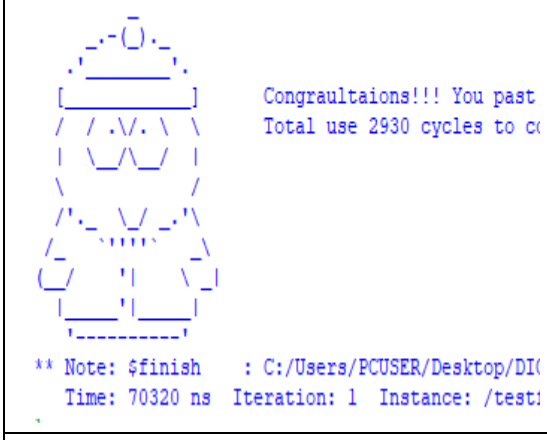
2023 Digital IC Design Homework 3

NAME	李亦軒
Student ID	E14091067

Simulation Result

Functional simulation	Score:100	Gate-level simulation	Score:100



Synthesis Result

Total logic elements	623
Total memory bits	0
Embedded multiplier 9-bit elements	1
Total cycle used	2930
Clock width	25

Flow Summary

<<Filter>>

Flow Status	Successful - Mon Apr 24 00:31:33 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AEC
Top-level Entity Name	AEC
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	623 / 55,856 (1 %)
Total registers	144
Total pins	19 / 325 (6 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

我設計的電路是利用 FSM 及 Datapath 的架構來實現，其中 FSM 有四個 state
READ:將測資讀進我設定的 buffer 中 ; POST:將 infix 轉 postfix;
POP:若在 POST 中遇到 precedence 狀況，進到 POP 並將 operator stack 中的運算元 pop 到 buffer 中; CALC: 將 postfix 的結果算出來。
另外，我利用組合電路的方式設計判斷 precedence 來判斷是否需要 pop 運算元。

*Scoring = Area cost * Timing cost*

*Area cost = Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used * Clock width*

*** Total logic elements must not exceed 1500.**