2023 Digital IC Design Homework 4

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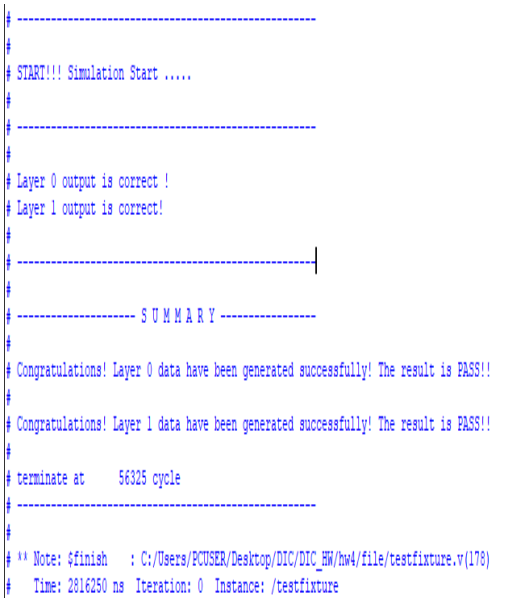
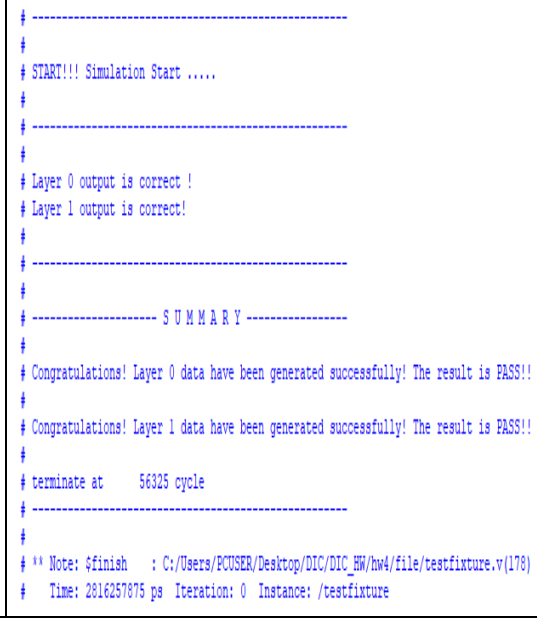
Simulation Result

Functional simulation	100	Gate-level simulation	100





Synthesis Result

Total logic elements	386
Total memory bits	0
Embedded multiplier 9-bit elements	0
Total cycle used	56325

Flow Summary

<<Filter>>

Flow Status	Successful - Mon May 22 13:08:47 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	386 / 55,856 (< 1 %)
Total registers	214
Total pins	82 / 325 (25 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	0 / 308 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

我設計了一有限狀態機來完成此次作業，其包含六個狀態：

1. IDLE： 等待 ready 訊號，ready 訊號拉 high 且 reset 訊號為 low 時進到 READ_IMAGE
2. READ_IMAGE： 一次讀取九個位置的 pixel 值，做完卷積與 RELU 後進到 WRITE_MEM0
3. WRITE_MEM0： 將結果寫入 Layer0 MEM 中，並回到 READ_IMAGE 中直到遍歷整張照片才會進到 READ_MEM0
4. READ_MEM0： 將 Layer0 的結果一次讀取四個出來，Max Pooling 後 round up 並進到 WRITE_MEM1
5. WRITE_MEM1： 將 round up 後的結果寫入 Layer1 MEM 並回到 READ_MEM0 直到遍歷整個 Layer0 MEM 才會進到 FINISH
6. FINISH： 歸零所有暫存器並回到 IDLE

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*

*** Total logic elements must not exceed 1000.**