SEM Imaging of an Integrated Circuit

Samuel Schmidt

MSCI 497

3/16/18

Introduction

I did my imaging of an integrated circuit (IC) specifically the Maxim DS80C400 Network Microcontroller that had been opened up to view its hardware. The purpose of this experiment was to discover the best methods to image an IC. A secondary goal was to identify some of the parts of the IC to reach a better understanding of the IC function and construction. I also wanted to try to see if I could image the transistor junctions. I was pretty sure it would be a long shot since the doping levels are in the parts per million

Instruments used

I used the secondary electron (SE) detector to get surface topography images. This works by collecting the electrons that get knocked out of the sample from the incoming primary electrons. The electrons are collected and turned into photons which are then turned into a surface image.

I also used the Back Scatter Electron (BSE) detector which detects electrons that are bent around the nucleus of the atoms. Because of the interaction with the nucleus heavier elements show up as brighter spots.

Finally I used the EDS detector. When an incoming electron knocks out an electron from an atom a higher energy electron drops down to take its place releasing an x-ray at specific energies to the element it came from. These specific energies are used to determine the elemental make up of an area.

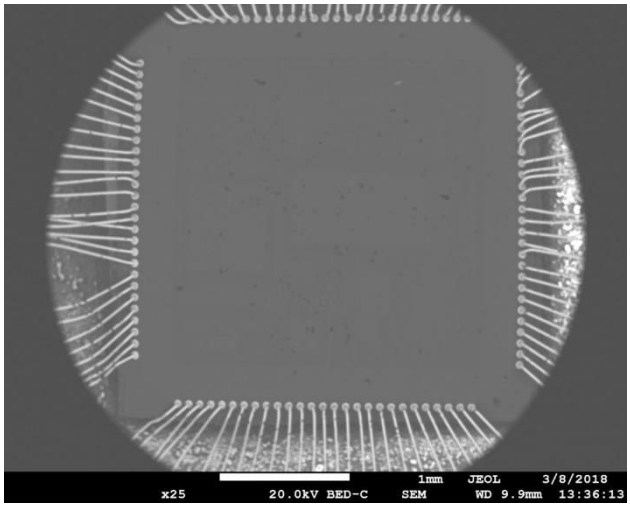
Sample Prep

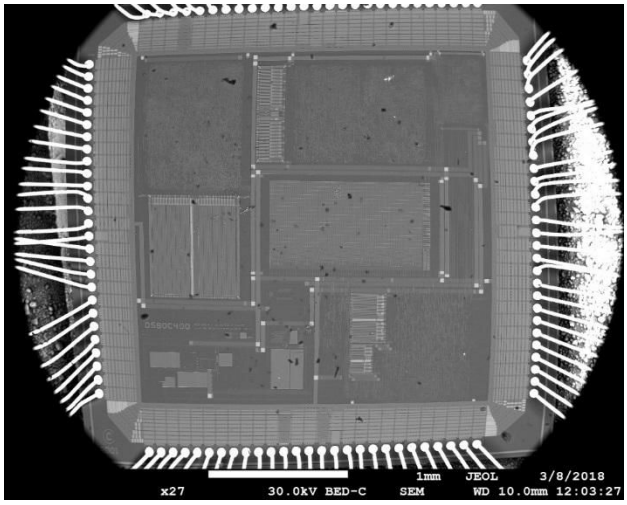
First the specimen had to be prepped for the SEM. The first step was to expose the actual IC hardware that was underneath the plastic casing. The majority of the plastic was removed with an abrasive rotary wheel. The remaining plastic material was removed using hydrofluoric acid (HF). This was used because HF will also remove the silicon dioxide glass layer that tops the hardware exposing the actual components to inspection. Great care needed to be taken with the HF as it is extremely dangerous to use.

Imaging Conditions

Initially the microscope was set up with an accelerating voltage of 20kV a working distance (WD) of 10mm and a probe current (PC) of 9. The 10mm WD was chosen because it gave the optimal angle for EDS to pick up the most x-ray counts. The PC was chosen to boost the EDS counts to the desired range. The 20 kV accelerating voltage was changed to 30 kV because it showed better BSE images as it was able to penetrate past any remaining silicon dioxide layers as seen in the following images. When first

imaging with the secondary electron detector at 20 kV a lot of charging was happening which kept any good images from being taken. I removed the sample and applied more carbon paste to the IC feet to make sure there was a good connection. This greatly helped decrease the charging that was first seen.





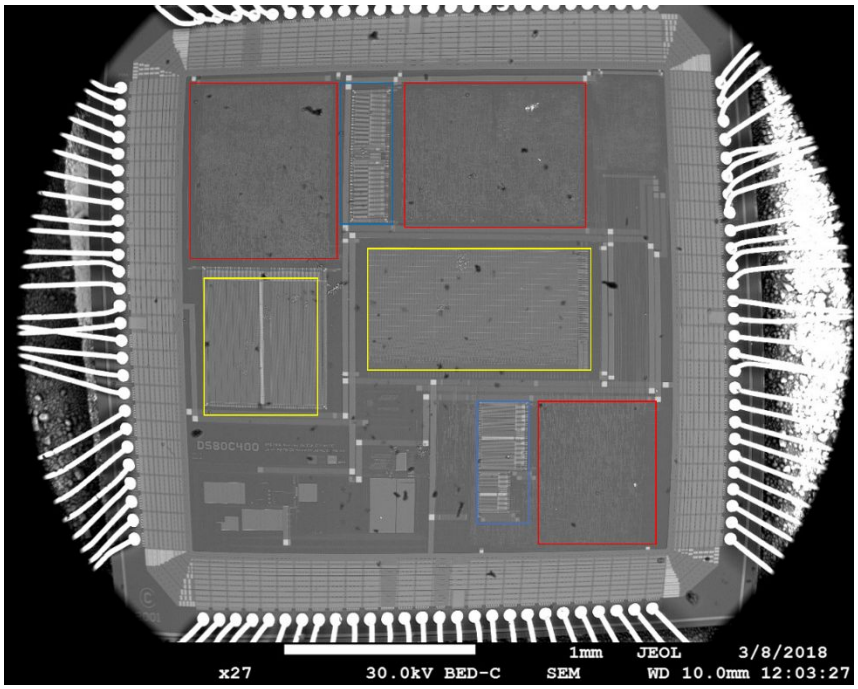
BSE image at 20kV (barely visible) BSE image at 30kV (readily visible)

Future experiments

If I has more time there are a few more experiments I would like to try involving the EDS and further sample prep. First I would like to do more EDS imaging but try to filter out the pervasive silicon and oxygen to see if any small spikes might show up. I also would want to make an EDS map of aluminum and tungsten to see if it would show up in specific areas of the IC over others. I did not do this at first because I thought I was getting equal amounts of aluminum and tungsten everywhere but on closer analysis of the spectrum data I realized there were at least two distinct values for aluminum and tungsten. I would also like to prep my sample in some different ways. One would be to introduce more HF to the top layer to see if I could image buried layers. A second idea I had would be to cut off a cross-sectional slice of the IC to see all the layers at once.

Conclusion

The best methods for IC imaging were discovered in this experiment through careful consideration and practice. While SE images showed some details and surface features BSE imaging showed much better detail and distinction between parts and was decided as the best detection method to use. Three main features were detected the transistor connections area, the data storage area, and the analog devices area. The transistor connections area took up the majority of the board as transistors are the workhorse of an IC. I was surprised that the data storage areas were just straight lines but I realized that was because they were connecting to linear grids of bits and words (binary data). The existence of the analog areas was interesting especially to study the way they turn 3 dimensional components into practically 2 dimensional components when implementing them on such a small flat chip. I also noticed a fair amount of bright small squares upon further inspection I realized these were through holes that acted as connections between the many layers. The imaging showed that at the top layer where we are looking it is mostly interconnect that goes down to the transistor layer where the real work is done. The EDS showed that the IC is made primarily of silicon with interconnect made of aluminum and tungsten. It also showed that a thin layer of silicon dioxide still covered the IC. I was unable to get any EDS data on possible doping agents I believe this was because doping is in the parts per million which is outside of the capabilities of the EDS to detect. Possible real world uses of IC SEM imaging are fault detection, device identification, and reverse engineering feasibility.



BSE Image of IC: Red is transistor interconnect; Yellow is data storage fields; Blue is analog circuit areas.