Part I – Common Source Amplifier

(1) DC Sweep

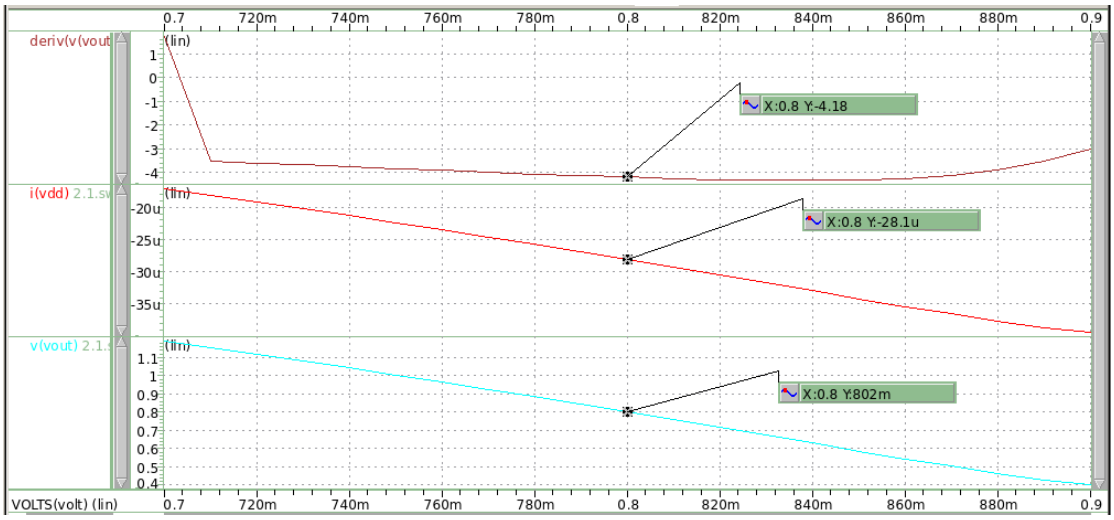

Fig. 1 Common Source Amplifier

Top: X-axis: V_{in} (V) Y-axis: derivative of V_{out} (V/V)

Mid: X-axis: V_{in} (V) Y-axis: I_D (A)

Down: X-axis: V_{in} (V) Y-axis: V_{out} (V)

Derivative of V_{out} = - 4.18(V/V)

I_D = 28.1 uA

V_{out} = 802mV

(2) TF Analysis

```
****     small-signal transfer characteristics

    v(vout)/vin                              =   -4.2110
    input resistance at             vin      =  1.000e+20
    output resistance at v(vout)             =   33.1222k
```

Yes, the DC gain A_v is close to the result in (1). Neglecting other nonideal effects, the DC gain $A_v = -g_m * R_D$ where $g_m = \frac{\partial ID}{\partial Vov}$. Thus we can we write the later equation to $-g_m * R_D = -\frac{\partial ID}{\partial Vov} * R_D = \frac{\partial(-ID*RD)}{\partial Vov} = \frac{\partial(VDD-ID*RD)}{\partial(Vin-Vth)} = \frac{\partial Vout}{\partial Vin}$

since V_{DD} and V_{th} is constant. From above math deduction, we can get the conclusion that if we want to get the DC gain, we don't bother to calculate V_{out}/V_{in} but we also have another approach by derivate V_{out} with V_{in}.

(3) Hand Calculation and Discussion

```
**** mosfets


subckt
element  0:mn
model    0:n_18.1
region   Saturation
 id        28.1149u
 ibs     -7.399e-21
 ibd     -131.8893a
 vgs      800.0000m
 vds      801.9205m
 vbs        0.
 vth      395.3452m
 vdsat    334.3371m
 vod      404.6548m
 beta     401.6412u
 gam eff  507.4472m
 gm       127.1657u
 gds        2.0227u
 gmb       24.0628u
 cdtot      1.8127f
 cgtot      8.9516f
 cstot     10.1795f
 cbtot      4.9404f
 cgs        7.8931f
 cgd      465.4772a
```

```
****     small-signal transfer characteristics

    v(vout)/vin                               =   -4.2110
    input resistance at            vin        =  1.000e+20
    output resistance at v(vout)              =   33.1222k
```

```
**** resistors

subckt
element  0:r
 r value    35.5000k
 v drop    998.0795m
 current    28.1149u
 power      28.0609u
```

Gain $A_V = -g_m * R_D = -4.514$ V/V error: 7.5%

$V_{out,DC} = V_{DD} - I_D * R_D = 0.8019$ V error: 0%

Output impedance $R_{out} = R_D || R_o = R_D || (1/g_{ds}) = 33.121k\Omega$ error: 0%

TABLE I

COMMON SOURCE PERFORMANCE TABLE

Working Item	SPEC	Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	0.8V	0.8V	0.8V
$V_{out,DC}$	0.8V	802mV	802mV
Gain A_V	> 3.2(V/V)	4.2(V/V)	4.5(V/V)
R_D	< 90KΩ	35.5KΩ	-
I_D	< 30μA	28.1μA	-
M_S W/L	-	1.3(m/m)	-

Design and Result discussion

When I designed this common source amplifier, I opened the AIC handout to check the equation we need first. Then, I set my channel length 1um to prevent the undesirable effect due to the short channel effect.

I thought the most difficult thing is to keep the output bias at 0.8V. Therefore, I set R_D to 10K and change the W/L to get desire output bias. However, the current was over the spec.

Thus, there are two main equations:

1. $A_V = -g_m * R_D$ where $g_m \alpha (W/L)$ since V_{ov} is constant in this case
2. $\Delta V = V_{DD} - V_{out,DC} = I_D * R_D$ where $I_D \alpha (W/L)$

From these two equations, I simply calculated what proportion I needed to hold the output bias by rising my R_D when reducing the W/L (proportional to I_D). After some tests, I got the result on the Table1. Besides I didn't overcome the problem that the voltage gain didn't meet the spec in the question.

In this lab, we can conclude that in common source stage, output bias, voltage gain and output impedance we calculated is closed to the simulation result. However, the error of output impedance is much larger. I think the reason is that I don't consider the MOS output impedance. Thus, I revise the equation $A_V = -g_m * R_D$ to $A_V = -g_m * R_{out}$. Then, we get the DC gain $A_V = 4.212$, it is almost the same as the V_{out}/V_{in}.

Part II – Common Gate

1. DC Sweep

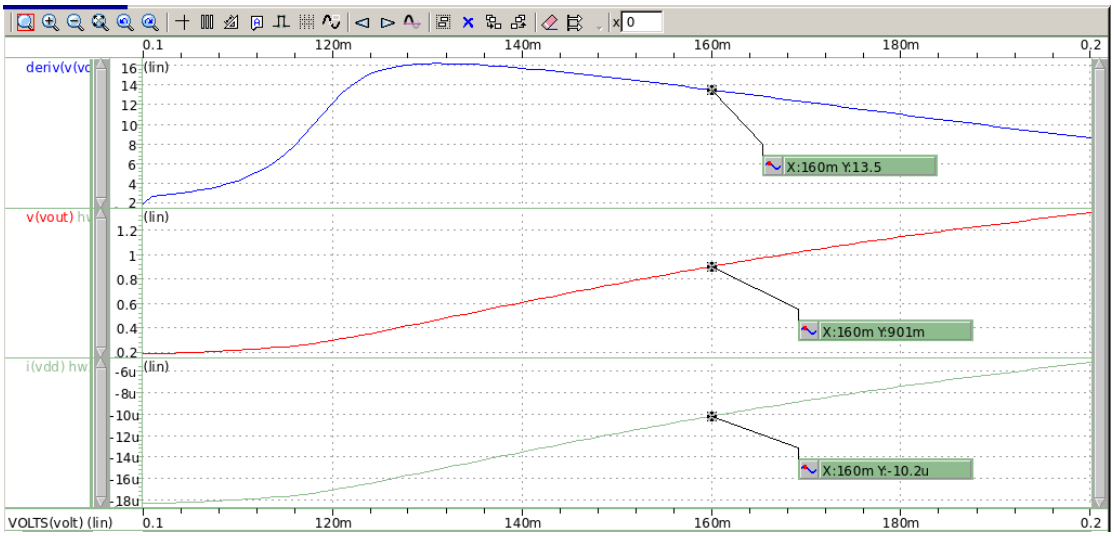

Fig. 2 Common Gate Amplifier

Top: X-axis: V_{in} (V) Y-axis: derivative of V_{out} (V/V)

Mid: X-axis: V_{in} (V) Y-axis: V_{out} (V)

Down: X-axis: V_{in} (V) Y-axis: I_D (A)

Derivative of V_{out} = 13.5(V/V)

V_{out} = 901mV

I_D = 10.2 uA

2. TF Analysis

```
****     small-signal transfer characteristics

v(vout)/vin                              =   13.4401
input resistance at             vin      =    6.5476k
output resistance at v(vout)             =   75.3973k
```

Yes, the DC gain A_v is close to the result in (1). Using the same method as we do in CS stage.

$$g_m{*}R_D = \frac{\partial ID}{\partial Vov} * R_D = \frac{\partial (ID{*}RD)}{\partial Vov} = \frac{\partial (-VDD + ID{*}RD)}{\partial ((Vb - Vin) - Vth)} = \frac{\partial Vout}{\partial Vin}$$

since V_{DD},V_b and V_{th} is constant. From above math deduction, we can get the conclusion that if we want to get the DC gain, we don't bother to calculate V_{out}/V_{in} but we also have another approach by derivate V_{out} with V_{in}.

3. Hand Calculation and Discussion

```
**** mosfets

subckt
element  0:mn
model    0:n_18.1
region   Saturation
 id        10.2140u
 ibs     -1.653e-21
 ibd     -576.6269a
 vgs      440.0000m
 vds      741.1678m
 vbs        0.
 vth      384.2957m
 vdsat     90.3048m
 vod       55.7043m
 beta       3.1078m
 gam eff  507.4460m
 gm       176.3657u
 gds        1.8995u
 gmb       36.0674u
 cdtot     13.2177f
 cgtot     63.7850f
 cstot     70.4911f
 cbtot     37.3373f
 cgs       53.6332f
 cgd        3.5795f
```

```
****     small-signal transfer characteristics

    v(vout)/vin                              =    13.4401
    input resistance at            vin       =     6.5476k
    output resistance at v(vout)             =    75.3973k

            **** resistors

            subckt
            element  0:r
             r value    88.0000k
             v drop    898.8322m
             current    10.2140u
             power       9.1807u
```

Gain $A_V = g_m * R_{out} = 13.27$ V/V error: 1.26%

$V_{out} = V_{DD} - I_D * R_D = 0.9012$ V error: 0.01%

Output impedance $R_{out} = R_D || R_o = R_D || (1/g_{ds}) = 75.24k\Omega$ error: 0.2%

Input impedance $R_{in} = (1/g_m) = 5.67k\Omega$ error: 13.4%

TABLE II

COMMON GATE PERFORMANCE TABLE

Working Item	SPEC	Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	0.16V	0.16V	0.16V
$V_{out,DC}$	0.9V	901mV	901mV
Gain A_V	> 10(V/V)	13.4(V/V)	13.3(V/V)
R_D	< 90KΩ	88KΩ	-
I_D	< 30μA	10.2μA	-
V_b	-	0.6 V	-
M_b W/L	-	10(m/m)	-

Design and Result discussion

First, the error of output impedance is too much. Thus, we need to take the channel length modulation into account. Rewriting the input impedance equation to

$$R_{in} = \frac{1}{gm} + \frac{RD}{gm*ro} = 5.67k\Omega + 947.8\Omega = 6.618\ k\Omega \quad error=1.07\%$$

(we can find this equation in the microelectronic lecture)
The revised error is more acceptable than the old one.

In this common gate amplifier design, I think the most difficult spec to achieve is to get the higher gain with lower I_D. That is, if we want to get the higher gain, the current will be over the spec easily. Using the same method, I write down the equations below.

1. $A_V = g_m * R_D$ where $g_m \alpha (W/L)$ when V_{ov} is constant
2. $I_D \alpha (W/L) * V_{ov}^2$
3. $\Delta V = V_{DD} - V_{out,DC} = I_D * R_D$

Since we want to lower the current to meet the spec but we also need to get the higher gain, we must lower the overdrive voltage V_{ov} to decease the current and rise the value of W/L to get the higher gain.(because I_D is more sensitive to V_{ov} due to square law) Thus, I tried to set the V_b to 0.6 V and it led to the sufficient small current to meet the spec. After that, I set the W/L to 10. Fortunately, I got the DC gain about 13.4 and met all the spec.

Part III – Source Follow

(1) DC Sweep

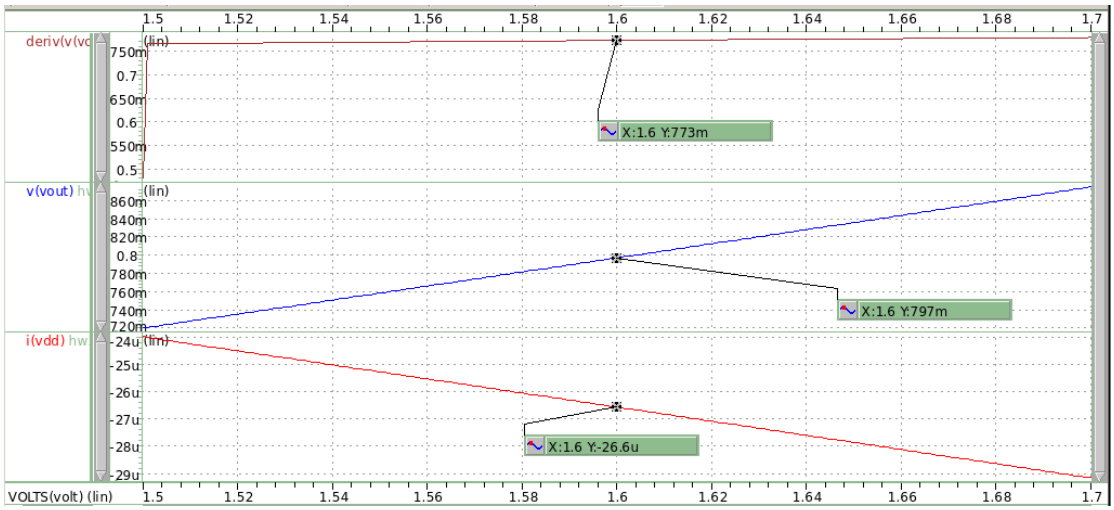

Fig. 3 Source Follow

Top: X-axis: V_{in} (V) Y-axis: derivative of V_{out} (V/V)

Mid: X-axis: V_{in} (V) Y-axis: V_{out} (V)

Down: X-axis: V_{in} (V) Y-axis: I_D (A)

Derivative of V_{out} = 0.773(V/V)

V_{out} = 797mV

I_D = 26.6 uA

(2) TF Analysis

```
****     small-signal transfer characteristics

    v(vout)/vin                              =  772.9930m
    input resistance at            vin       =  1.000e+20
    output resistance at v(vout)             =    6.4898k
```

The DC gain A_v is actually the same as the result in (1). Using the same method as we do in CS stage. Thus, we can we rewrite the equation to

$$\frac{\partial \text{Vout}}{\partial Vin} = \frac{\partial(ID*\text{Reff})}{\partial(ID*\text{Reff}+\text{Vth}+\text{Vov})} = \frac{\partial(ID*\text{Reff})}{\partial(ID*\text{Reff}+\text{Vov})} = \frac{\partial(ID*\text{Reff})/\partial(Vov)}{\partial(ID*\text{Reff}+\text{Vov})/\partial(Vov)}$$

$$= \frac{\text{Reff}*\partial(ID)/\partial(Vov)}{\text{Reff}*\partial(ID)/\partial(Vov)+\partial(\text{Vov})/\partial(Vov)} = \frac{\text{Reff}*gm}{\text{Reff}*gm+1} = \frac{\text{Reff}}{\text{Reff}+1/gm} \text{ where } R_{eff} = R_L||R_o$$

since V_{th} is constant. From above math deduction, we can get the conclusion that if we want to get the DC gain, we don't bother to calculate V_{out}/V_{in} but we also have another approach by derivate V_{out} with V_{in}.

(3) Hand Calculation and Discussion

```
**** mosfets

subckt
element  0:mn
model    0:n_18.1
region   Saturation
 id        26.5623u
 ibs      -7.248e-21
 ibd      -157.9096a
 vgs       803.1304m
 vds         1.0031
 vbs         0.
 vth       394.7374m
 vdsat     337.2298m
 vod       408.3930m
 beta      370.4768u
 gam eff   507.4472m
 gm        119.1390u
 gds         1.6462u
 gmb        22.4235u
 cdtot       1.6236f
 cgtot       8.2582f
 cstot       9.4026f
 cbtot       4.5285f
 cgs         7.2783f
 cgd       426.5870a

****     small-signal transfer characteristics

      v(vout)/vin                              =  772.9930m
      input resistance at            vin       =  1.000e+20
      output resistance at v(vout)             =    6.4898k


                        **** resistors

                        subckt
                        element  0:r
                         r value    30.0000k
                         v drop    796.8696m
                         current    26.5623u
                         power      21.1667u
```

Gain $A_V = \frac{RL||Ro}{RL||Ro+1/gm} = 0.773$ V/V error: 0%

$V_{out} = I_D * R_L = 0.797$ V error: 0%

Output impedance $R_{out} = R_L \,||\, R_o \,||\, \frac{1}{gm} = 6.4885k\Omega$ error: 0.02%

TABLE III

SOURCE FOLLOWER PERFORMANCE TABLE

Working Item	SPEC	Design	Hand Calculation
V_{DD}	1.8V	1.8V	1.8V
$V_{in,DC}$	1.6V	1.6V	1.6V
$V_{out,DC}$	0.8V	797mV	797mV
Gain A_V	> 0.75(V/V)	0.773 (V/V)	0.773 (V/V)
R_S	< 90KΩ	30KΩ	-
I_D	< 30μA	26.6μA	-
M_d W/L	-	1.2(m/m)	-

Design and Result discussion

When I conduct the TF analysis, I have considered the channel length modulation. All the error I calculated are negligible.

In this common gate amplifier design, the most difficult spec is to keep output bias at 0.8V but the current may not over 30uA. From the experience, write down the equations that we may use.

1. $I_D \alpha (W/L) * V_{ov}^2$
2. $V_{ov} = (V_{in}\text{-}I_D*R_S\text{-}V_{th})$
3. $V_{out} = I_D*R_S$

From the above equations, we can believe that V_{ov} be the constant due to the spec requiring us to set the V_{out} to 800mV. Thus, to meet the spec, we may lower the I_D by reducing the value of (W/L) and increasing R_s to maintain V_{out}. In fact, when I first try this problem, I use R_s = 88KΩ (the same as CG stage). However, this R is too big to make V_{out} 0.8V. After some test, I set the Rs to 30KΩ meeting the current spec but the gain is closed to 0.75. So, I increase the W/L to increase the DC gain with care to keep the current lower than 30uA.