EE3235 Analog Integrated Circuit Analysis and Design I

Homework 1

Process Analysis

Due date: 2023.10.11 (Wed.) 23:30 (upload to eeclass system)

In this homework, you are to run HSPICE and evaluate the device performance with threshold voltage V_{th}, transconductance g_m, output conductance g_{ds}, saturation drain voltage V_{dsat}, intrinsic gain $g_m r_O$, power efficiency g_m/I_D, speed g_m/C_g, drain current I_D, and body effect as the benchmarks.

Suppose V_{DD}=1.8V, temperature=25°C, TT corner in this homework.

Please note that:

1. **No delay allowed**.
2. Please hand in your report using eeclass system.
3. Please generate your report with **pdf** format, name your report as HWX_studentID_name.pdf.
4. Please hand in the spice code file (.sp) for each work. Do not include output file.
5. Please print waveform with white background, and make sure the X, and Y labels are clear.
6. Please do not zip your report.

Part I – Analyze with Diode Connected Structure

In part I, consider the schematic shown in Fig. 1. Please keep the bias current constant and sweep the channel length of M_{thn} and M_{thp} from 0.18μm to 10μm with a step of 0.01μm. Please probe the following parameters of M_{thn} and M_{thp} with respect to the channel length. Discuss your observations. (9 graphs, 18 curves)

(1) Threshold voltage V_{th}. (plots of graphs for TT、SS、FF corners)

(2) Transconductance g_m.

(3) Output conductance g_{ds}.

(4) Saturation drain voltage V_{dsat}.

(5) Intrinsic gain $g_m r_O$.

(6) Power efficiency g_m/I_D.

(7) Speed g_m/C_g.

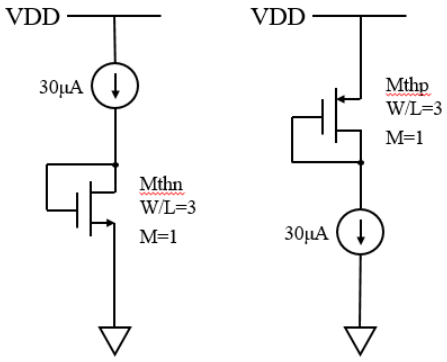

Fig. 1. Diode-connected.

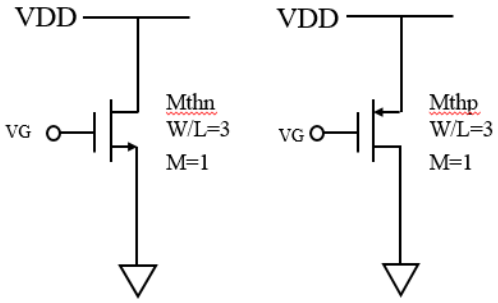

Fig. 2. Drain current.

Part II – Drain Current I_D

As shown in Fig. 2, please run DC analysis with V_G from 0V to 1.8V with a step of 0.01V, then sweep the channel length of M_{idn} and M_{idp} from 1.8μm to 10μm with a step of 1.8μm. Probe I_D v.s. V_G with different channel lengths of M_{idn} and M_{idp}. Discuss your observations. (2 graphs, 10 curves)

Part III – Body Effect

We often assumed that the source and the body of a single transistor are connected, such that the threshold voltage V_{th} remains a constant while V_s varies, however, for a p-substrate process, all native transistors share the same body, and Vth varies with V_{SB}.

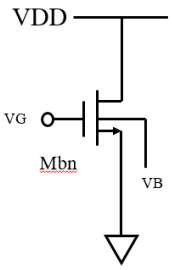

Fig. 3. Body effect.

(1) For Mbn , given that VDD =1.8V, V_g =0.7V, V_s = V_B =0V, find a correct size when the drain current equals to 30μA(±1μA is allowed, and longer channel length is recommended in order to minimize the effect of channel length modulation)

(2) Use the size derived above, sweep V_s from 0V to 1V with a step of 1mV, while V_{gs}, V_B and VDD fixed. Probe I_D v.s. V_s, V_{th} v.s. V_s and gm v.s. V_s. Discuss your observations. (3 graphs, 3 curves)

(3) Repeat the steps in (2), but this time with the source and the body connected. Compare the difference, discuss your observation and explain the cause.(3 graphs, 6 curves)

Please refer to the following examples to print your waveform.

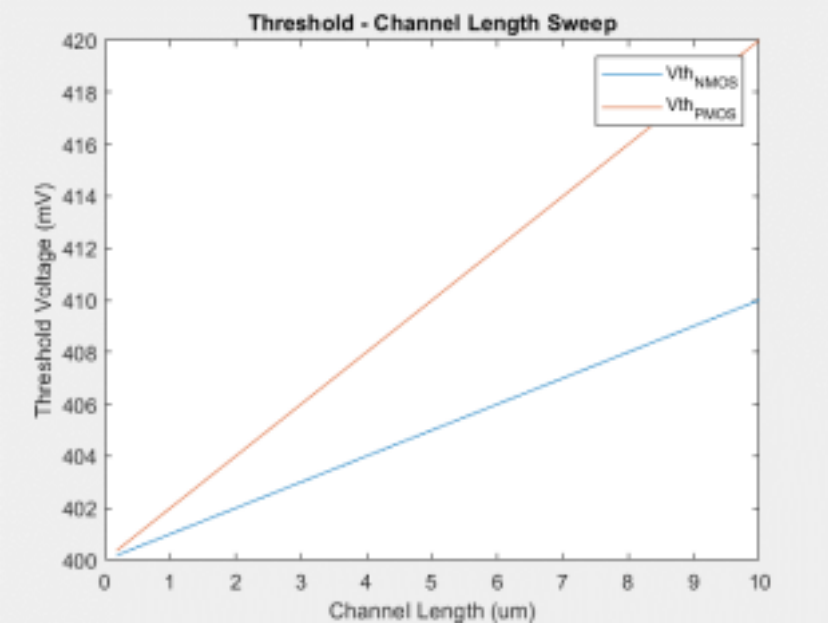

Fig. 4. Example waveform of part I

Please plot the parameters of NMOS and PMOS in a single graph, there will be 9 graphs in part I.

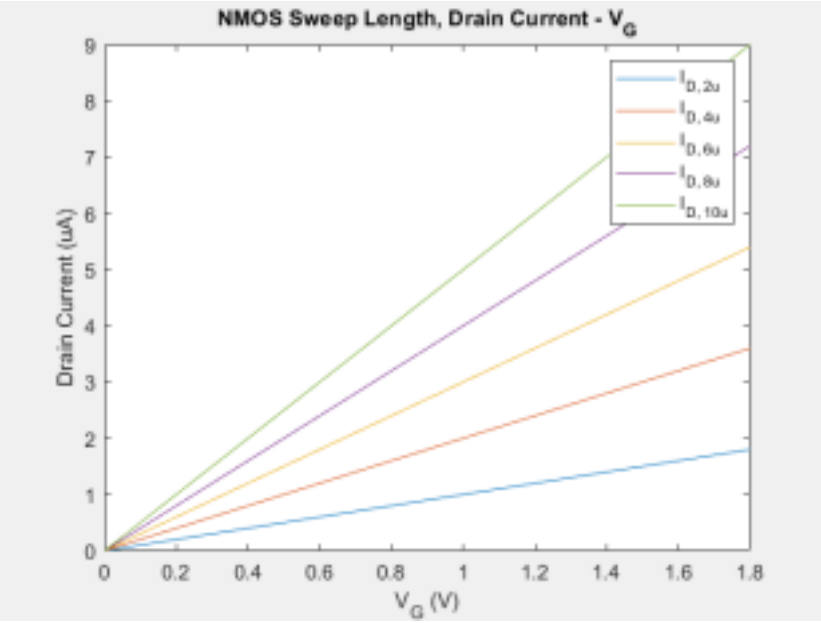

Fig. 5. Example waveform of part II

Please plot the drain currents with different channel length in a single graph, there will be 2 graphs in part II, which are for NMOS and PMOS, respectively.

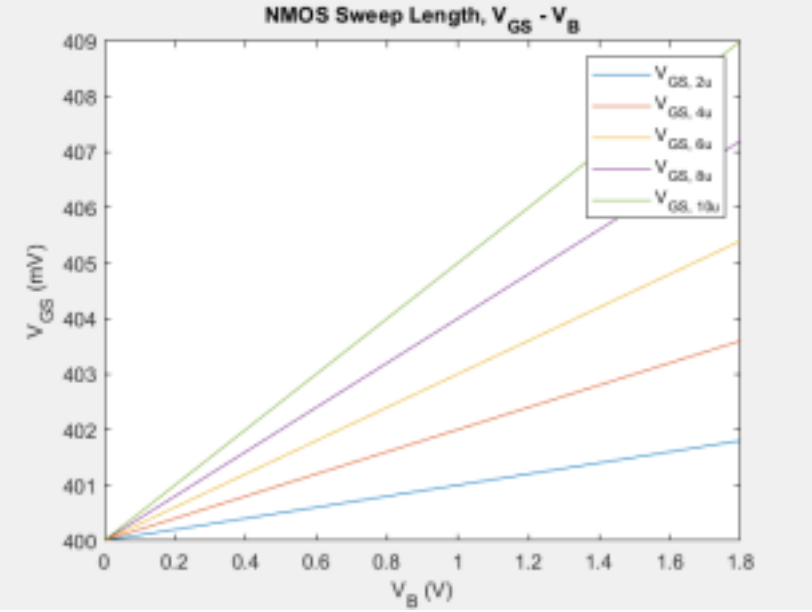

Fig. 6. Example waveform of part III

Please plot or with different channel length in a single graph, there will be 4 graphs in part III, which are for and of NMOS and PMOS, respectively.