

Lab 3: Counters and Shifters I

Objective

- ✓ Review synchronous sequential circuits.
- ✓ Review counter and shift register logics.

Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Clocking concepts
- ✓ Logic modeling in Verilog HDL.

Pre-labs

- 1 Consider a 4-bit synchronous binary up counter ($q_3q_2q_1q_0$).
 - 1.1 Draw the logic diagram
 - 1.2 Construct Verilog RTL representation for the logics with verification.
- 2 Cascade eight DFFs together as a shift register. Connect the output of the last DFF to the input of the first DFF as a ring counter. Let the initial value of DFF output after reset be 01010101. Construct the Verilog RTL representation for the logics with verification.

Experiments

- 1 Frequency Divider: Construct a 27-bit synchronous binary counter. Use the MSB of the counter, we can get a frequency divider which provides a $1/2^{27}$ frequency output (f_{out}) of the original clock ($f_{crystal}$, 100MHz). Construct a frequency divider of this kind.
 - 1.1 Write the specification of the frequency divider.
 - 1.2 Draw the block diagram of the frequency divider.
 - 1.3 Implement the frequency divider with the following parameters.

I/O	$f_{crystal}$	f_{out}
Site	W5	U16

- 2 Frequency Divider: Use a count-for-50M counter and some glue logics to construct a 1 Hz clock frequency. Construct a frequency divider of this kind.
 - 2.1 Write the specification of the frequency divider.
 - 2.2 Draw the block diagram of the frequency divider.
 - 2.3 Implement the frequency divider with the following parameters.

I/O	$f_{crystal}$	f_{out}
Site	W5	U16

- 3 Implement pre-lab1 with clock frequency of 1 Hz. Use the following I/O to demonstrate the counter results.

I/O	$f_{crystal}$	q_3	q_2	q_1	q_0
Site	W5	V19	U19	E19	U16

- 4 Implement pre-lab2 with clock frequency of 1 Hz. The I/O pins can be assigned by yourself.
- 5 Use the idea from pre-lab2. We can do something on the seven-segment display. Assume we have the pattern of E, H, N, T, U for seven-segment display as shown below. Try to implement the scrolling pre-stored pattern "NTHUEE2023" with the four seven-segment displays.

