EE3230 VLSI Design HW #2 **2023 Fall**

Due date: 2023/11/06 (Monday) 10am

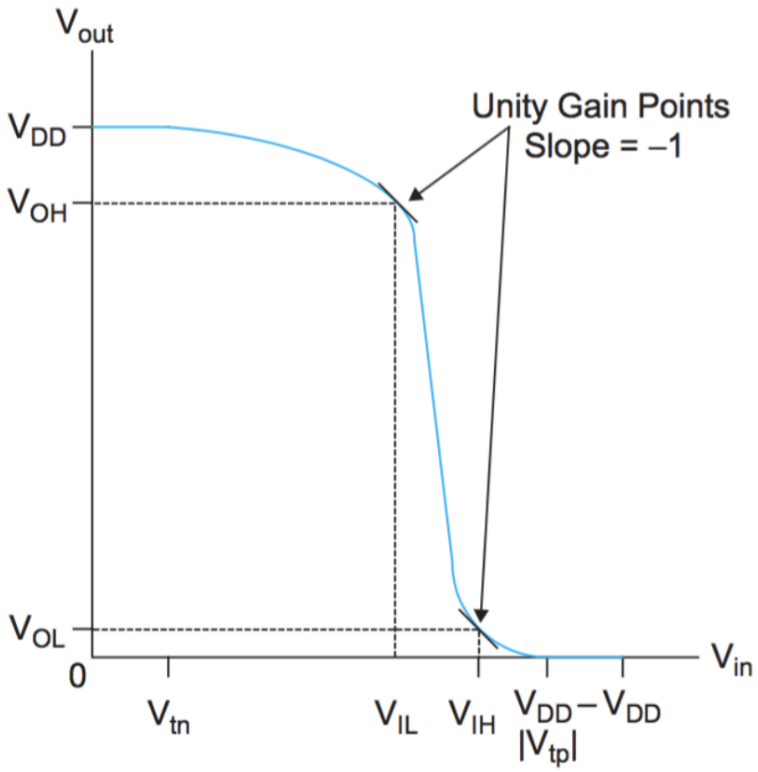
Plagiarism is strictly prohibited. While you may engage in discussions with your peers, the homework must be completed individually by each student.

Run HSpice simulations to answer the following questions.
In your simulations, don't forget to connect the substrates for all the PMOSs and NMOSs are connected to V_{DD} and ground, respectively.

Set V_{DD} to 1.8V.
In your report, set the unit to mV/μm/ps/ohm with 2-digit precision.

1. (25%) Please design an inverter using an NMOS of $(W/L)_N = 1.2\,\mu m/0.2\,\mu m$ and a load resistor. Set the simulation corner to TT, 25°C.
    a. Find and report the resistance such that the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is also $0.5 \cdot V_{DD}$.
    b. Find V_{out} when $V_{in} = V_{DD}$. What is the NMOS operating region in this case, and what is the current flowing through the inverter?

    c. Increase the resistance by 2 times. Do you expect the transition point (of the V_{out} vs. V_{in} plot) to shift to the left or right, why?
    d. Simulate and plot the DC voltage transfer curve of this inverter (from Q1-c) as V_{out} vs. V_{in} with steps of 10 mV. Find $V_{in} = V_{in0}$ when $V_{out} = 0.5 \cdot V_{DD}$. On your plot, label where ($V_{in} = V_{in0}$, $V_{out} = 0.5$) clearly.
    e. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1 as shown with the figure below. You may need to repeat Q1-d with finer steps.
    f. What are the noise margins NM_L and NM_H of your design?



2. (30%) Please design a CMOS 3-input NAND gate. Use the same NMOS size as in Q1 and size the PMOS such that, with the three inputs all set to V_{in}, the transition point happens at $V_{out} = 0.5 \cdot V_{DD}$ when V_{in} is also $0.5 \cdot V_{DD}$.

   All three NMOS sizes are the same, and all three PMOS sizes are the same.
   Use the same length for NMOS and PMOS.

   a. What is the ratio between PMOS and NMOS? How is this compared to a CMOS inverter and why?
   b. Simulate and plot the DC voltage transfer curve of this inverter as V_{out} vs. V_{in} with steps of 10 mV (with all three inputs tied together).
   c. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1, and the corresponding noise margins NM_L and NM_H.

   Connect input A connected to the NMOS closest to VSS and input C to the NMOS closest to the output.

   d. Set V_{inA}=V_{inB}=1. Simulate and plot the DC voltage transfer curve of this NAND gate as V_{out} vs. V_{inC} with steps of 10 mV.

e. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1, and the corresponding noise margins NM_L and NM_H.

f. Set V_{inB}=V_{inC}=1. Simulate and plot the DC voltage transfer curve of this NAND gate as V_{out} vs. V_{inA} with steps of 10 mV.

g. Find the values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} at points with slope of -1, and the corresponding noise margins NM_L and NM_H.

h. How do the results in Q2-bc, Q2-de, and Q2-fg compared to each other? Explain reasons for the difference.

3. (25%) Simulate the above 3-input NAND gate with C_{load} of 20 *f*F at the output. Consider input signals that go between 0 V and VDD with both the rise and fall time of 100 ps. Furthermore, **only one of the three inputs is switching at a time**.
   a. Simulate the contamination delays for both rising and falling output. For both rising and falling cases, explain the input pattern that results in this shortest delay.
   b. Simulate the worst-case propagation delays for both rising and falling output. For both rising and falling cases, explain the input patterns that result in this worst-case propagation delay.
   c. Repeat the above two questions across the following 5 corners. Show the waveforms with proper markers and complete the following table.
   d. Please also submit the sp netlist along with your report.

Process	Temperature	t_{cdr} (ps)	t_{cdf} (ps)	t_{pdr} (ps)	t_{pdf} (ps)
TT	25°C				
FF	–40°C				
SS	125°C				
SF	25°C				
FS	25°C				

4. (20%) For the 3-input NAND gate in the previous questions, with all the three inputs tied together –
   a. Simulate the propagation delay at TT corner, 25°C. Don't forget the 20-*f*F capacitive load.

b. Increase all the transistors' sizes altogether by increasing the m factor from 1 to whatever needed (but at least 5), and simulate the propagation delay at TT corner, 25°C as a function of m. You should see that the corresponding propagation delay decrease first. But if you continue to increase the transistors sizes, you will find that the propagation delay increases eventually. Report the results and explain what it happens.