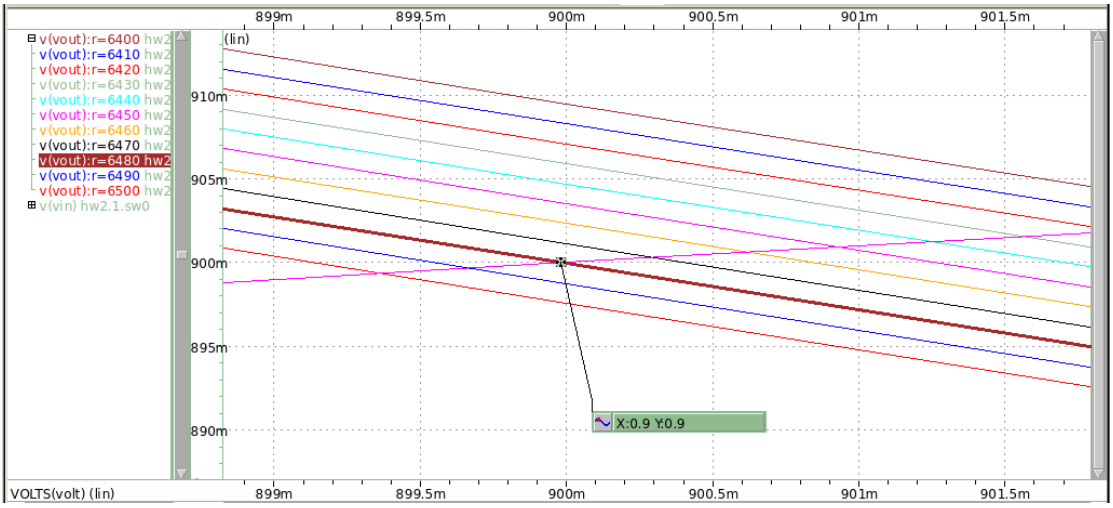
1(a)



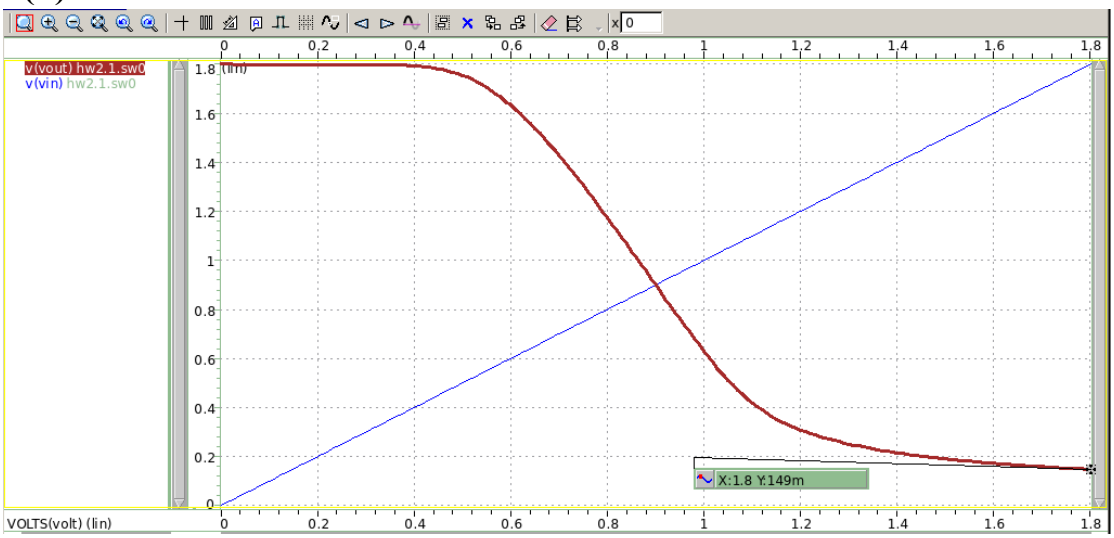

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
 *** parameter r =     6.4796k       ***

vout= 899.9976m
******
```

I use DC analysis and sweep parameter R to get the above result.

The resistance R = 6.48 kΩ

1(b)



vgs	1.8000
vds	148.5934m
vbs	0.
vth	523.6909m
vdsat	531.2545m

subckt	
element	0:mn
model	0:n_18.1
region	Linear

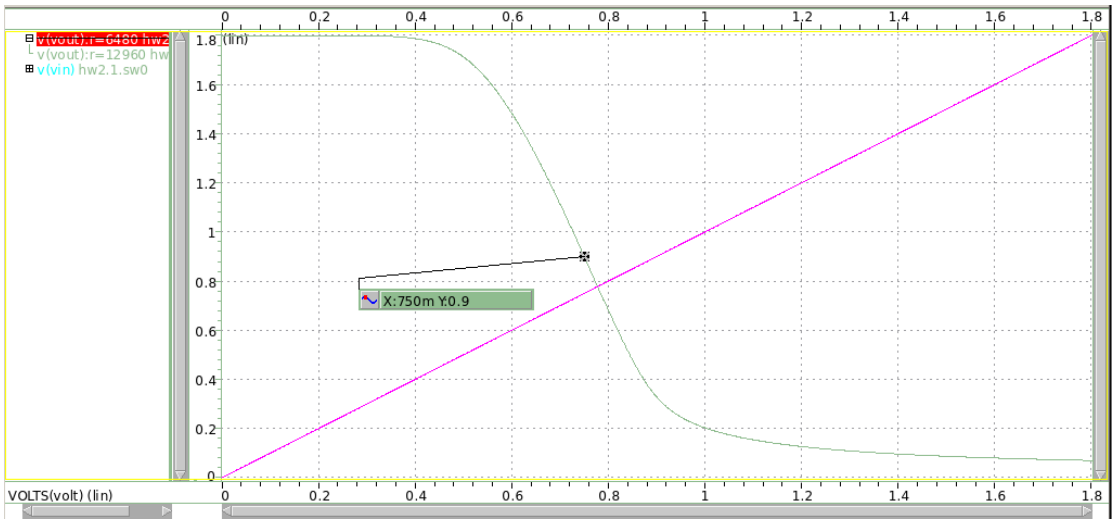
From the plot, we get V_{out} = 150mV and from the list we can get that $V_{ds} < V_{GS} - V_{TH}$.

NMOS is in triode region (liner region).

1(c)

The transition point will shift left since we want to get the same $V_{out} = 0.5\ V_{DD} = V_{DD} - I_D * R_D$, which implies that the I_D times R_D is constant. Thus, when we increase the R_D, the I_D must decease and then the overdrive voltage = $(V_{gs} - V_{th})$ would decrease since $I_D = u_n C_{ox} (W/L) * V_{ov}^2$. Therefore, the whole plot including transition point will go left.

1(d)

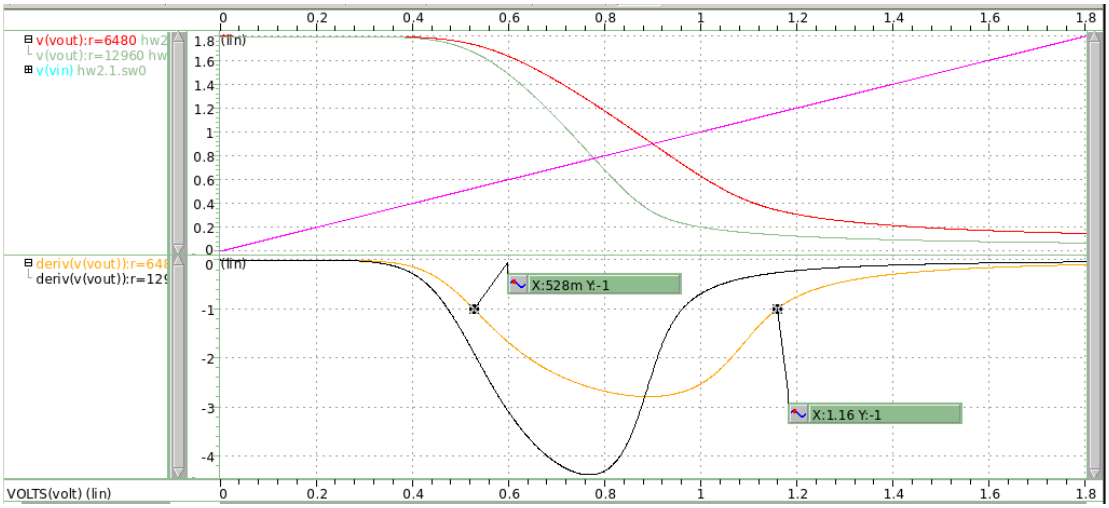


Vin= 750mV ; $V_{out} = 0.5V_{DD}$

1(e)

```
**** Analisis ****
.dc vin 0 1.8 1m sweep r 6.48k 6.48*2k 6.48k
.meas DC vil find v(vin) when deriv('v(vout)')=-1
.meas DC voh find v(vout) when deriv('v(vout)')=-1
.meas DC vih find v(vin) when deriv('v(vout)')=-1 rise=1
.meas DC vol find v(vout) when deriv('v(vout)')=-1 rise=1
.op

.end
```



1(e) for the origin R

```
*** 110030039 homework 2

****** dc transfer curves tnom=  25.000 temp=  25.000 ******
 *** parameter r =     6.4800k       ***

vil= 527.7739m
voh=   1.7310
vih=   1.1589
vol= 344.6748m
```

1(e) for the 2R

```
*** 110030039 homework 2

****** dc transfer curves tnom=  25.000 temp=  25.000 ******
 *** parameter r =    12.9600k       ***

vil= 473.9119m
voh=   1.7439
vih= 961.9826m
vol= 234.2152m
```

1(f) Noise margins for R

$NM_L = V_{IL}-V_{OL} = 183.01mV$

$NM_H = V_{OH}-V_{IH} = 572.10mV$

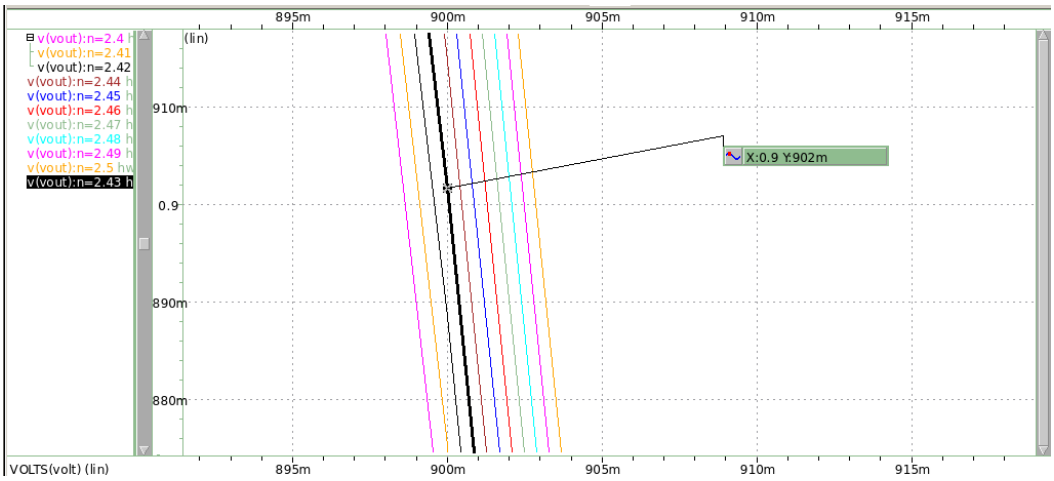
1(f) Noise margins for 2R

$NM_L = V_{IL}-V_{OL} = 239.70mV$

$NM_H = V_{OH}-V_{IH} = 781.92mV$

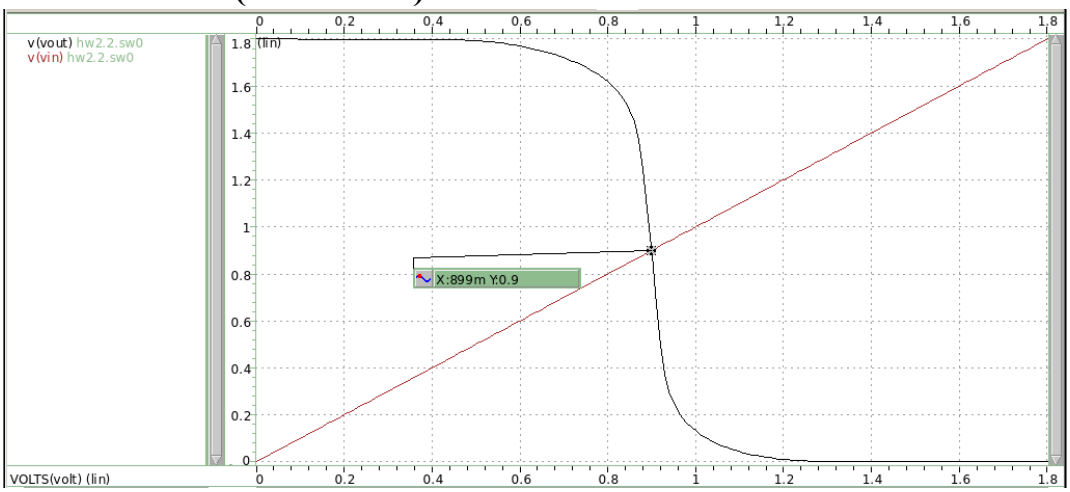
2(a)

NAND n=2.43 (set n=W/L)



The $(W/L)_P$ / $(W/L)_N$ ratio = 2.43/6 = 0.41

Inverter n=21 (set n=W/L)

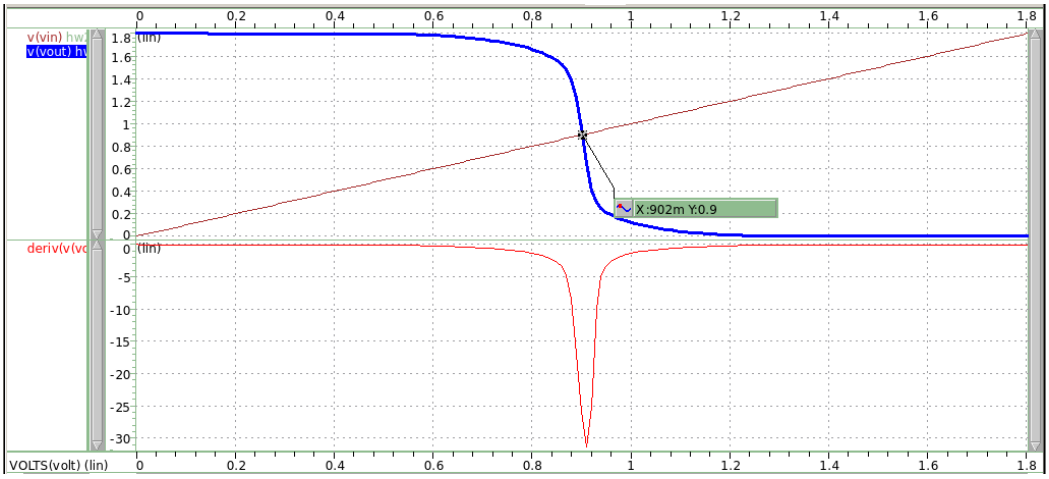


The $(W/L)_P$ / $(W/L)_N$ ratio = 21/6 = 3.50

Neglecting nonideal effects, from the equation $I = u\ C_{ox}\ (W/L)\ V_{ov}^2$, if V_{ov} is constant, the (W/L) is proportional to 1/u where u is mobility of PMOS/NMOS. From the golden inverter, we can get the result that the ratio between mobility of electrons and the mobility of holes(u_N/u_P) is 3.5. However, when we design the NAND3, we hope that the size of PMOS in this case is (6/3) *3.5 = 7. However, the result we get from simulation is n=2.43.

The reason is that when we design the NAND3, the case n=7.5 is in the critical path case, that means the only one gate will be triggered with time (only one PMOS will flow current). Nonetheless, in this case, because we trigger the 3 inputs all together (do not occur in reality), all of the 3 PMOS would flow the current. Then, if we want to get the same trigger point in this NAND3, we also need to divide the n=7.5 to 3 again. We will get that new n=2.5 which is closed to the result NAND n=2.43.

2(b)



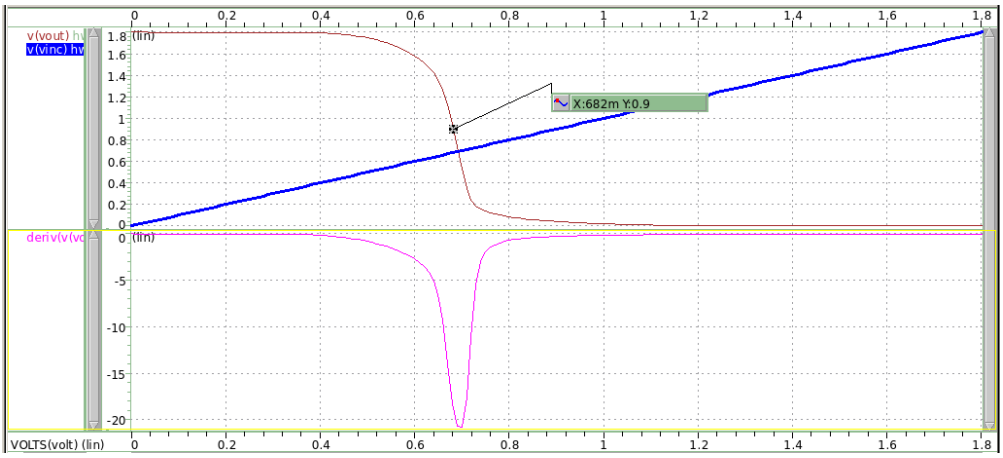
2(c)

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vil= 770.9493m
voh=   1.6926
vih=   1.0231
vol=  96.5223m
```

$NM_L = V_{IL}-V_{OL} = 674.43mV$

$NM_H = V_{OH}-V_{IH} = 669.50mV$

2(d) change input C



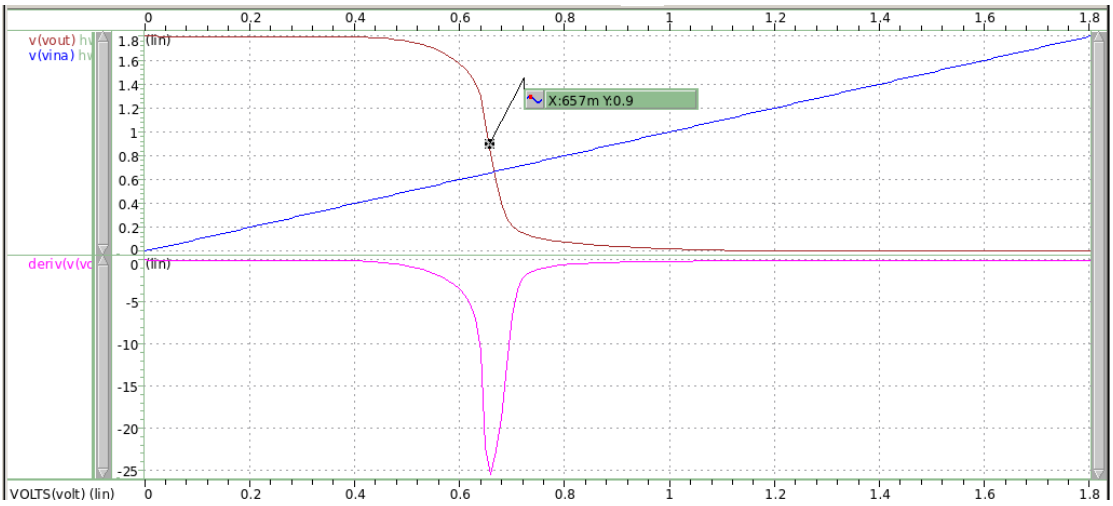
2(e) change input C

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vil= 515.1759m
voh=   1.7334
vih= 778.2565m
vol= 101.3984m
```

$NM_L = V_{IL}-V_{OL} = 413.78mV$

$NM_H = V_{OH}-V_{IH} = 955.14mV$

2(f) change input A



2(g) change input A

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vil= 520.7656m
voh=   1.7406
vih= 754.8435m
vol= 109.0913m
```

$NM_L = V_{IL}-V_{OL} = 411.67mV$

$NM_H = V_{OH}-V_{IH} = 985.76mV$

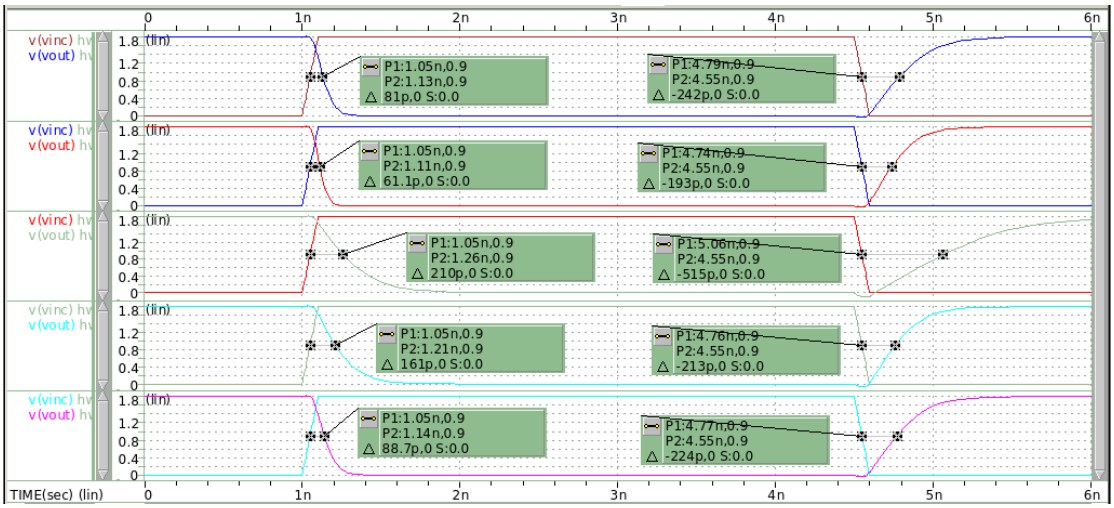
2(h)

First, in 2(b)and 2(c) we get the most balanced since $NM_L = NM_H$. Besides, the trigger point is the nearest to $0.5V_{DD}$.

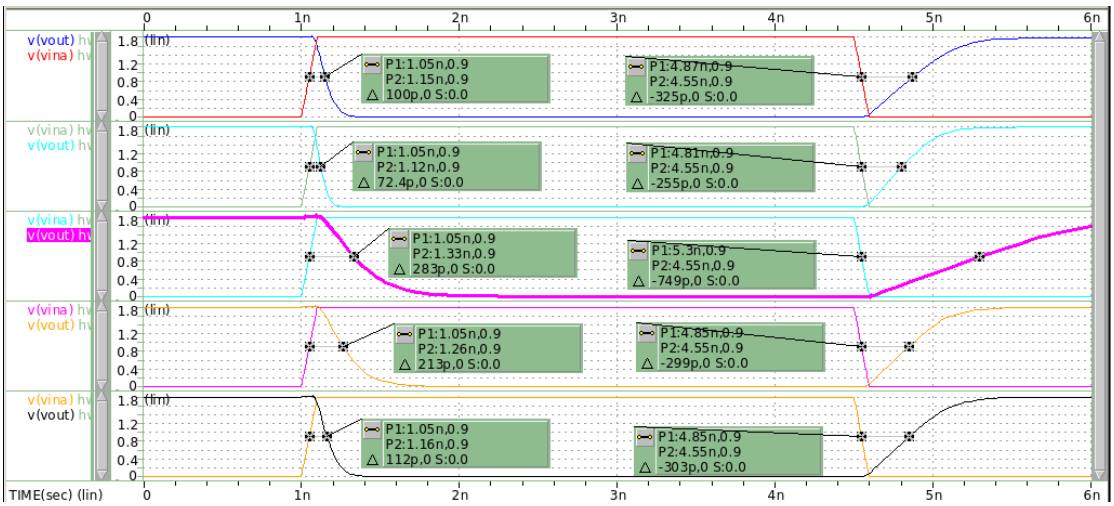
According 2(d) and 2(f), we can get the result that the trigger point shift left form V_{DD}. The reason is that if we only let one input triggered, it means that there is only one PMOS will flow the current (compare to the other two MOS). Compared to the original case, it can imagine that the β ratio decrease. Besides, since MOS with input C is more closed to MOS with input C, we also need to consider the capacitor will flow the current. It is similar to the discussion of delay, when input A goes from low to high, the capacitor of MOS B and MOS C may be charged, so input A need less current (Vgs) to let the output be 0.9V.

Furthermore, from 2(e) and 2(g), the results share the same NM_L since PMOS are parallel in NAND3 which means that the NM_H may not be influenced effectively. However, since NMOS is in series in NAND3, thus the NM_H we change input A have larger noise margin with the same reasons above.

3(a)



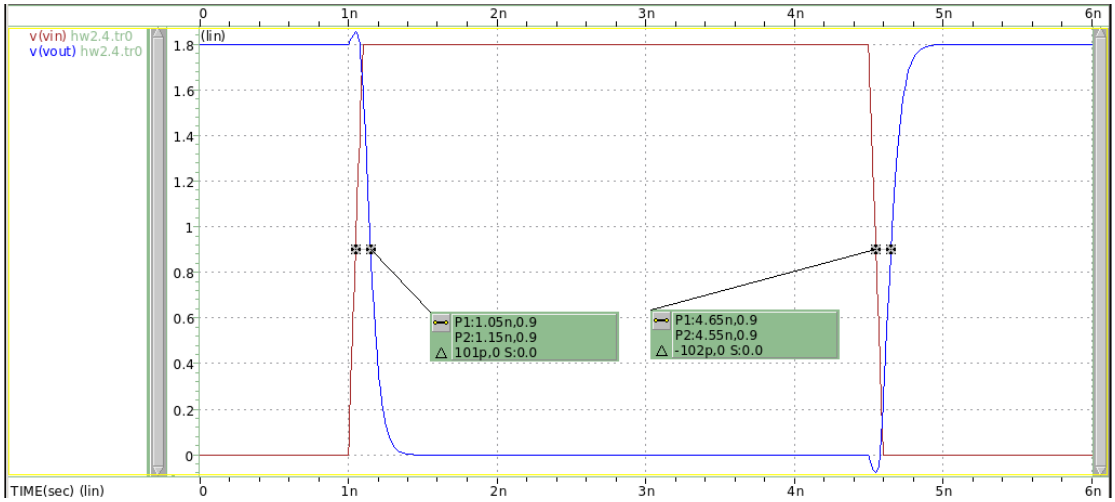
3(b)



3(c)

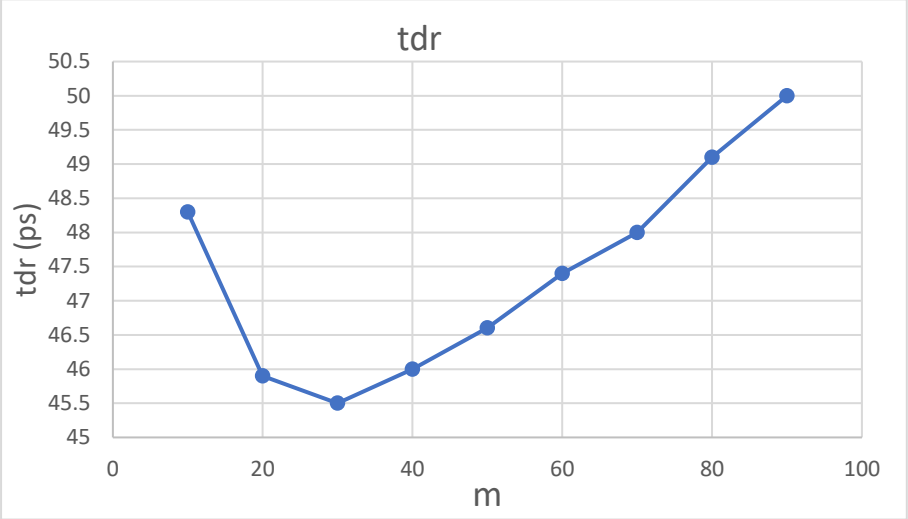
Process	Temperature	t_{cdr} (ps)	t_{cdf} (ps)	t_{pdr} (ps)	t_{pdf} (ps)
TT	25°C	240	81	330	100
FF	-40°C	190	61	260	72
SS	125°C	520	210	750	280
SF	25°C	210	161	300	210
FS	25°C	440	70	600	84

4(a)

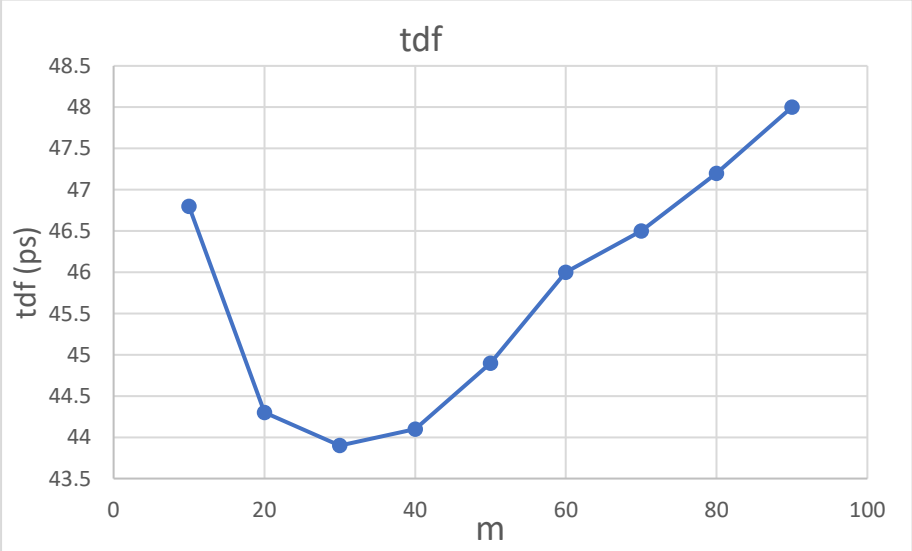


4(b)

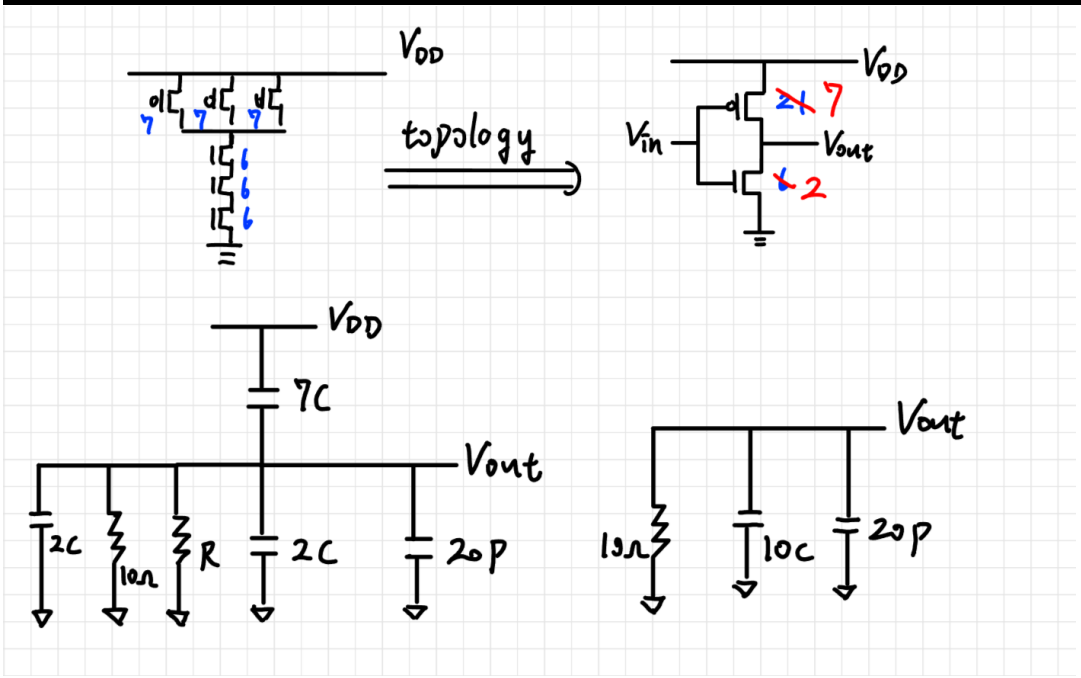
Rise delay



Fall delay



rise		fall	
n	tr(ps)	n	tf(ps)
10	48.3	10	46.8
20	45.9	20	44.3
30	45.5	30	43.9
40	46	40	44.1
50	46.6	50	44.9
60	47.4	60	46
70	48	70	46.5
80	49.1	80	47.2
90	50	90	48



Total delay = parasitic delay + effort delay

parasitic delay = 9C ≈ 10C

effort delay = $1 \cdot \frac{20P}{9C} \approx \frac{2P}{C}$

total delay ≈ $5(2C + \frac{1P}{C})$

⇒ total delay = $mC + \frac{n}{C}$, C is the cap.

m.n is artribute

First, we know that the capacitor of the MOS is proportional to its size.
From the above deduction, we can get the graph of below. We can observe that the graph goes down rapidly but after it reach the inflection point, it will do linearly.
The reason to explain the result is that when C_{MOS}<<20pF, it has difficulty driving the C load in terms of 1/C. but after it reach the inflection point, the parasitic delay leads the graph in terms of C.

Besides, before TA announced the revision of HW2_4, I have tried that when m went to 3000, there was an inflection point. I think the reason why we add the 10Ω R can help us to find c in more small value is that we can simplify the rising or falling delay to a RC charging or discharging. In the original case, the parasitic R in MOS is too small so that $\tau=RC$ is too small. However, when we add the R= 10Ω in series with all MOS, we can increase the time constant to make the result obvious with small C.