EE3230 VLSI Design (2023 Fall) HW #1

Due date: 2023/10/13 (Friday) 10am

Plagiarism is strictly prohibited. While you may engage in discussions with your peers, the homework must be completed individually by each student.

1. (30%) Use a combination of **CMOS gates with no more than 2 inputs** (i.e., NAND2, NOR2, and INV) to generate the schematics in gate-level symbols for the following functions from inputs *A*, *B*, and *C*.
(You will need to use inverters to generate $\bar{A}$, $\bar{B}$, and $\bar{C}$.)
Then complete the stick diagrams for each of the following functions according to the schematics you draw.
Hint: you may want to simplify the logic first.

(a) $Y = \left(\overline{(A+B)} + \bar{A}\right)B + A$

(b) $Y = (A + BC)\overline{(A+B)}$

(c) $Y = (\bar{A}B + A)((\bar{A})(\bar{B}) + C)\overline{(\bar{B} + AC)}$

2. (15%) For the Boolean function of the function $Y = \overline{A(B+C) + DE}$, implement the logic using ONE single complex gate with 5 inputs *A*, *B*, *C*, *D*, and *E*. Then complete the stick diagram using only one P+ and one N+ diffusion (without breaks).

3. (20%) Please simulate and analysis a CMOS inverter according to the following conditions using the model provided by TA (CIC018.l).

* Set the supply voltage to 1.8 V.
* Set the output load of this inverter to 0.1 pF.
* Use the channel length of 0.3μm for both NMOS and PMOS.
* Use the channel width of 1.8μm for NMOS.

3a) Find the optimal width for PMOS for a balanced trigger point of inverter at tt corner 25°C, report the PMOS size you use, and then report the trigger inputs for the following four corners.

The meaning of a trigger input is the input that sets Vout = 0.5×VDD.

The meaning of a balanced trigger point is as the following.

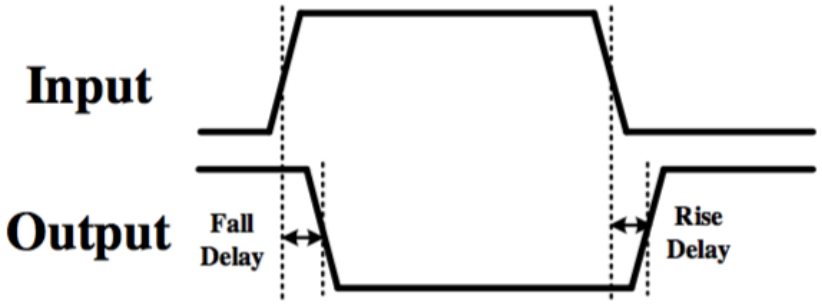
Vin = Vout = 0.5×VDD

3b) Repeat 3a) with 5X the NMOS channel width.

Process	Temperature	NMOS width 1X	NMOS width 5X
		PMOS width (μm)	PMOS width (μm)
TT	25°C		
		Trigger input (V)	Trigger input (V)
FF	–40°C		
SS	125°C		
SF	25°C		
FS	25°C		

4. (20%) Follow the previous question, run transient simulations for all 10 conditions and measure the input to output delay of the inverter. The input to output delay is measured from the input waveform crossing 0.5×VDD to the output waveform crossing 0.5×VDD, as shown in the following figure.

In your simulations, use Vpulse for the input signal. Set the rise and fall time (tr and tf) to 500 ps, and the period to 5 ns.



Attach the simulated waveforms for TT 25°C (with rise and fall time labeled clearly) for both 1X NMOS and 5X NMOS.

Process	Temperature	NMOS width 1X		NMOS width 5X	
		Fall Delay	Rise Delay	Fall Delay	Rise Delay
TT	25°C				
FF	–40°C				
SS	125°C				
SF	25°C				
FS	25°C				

5. (15%) Complete the layout, DRC, LVS, and R+C+CC PEX of the inverter in Q3a (with the channel width of 1.8μm). Repeat Q4.

Process	Temperature	NMOS width 1X	
		Fall Delay	Rise Delay
TT	25°C		
FF	–40°C		
SS	125°C		
SF	25°C		
FS	25°C		