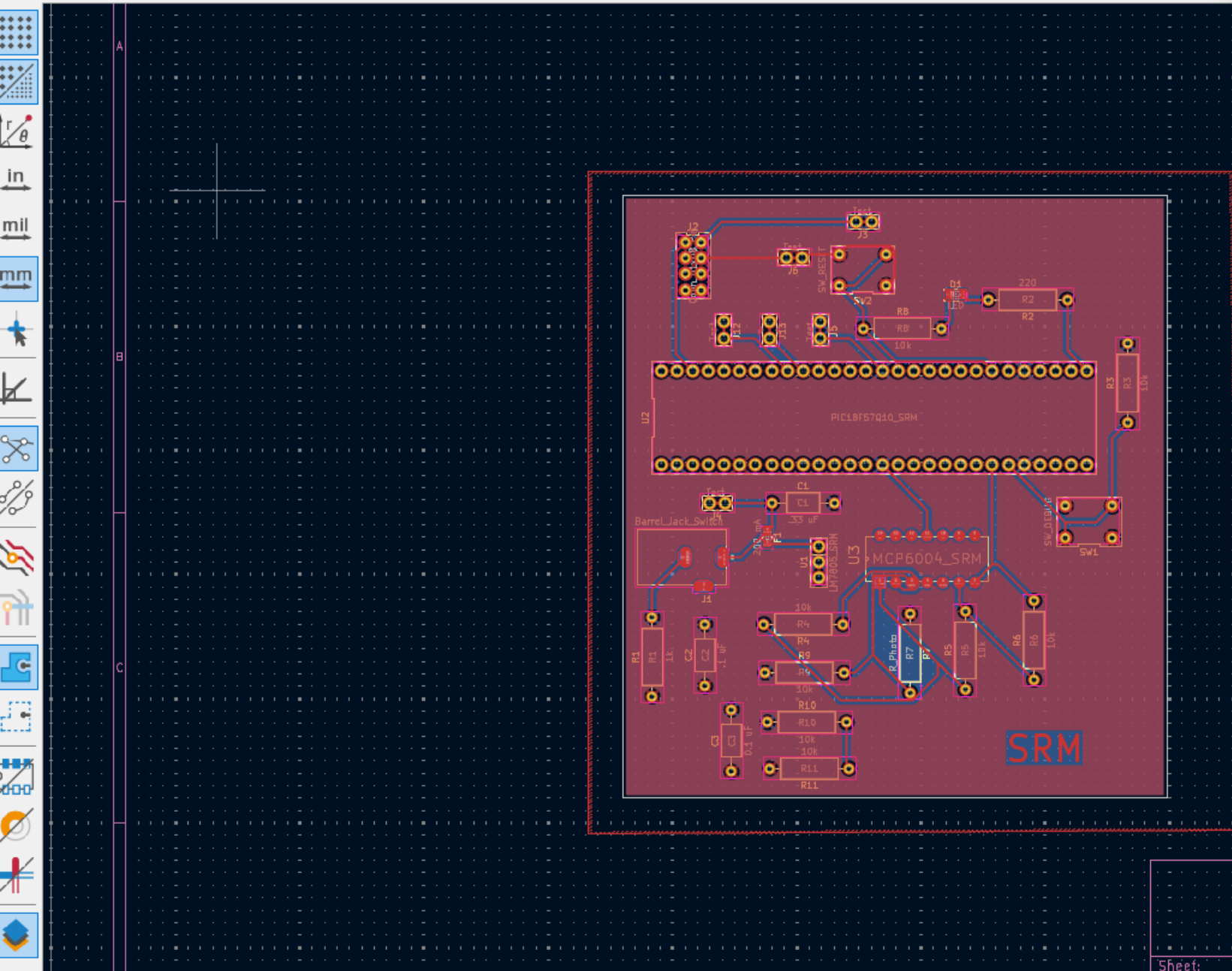




Track: use netclass width Via: use netclass sizes F.Cu (PgUp) 0.2000 mm (7.87 mils) Zoom 1.50



Pads	Vias	Track Segments	Nets	Unrouted
136	0	87	73	0

## Design Rules Checker

☒ Refill all zones before performing DRC☐ Test for parity between PCB and schematic☐ Report all errors for each track

Violations (0)

Unconnected Items (0)

Schematic Parity (not run)

Ignored Tests (5)

Show: ☐ All☒ Errors 0☒ Warnings 0☐ Exclusions

Save...

Delete Marker

Delete All Markers

Run DRC

Close

Layer Display Options

Presets (Ctrl+Tab):

---

Viewports (Shift+Tab):

---

Selection Filter

☒ All items☐ Locked items☒ Footprints☒ Text☒ Tracks☒ Vias☒ Pads☒ Graphics☒ Zones☒ Rule Areas☒ Dimensions☒ Other items