Samvel Manukyan
6173231

Lab 5: Digital to Analog Conversions

Introduction:
This lab is intended to provide an introduction on how to convert digital to analog. It exposes us to multiple bit versions of DAC circuits mainly 2 bit,4 bit, and 8 bit. This lab is also intended to introduce us to the different wave forms produced by the DAC circuits, and how to calculate sine wave word sequences in decimal (to binary).

Step 1:

n	$V_{out,\ max}$	ΔV
2	0.750000 x V_{ref}	0.250000 x V_{ref}
4	0.9375 x V_{ref}	0.0625 x V_{ref}
8	0.99609375 x V_{ref}	0.00390625 x V_{ref}
16	0.999847 x V_{ref}	0.000015259 x V_{ref}

Table 1. Maximum output voltage and step size of n-bit R-2R DAC. **[RP1]**

Step 2:
2.2. $((((((R_1 \,||\, R_2) + R_3) \,||\, R_4) + R_5) \,||\, R_6) + R_7) \,||\, R_8 = 1000\Omega$ **[RP2]**

2.3. measured: 0.9934 kΩ **[RP3]**

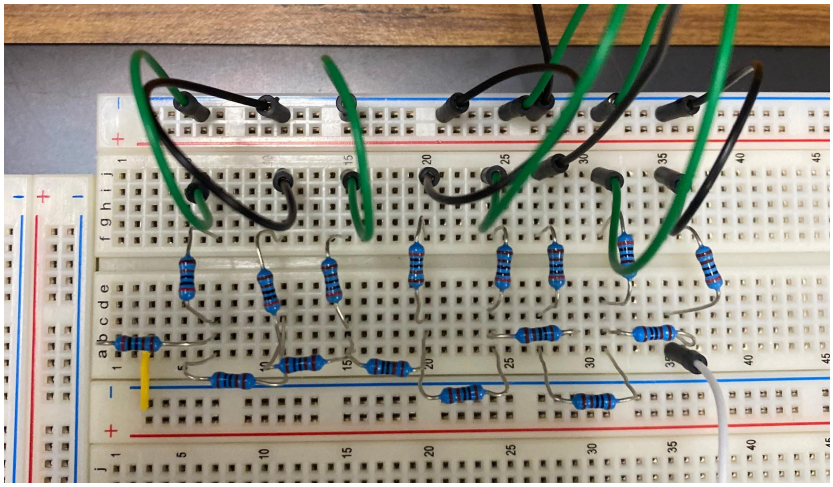
Step 3:
3.1.

D	B = $(a_3a_2a_1a_0)_2$	V_{out} (V)	ΔV_{out} (V)	D	B = $(a_3a_2a_1a_0)_2$	V_{out} (V)	ΔV_{out} (V)
0	$(0000)_2$	0.0		8	$(1000)_2$	1.6462	0.1998
1	$(0001)_2$	0.207	0.207	9	$(1001)_2$	1.8528	0.2066
2	$(0010)_2$	0.4133	0.2063	10	$(1010)_2$	2.059	0.2062
3	$(0011)_2$	0.6206	0.2073	11	$(1011)_2$	2.2658	0.2068
4	$(0100)_2$	0.8260	0.2054	12	$(1100)_2$	2.4752	0.2094
5	$(0101)_2$	1.033	0.207	13	$(1101)_2$	2.6790	0.2038
6	$(0110)_2$	1.2393	0.2063	14	$(1110)_2$	2.8856	0.2066
7	$(0111)_2$	1.4464	0.2071	15	$(1111)_2$	3.0928	0.2072

Table 2. Vout and ΔVout of the 4-bit R-2R ladder DAC **[RP4]**.

3.2. The results in table 2 do agree with our voltages from table 1. If we use the max voltage from the DC supply for logic 1, we get 3.3V($\frac{1}{16}$)=0.20625. The result comes out to be very close to what we measured for our ΔV_{out}. **[RP5]**

Step 4:
4.1.



[RP6]

4.2.

D	B = $(a_7a_6a_5a_4a_3a_2a_1a_0)_2$	V_{out} (V)	ΔV_{out} (V)	D	B = $(a_3a_2a_1a_0)_2$	V_{out} (V)	ΔV_{out} (V)
0	$(00000000)_2$	0.0		8	$(11111000)_2$	3.1937	
1	$(00000001)_2$	0.013	0.013	9	$(11111001)_2$	3.2058	0.0121
2	$(00000010)_2$	0.026	0.013	10	$(11111010)_2$	3.2211	0.0153
3	$(00000011)_2$	0.03903	0.01303	11	$(11111011)_2$	3.2330	0.0119
4	$(00000100)_2$	0.05197	0.01294	12	$(11111100)_2$	3.2478	0.0148
5	$(00000101)_2$	0.064992	0.013022	13	$(11111101)_2$	3.2602	0.0124
6	$(00000110)_2$	0.077948	0.012956	14	$(11111110)_2$	3.2738	0.0136
7	$(00000111)_2$	0.090968	0.01302	15	$(11111111)_2$	3.2869	0.0131

Table 3. V_{out} and ΔV_{out} of the 8-bit R-2R ladder DAC **[RP7]**

4.3. The steps are smaller for N=8. We expected the steps to be smaller because according to our calculations 3.3V($\frac{1}{16}$) is larger than 3.3V($\frac{1}{256}$) and as such the calculated ΔV_{out} is equal to 0.01289 which is consistent with our data table. **[RP8]**

4.4 The ratio is greater for N=8

	Mean (μ) of ΔV_{out}	STD (σ) of ΔV_{out}	σ/μ
N = 4 (Table 2)	0.206193	0.00204303	0.009908
N = 8 (Table 3)	0.013155	0.00091784	0.069771

Table 4. $\frac{\sigma}{\mu}$ of ΔV_{out} for the 4-bit and 8-bit R-2R ladder DAC. **[RP9]**

4.5. If we were to use more bits to reduce the deviation in the step sizes we would have a better performance. Minimizing the deviation in the step sizes can also increase the resolution. **[RP10]**

Step 5:

Time step (k)	D_k	$B_k = a_3a_2a_1a_0$ (binary value of D_k)	Time step (k)	D_k	$B_k = a_3a_2a_1a_0$ (binary value of D_k)
0	8	1000	8	8	1000
1	10	1010	9	5	0101
2	13	1101	10	2	0010
3	14	1111	11	1	0001
4	15	1110	12	0	0000
5	14	1101	13	1	0001
6	13	1101	14	2	0010
7	10	1010	15	5	0101

Table 5. Sine wave word sequence produced for 4-bit R-2R ladder DAC **[RP11].**

5.2.

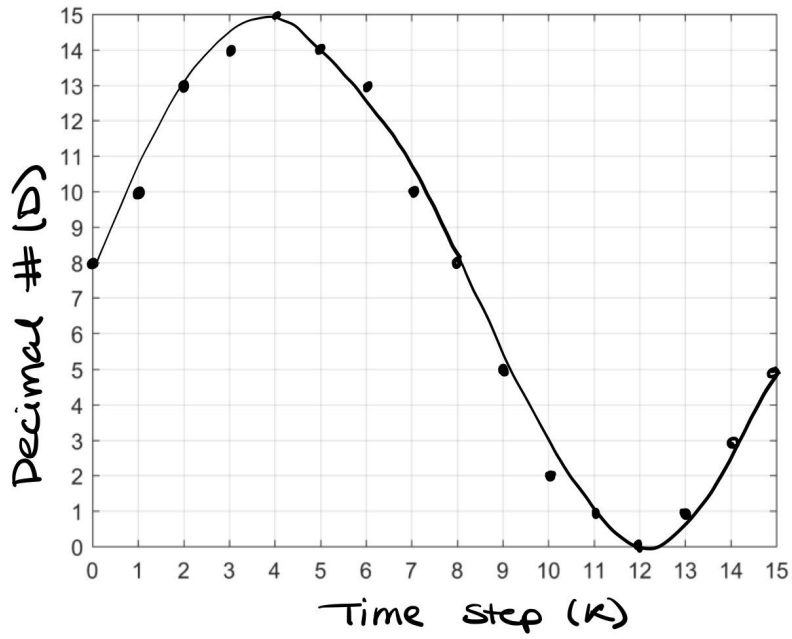


Figure 4. Sine wave using 4-bit R-2R DAC **[RP12].**

Conclusion:

It can be deduced from practice with various bit R-2R DAC circuits, different word inputs, and evaluation of change in V_{out} at each step interval that reducing the step sizes and increasing the number of bits results in less deviation from the voltage output. We proved this through calculating expected resistance as well as measuring the circuit directly. The 8-bit ladder's standard deviation of V_{out} was 0.00091784 V, compared to the 4-bit ladder's standard deviation of 0.00204303 V. Additionally, it was demonstrated that decimal word sequences could be translated into binary and represented as a sine wave for a 4-bit R-2R ladder DAC.