

### Lab 4: Introduction to Digital Combinational Logic

**Introduction:** This lab is intended to familiarize us with digital and analog signals, logic gates, and digital logic. The relationship between frequency and the number of inverters in a ring oscillator will also be covered, as well as the relationship between Vin and Vout with different input signals, the characteristics of NAND and NOR gates, how to build and debug a 1-bit half adder using a circuit diagram, and the properties of NAND and NOR gates.

#### Step 1:

##### 1.2.

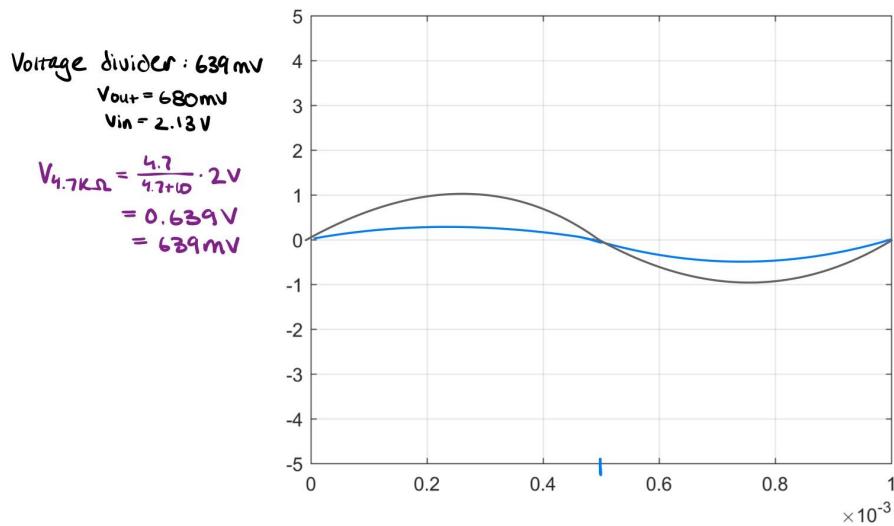


Figure 2. Vin vs. time and Vout vs. time for step 1.2 [RP1]

##### 1.3.

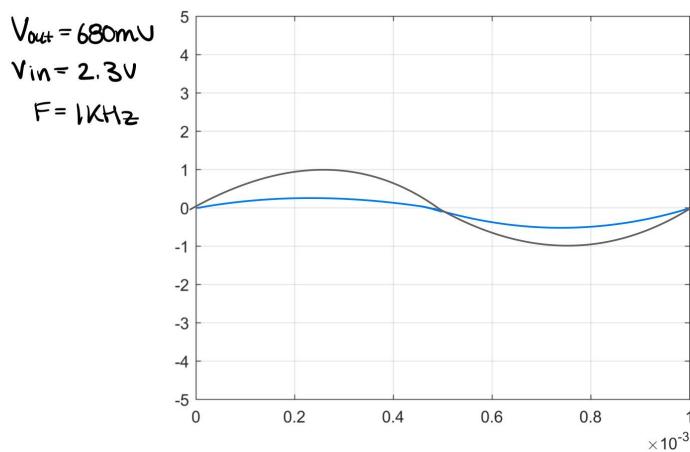


Figure 3. Vin vs. time and Vout vs. time for step 1.3 [RP2]

**1.4.** measured:  $0.99\text{ k}\Omega$

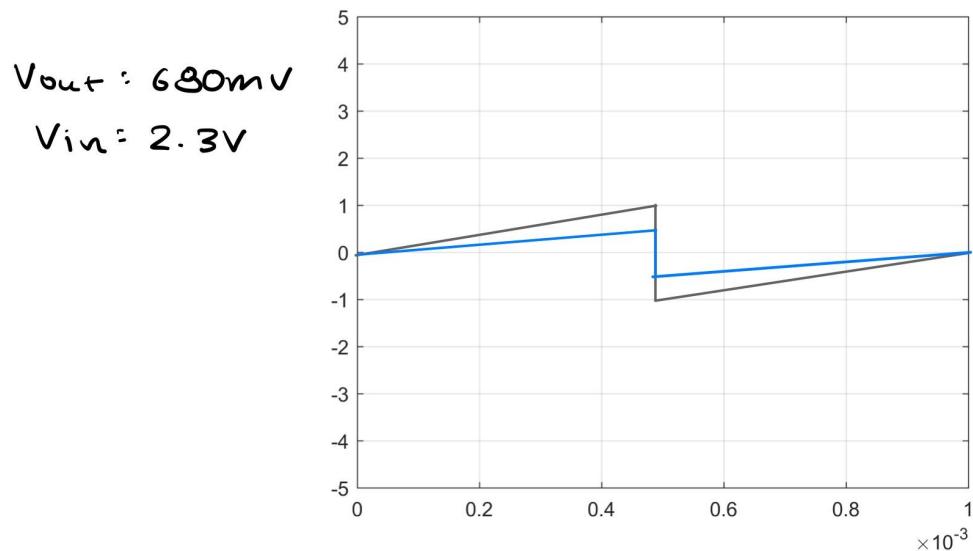


Figure 4.  $V_{in}$  vs. time and  $V_{out}$  vs. time for step 1.4 [RP3]

**1.5.**

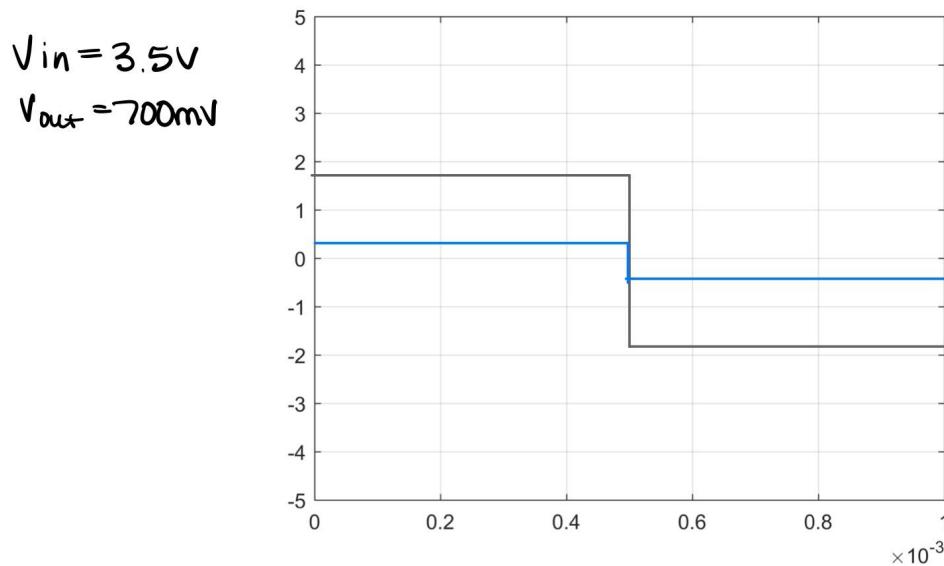


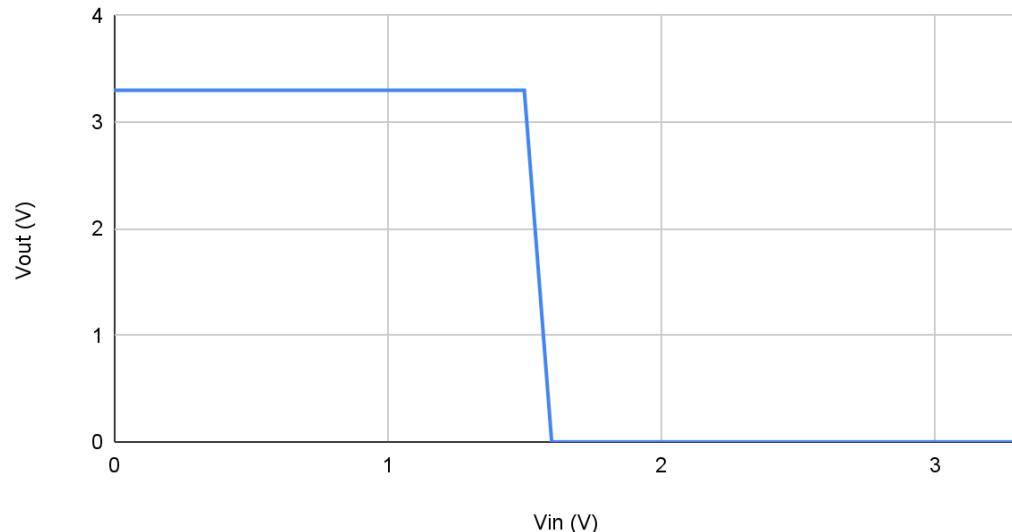
Figure 5.  $V_{in}$  vs. time and  $V_{out}$  vs. time for step 1.5 [RP4]

**Step 2:**

The proper supply voltage for both ICs is 3-18V. [RP5]

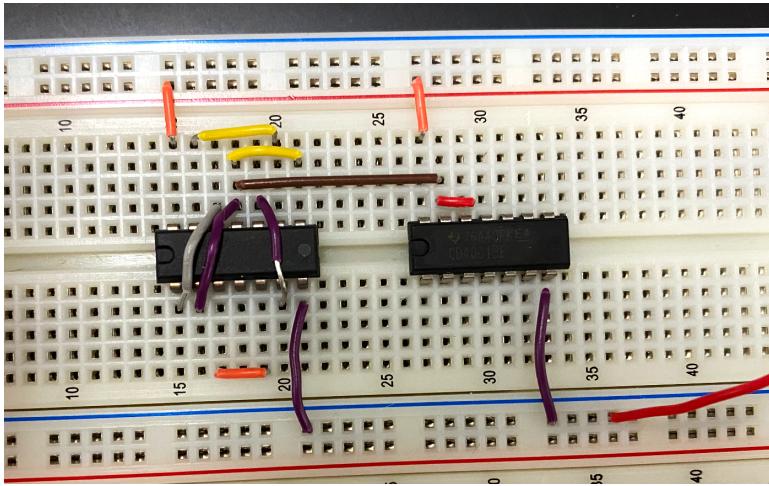
**Step 3:****2.4.**

$V_{in}$ (V)	$V_{out}$ (V)						
0.0	3.2998	1.0	3.2998	2.0	.00014	3.0	.00013
0.1	3.2998	1.1	3.2999	2.1	.00014	3.1	.00013
0.2	3.2999	1.2	3.2999	2.2	.00013	3.2	.00013
0.3	3.2999	1.3	3.2999	2.3	.00014	3.3	.00013
0.4	3.3000	1.4	3.2999	2.4	.00014		
0.5	3.3000	1.5	3.2999	2.5	.00014		
0.6	3.3000	1.6	.00016	2.6	.00013		
0.7	3.3000	1.7	.00015	2.7	.00014		
0.8	3.3000	1.8	.00015	2.8	.00014		
0.9	3.3000	1.9	.00015	2.9	.00014		

Table 4.  $V_{in}$  and  $V_{out}$  (V) of the NAND gate [RP6].**2.5.****Vout vs. Vin****[RP7]**

**2.6.** There is a voltage drop after  $V_{in}$  exceeds 1.5 V. The voltage exceeded the logical state becoming invalid. [RP8]

**Step 3:**



[RP9]

A (n1)	B (n2)	n3	n4	n5	Sum (S, n6)	Carry (C, n7)
0	0	1 (3.29 V)	1 (3.3001 V)	1 (3.3001 V)	0 (0 V)	0 (0 V)
0	1	1 (3.301 V)	1 (3.3001 V)	0 (0 V)	1 (3.3002 V)	0 (0 V)
1	0	1 (3.3001 V)	0 (0 V)	1 (3.3002 V)	1 (3.3002 V)	0 (0 V)
1	1	0 (0 V)	1 (3.3002 V)	1 (3.3002 V)	0 (0 V)	1 (3.3003 V)

Table 5. The truth table of a 1-bit half adder. [RP10]

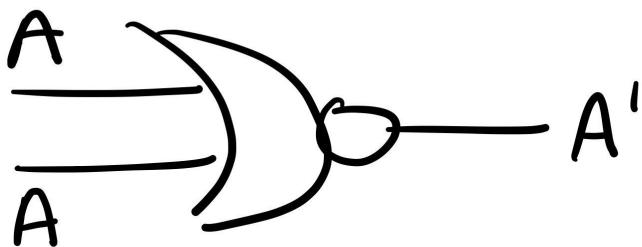
**3.4.**

$S = A \underline{XOR} B$

$C = A \underline{AND} B$

[RP11]

**Step 4:**



[RP12]

**Step 5:**

5.1.

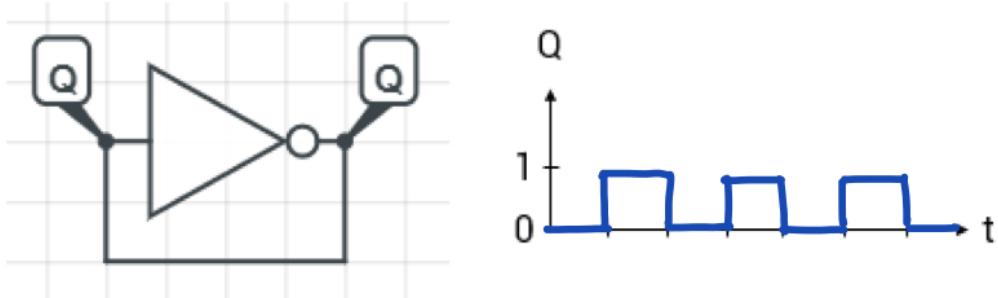


Figure 13. The schematic (left) and the suggested plot grid (right) for step 5.1.

[RP13]

5.2.

n	Period (T)	Frequency ( $f = 1/T$ )
1	$2t_p$	$(\frac{1}{2})t_p$
3	$6t_p$	$(\frac{1}{4})t_p$
5	$8t_p$	$(\frac{1}{10})t_p$
7	$14t_p$	$(\frac{1}{14})t_p$

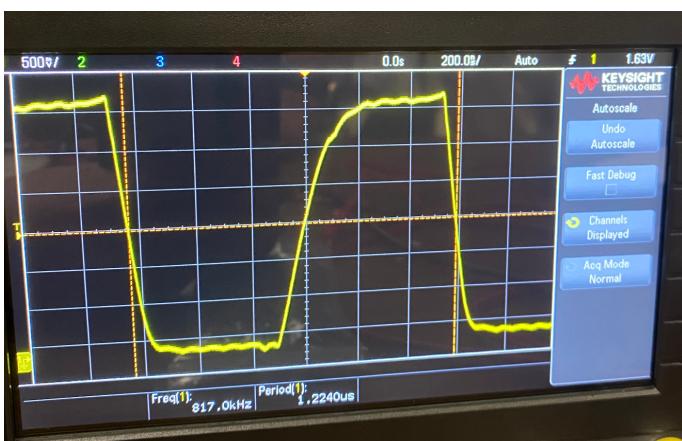
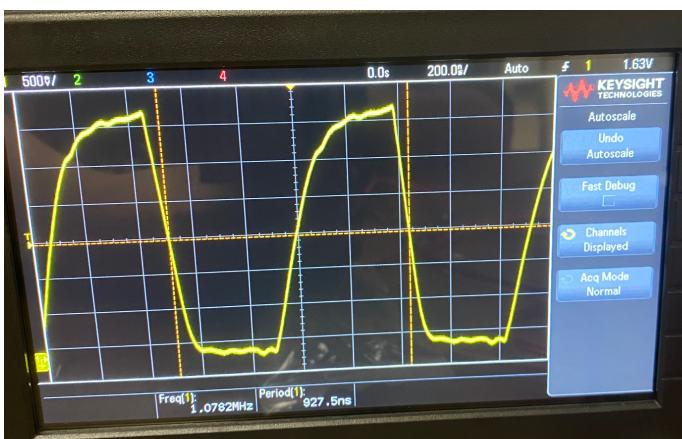
Table 6. Calculated period and frequency of the chain of inverters [RP14]

5.3.

$$f = \frac{1}{2nt_p}$$

[RP15]

## 5.4.



[RP16]

n	Period (T)	Frequency ( $f = 1/T$ )
3	632.5μs	1.57 MHz
5	927.5ns	1.077 MHz
7	1.22μs	817.3 kHz

Table 7. Measured period and frequency of the chain of inverters [RP17]

### 5.5.

Such a circuit has the advantage of making it possible to test transistor speeds. In these ICs, a new transistor might be tested, and a greater frequency would imply that the transistor can switch on and off more quickly. [RP18]

#### Conclusion:

The peak output voltage across a resistor remains constant regardless of the shape of an AC voltage, as shown by modifying the voltage's waveform, which is in accordance with the data gathered during the lab. It was discovered that the behavior of a 1-bit half adder could be demonstrated using NAND and NOR gates. Additionally, logic gates could be used to create an inverter chain or ring oscillator, which shows that there are delays between node state inversions.