

## ECE 10BL: Lab 1

### Introduction:

This lab introduces the imbalance of the NMOS and PMOS in the CMOS inverter and how the ratio of PMOS to NMOS affects the transient voltage ( $V_{TH}$ ) and the noise margin parameters in the CMOS ( $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ , NMH, NML). It also introduced us to virtually simulating and implementing NMOS, PMOS, and CMOS inverters in LTspice. We were also exposed to the relationship between  $K_p$  and  $K_n$ , and the derivation of the transient voltage and how it changes with different configurations.

### Part 1:

#### Parallel Connection of MOSFETs

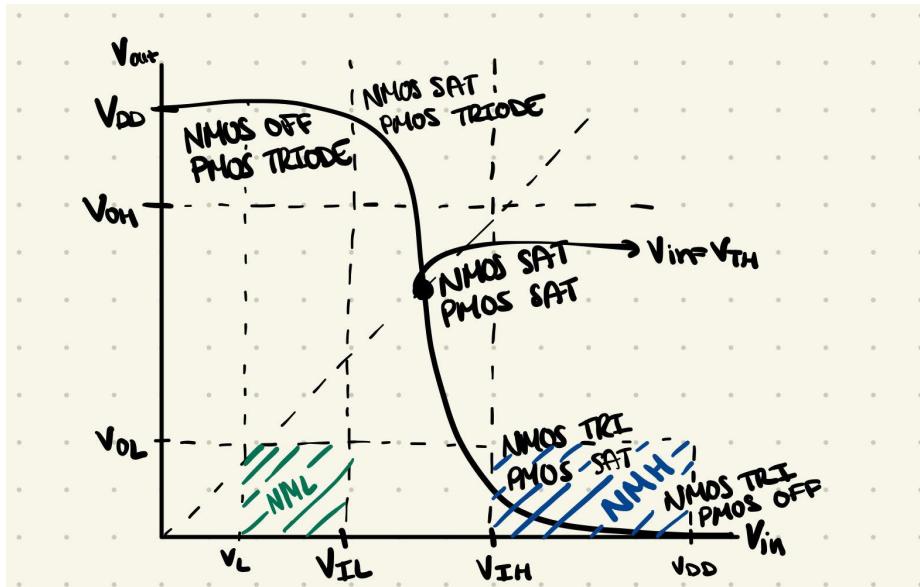
The total current flowing through the parallel NMOS circuit will be the sum of each of the currents flowing through each NMOS,  $i_{DS}(\text{total}) = i_{DS(1)} + i_{DS(2)}$ . The current in the parallel circuit will be twice the current of the single NMOS circuit. None of the parameters in the  $i_{DS}$  equation is changed by the parallel NMOS connection, and the equation of the  $i_{DS}$  remains the same for each individual transistor. Any change in the parameters will result in a different drain to source current and the parallel circuit will be the sum of the individual current flowing through the transistors with different parameters. The only difference is that the total current for the parallel NMOS connection would be the sum of the individual currents flowing through each respective transistor. If  $n$  NMOS are connected in parallel the total current equation would be the sum of the currents of each individual transistor,  $i_{DS}(\text{total}) = i_{DS(1)} + i_{DS(2)} + \dots + i_{DS(n)}$ . [RP1]

#### Inverter Transient Point (Threshold Voltage)

$$\begin{aligned}
 & \text{NMOS } \not\in \text{PMOS in SAT } \not\in \text{ON} \\
 & V_{GS_1} \geq V_{TN} \quad |V_{GS_2}| \geq |V_{TP}| \\
 & V_{DS_1} \geq V_{GS_1} - V_{TN} \quad |V_{DS_2}| \geq |V_{GS_2}| - |V_{TP}| \\
 & V_{GS_1} = V_{IN} = V_{TH} \quad V_{GS_2} = |V_{GS_2}| = V_{DD} - V_{IN} \\
 & i_{D_1} = i_{D_2} \\
 & \frac{K_n}{2} (V_{GS_1} - V_{TN})^2 = \frac{K_p}{2} ((|V_{GS_2}| - |V_{TP}|)^2) \\
 & \frac{K_n}{2} (V_{TH} - V_{TN})^2 = \frac{K_p}{2} (V_{DD} - V_{TH} - |V_{TP}|)^2 \\
 & \sqrt{K_n} (V_{TH} - V_{TN}) = \sqrt{K_p} (V_{DD} - V_{TH} - |V_{TP}|) \\
 & \sqrt{K_n} V_{TH} - \sqrt{K_n} V_{TN} = \sqrt{K_p} V_{DD} - \sqrt{K_p} V_{TH} - \sqrt{K_p} |V_{TP}| \\
 & \sqrt{K_n} V_{TH} + \sqrt{K_p} V_{TH} = \sqrt{K_p} V_{DD} - \sqrt{K_p} |V_{TP}| + \sqrt{K_n} V_{TN} \\
 & V_{TH} (\sqrt{K_n} + \sqrt{K_p}) = \sqrt{K_p} (V_{DD} - |V_{TP}|) + \sqrt{K_n} V_{TN} \\
 & V_{TH} = \frac{\sqrt{K_p} (V_{DD} - |V_{TP}|) + \sqrt{K_n} V_{TN}}{\sqrt{K_n} + \sqrt{K_p}}
 \end{aligned}$$

If  $K_p > K_n$ , then the threshold voltage ( $V_{TH}$ ) will be more negative, meaning the device will turn on at a lower voltage. If  $K_p = K_n$ , the threshold voltage will be zero, meaning that the device will turn on at zero gate-source voltage and the drain-source current will be at its maximum value at this point. If  $K_p < K_n$ , then the threshold voltage will be more positive, meaning the device will turn on at a higher voltage. [RP2]

## Noise Margin



The metric of noise margin is very useful because it describes the circuit's tolerance to noise and other disturbances in the signal. The higher the noise margins the less tolerance to noise, but the more costly and the less power efficient the digital circuit becomes. [RP3]

An increase in the threshold voltage will decrease the noise margins, because it will decrease the range of the input voltages that are in between the high and low outputs. A decrease in the threshold voltage will increase the noise margins, because as per section 6.9.4 in the textbook it will increase the range of input voltage between the high and low output states. Decreasing the threshold voltage will maximize the area of gray boxes shown in Figure 6.51 in the textbook.

[RP4]

## Part 2:

### Inverter as a Switch

A NMOS inverter is a circuit where the power source is connected to a load resistor in series with a NMOS with the drain terminal connected to  $V_{out}$  and the source terminal connected to ground. In its ON state, when  $V_{in} \geq V_{TH}$ ,  $V_{out} = V_{DD} \frac{R_{ON}}{R_L + R_{ON}}$ . In its OFF state, when  $V_{in} < V_{TH}$ , the NMOS pulls the  $V_{out}$  up to  $V_{DD}$ . This mimics the behavior of an inverter because when our input voltage is considered to be high our output voltage is low and when our input voltage is

considered to be low our output voltage is high. The PMOS works in sort of the same way. The structure of the PMOS inverter is the power source connected to the PMOS in series with a load resistor tied to ground. In its OFF state, when  $V_{IN} > V_{TH}$ , the PMOS pulls the  $V_{out}$  down to ground.

In its ON state,  $V_{IN} \leq V_{TH}$ , the  $V_{out} = V_{DD} \frac{R_L}{R_L + R_{ON}}$ . The PMOS and NMOS inverters are not ideal

inverters due to the fact that the PMOS in its ON state doesn't pull  $V_{out}$  up all the way to  $V_{DD}$  and the NMOS in its ON state doesn't pull  $V_{out}$  all the way down to ground. In the case of Figure 3, the above explanation can be applied assuming  $V_{IN}=0V$  is below the threshold voltage for an NMOS and above a threshold voltage in a PMOS and  $V_{IN}=5V$  is above threshold voltage for an NMOS and below threshold voltage in a PMOS. [RP5]

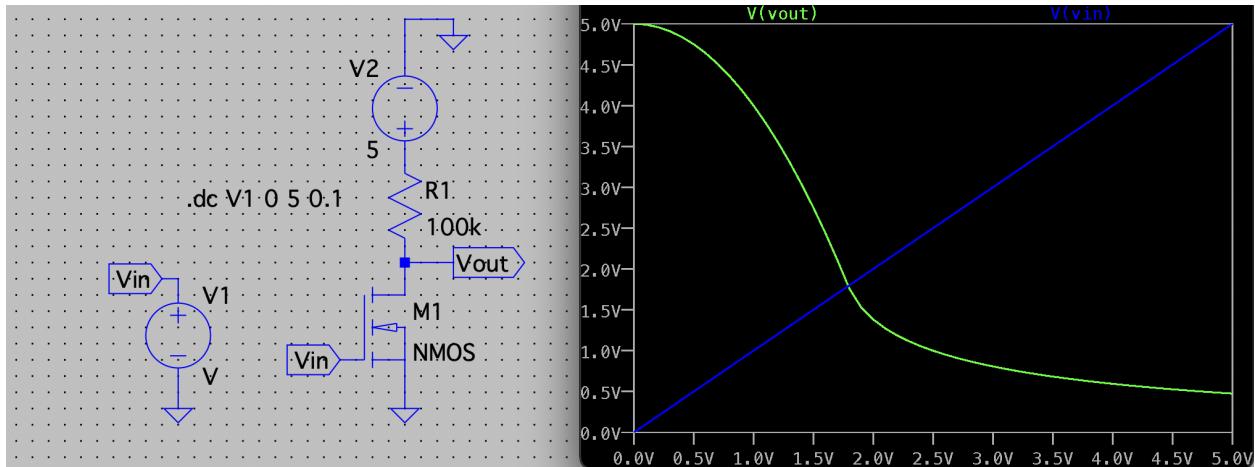


Figure 3. NMOS inverter/switch [RP6]

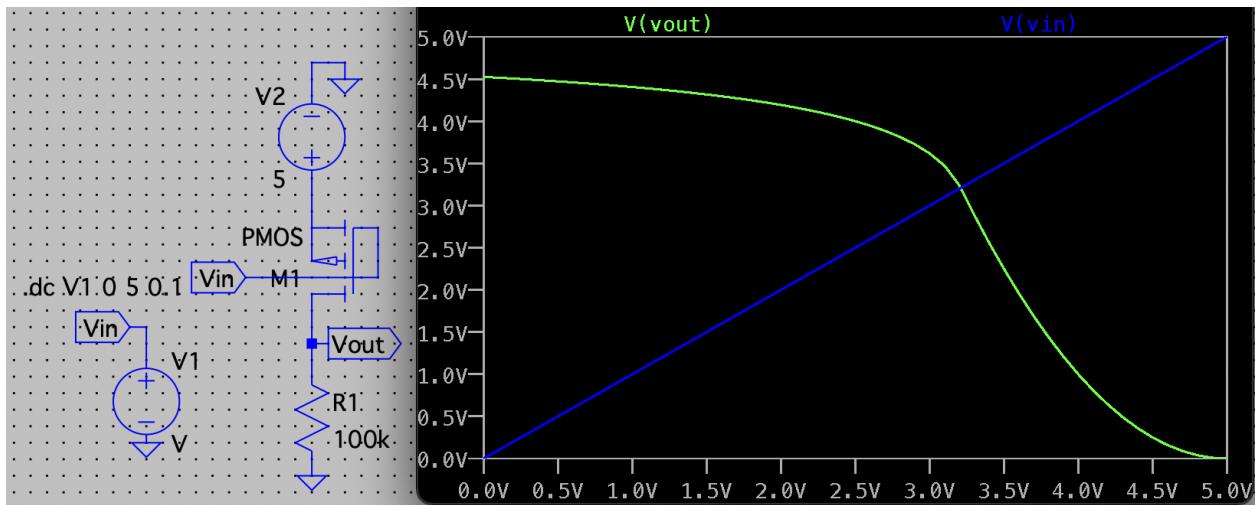


Figure 4. PMOS Inverter/switch [RP6]

The simulation outputs show that the circuits are bad switches, because ideal switches behave like a step function where the voltage switches from high to low instantaneously and our simulation shows that the switches are not like the ideal model. [RP7]

## CMOS Inverter

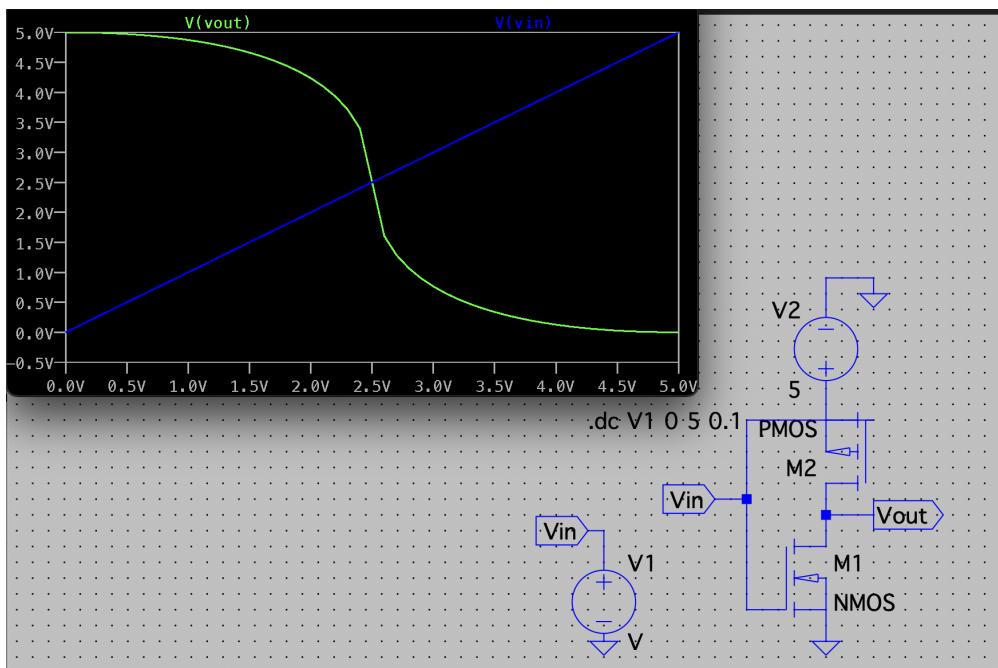


Figure 5. 1:1 CMOS Inverter Schematic [RP8]

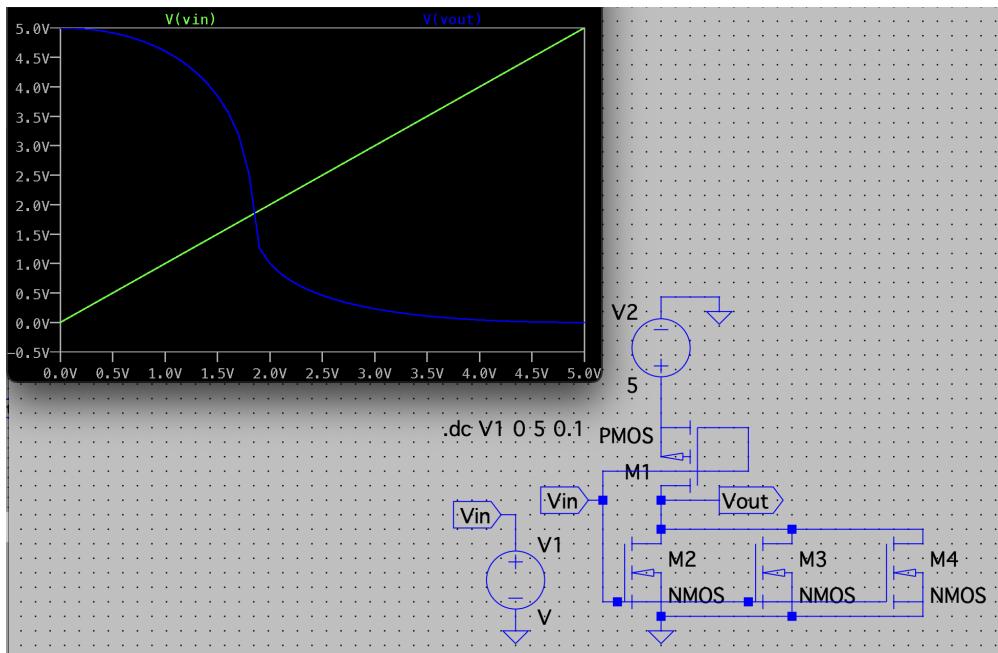


Figure 6. 1:3 CMOS Inverter Schematic [RP8]

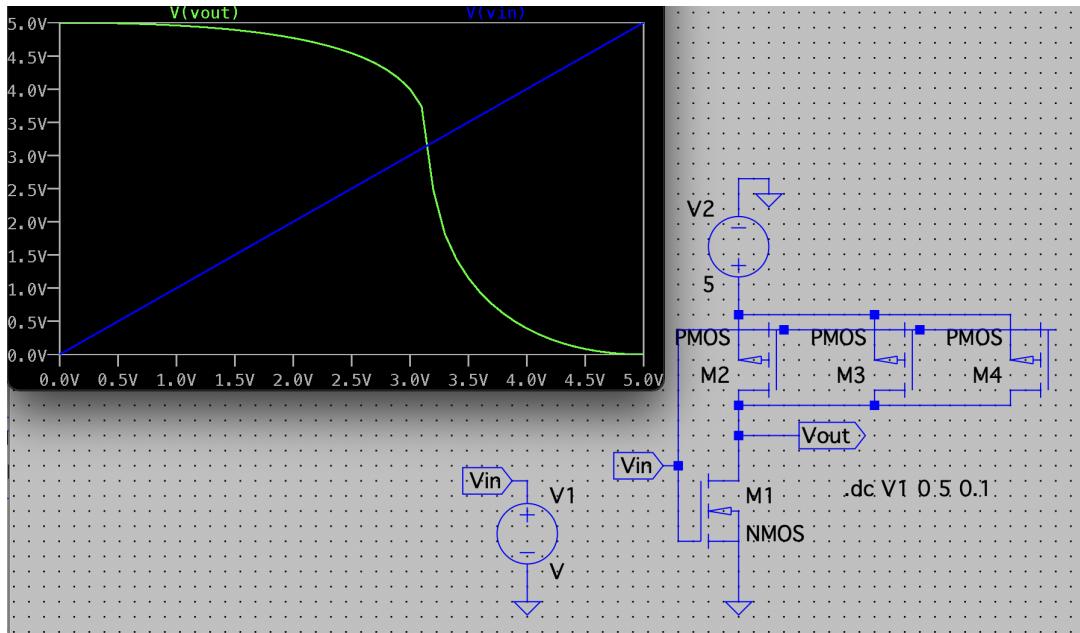


Figure 7. 3:1 CMOS Inverter Schematic [RP8]

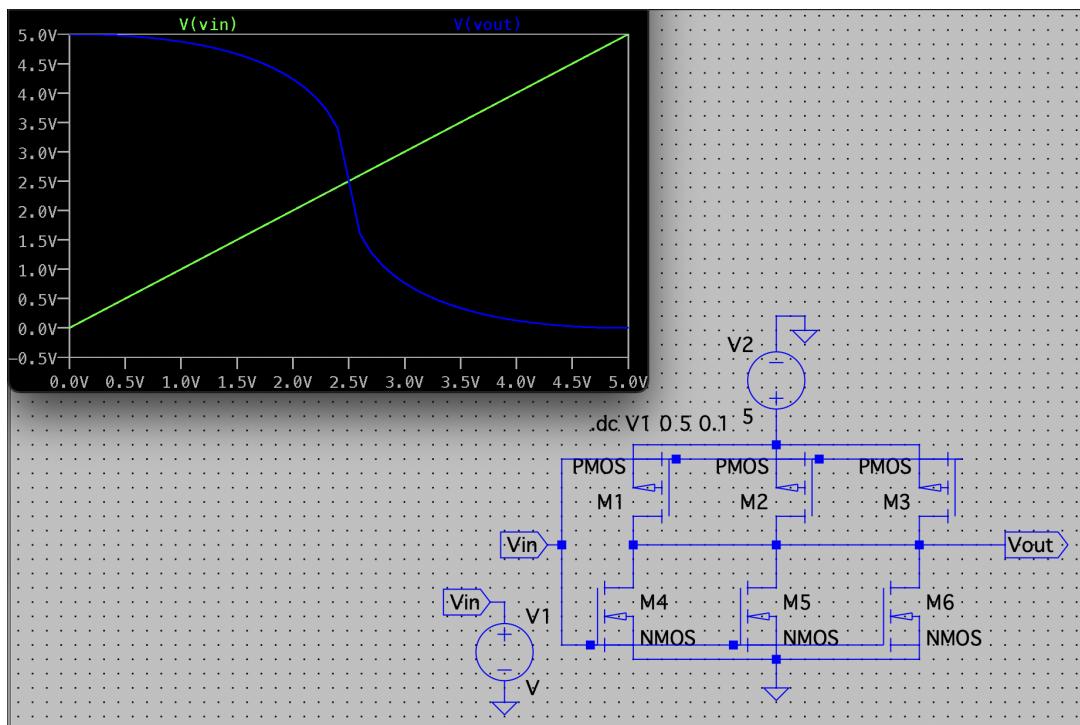


Figure 8. 3:3 CMOS Inverter Schematic [RP8]

PMOS:NMOS Ratio	1:1	1:3	3:1	3:3
$V_{TH}$	2.5 V	1.85 V	3.15 V	2.5 V
$V_{IL}$	2.2 V	1.45 V	2.9 V	2.2 V
$V_{OH}$	3.9 V	4.1 V	4.3 V	4 V
$V_{IH}$	3.0 V	2.2 V	3.5 V	2.9 V
$V_{OL}$	0.8 V	0.66 V	1.2 V	0.9 V
NML	1.4 V	0.79 V	1.7 V	1.3 V
NMH	0.9 V	1.9 V	0.8 V	1.1 V

Table 1. The static discipline of inverters with different sizes of transistors [RP9]

The data in Table 1 shows that the 1:1 and 3:3 CMOS configurations are very similar in terms of the  $V_{TH}$  and the noise margins parameters. This was expected as the configurations both have the same ratio. The 1:3 CMOS configuration produced lower  $V_{TH}$  and noise margin values compared to the 3:1 CMOS configuration. This could have been predicted due to the fact that the NMOS inverters have a low threshold voltage. It should be noted that the NML and NMH values for the 3:1 and 1:3 CMOS configurations appear to be switched. [RP10]

The data obtained from Table 1 is consistent with the analytical expressions and predictions we made from Part 1. When we do a side by side comparison of the 1:1 and 3:1 CMOS configurations we can see that the  $V_{TH}$  increases, the NML increases, and the NMH decreases. This observation aligns with our prediction from Part 1. When doing a side by side comparison of the 3:3 and 1:3 CMOS configurations we can see that  $V_{TH}$  decreases, the NML decreases, and NMH increases. This was the complete opposite of our previous observation. We were able to notice that when we had more NMOS in the ratio of the CMOS configuration our  $V_{TH}$  decreased, and when we had more PMOS in the ratio our  $V_{TH}$  increased. [RP11]

**Part 3:**  
**CMOS Inverter**

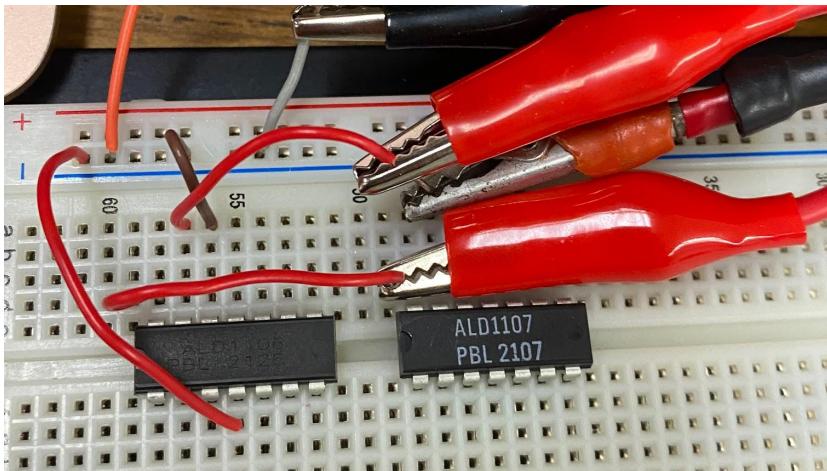


Figure 9. 1:1 CMOS Inverter Circuit [RP12]

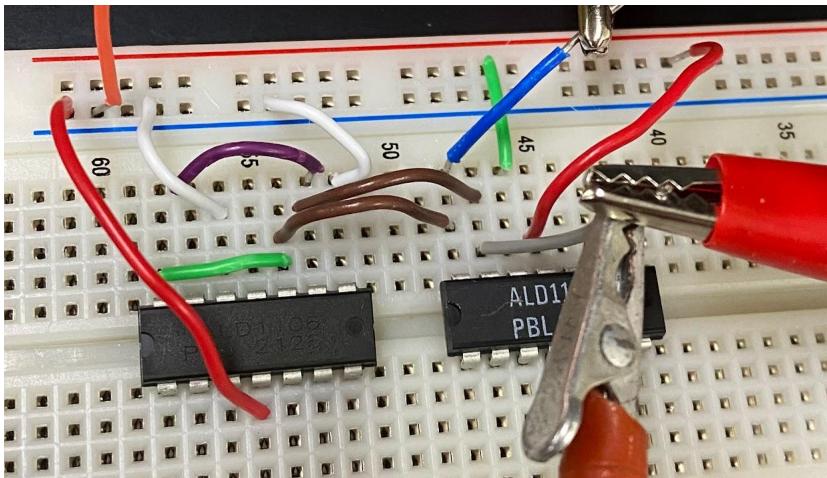


Figure 10. 1:2 CMOS Inverter Circuit [RP12]

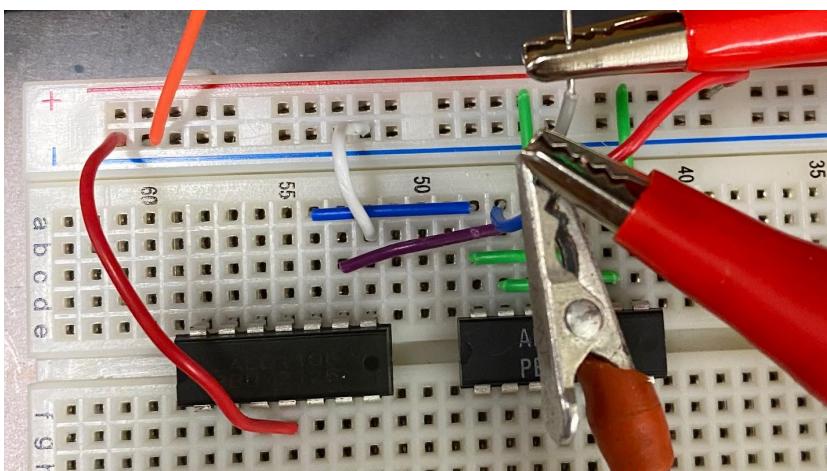


Figure 11. 2:1 CMOS Inverter Circuit [RP12]

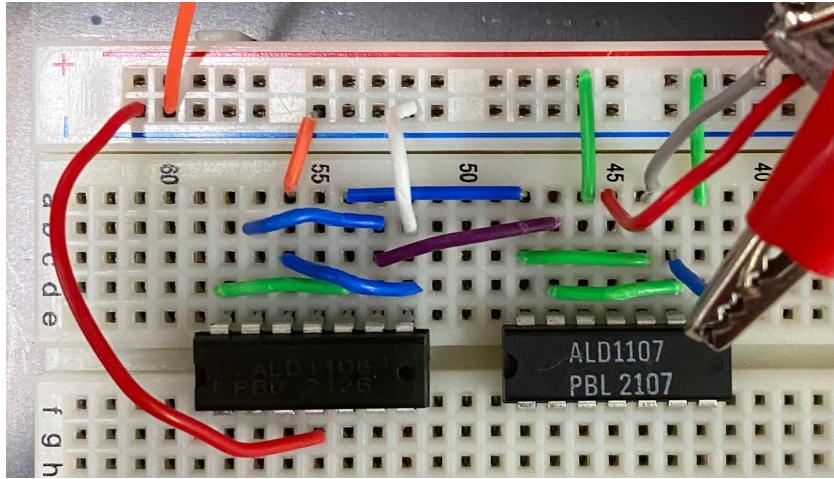


Figure 12. 2:2 CMOS Inverter Circuit [RP12]

PMOS:NMOS Ratio	1:1	1:2	2:1	2:2
$V_{TH}$	2.213 V	2.018 V	2.375 V	2.267 V

Table 2.  $V_{TH}$  of inverters with different sizes of transistors [RP13]

Our data in Table 2 matches the  $V_{TH}$  expression found in Part 1. When we increased the number of PMOS in the CMOS configuration ratio the  $V_{TH}$  increased, and when we increased the number of NMOS in the CMOS configuration ratio the  $V_{TH}$  decreased. We also found that the  $V_{TH}$  for the 1:1 and the 2:2 CMOS configurations are almost identical, which proves that maintaining a 1:1 CMOS configuration has no effect on  $V_{TH}$ . [RP14]

### Conclusion:

In this laboratory experiment, we studied the correlation between varying PMOS to NMOS ratios and their impact on threshold voltage and noise margins. Our findings, which were based on CMOS simulations, breadboard setups, and data analysis, showed that increasing the PMOS to NMOS ratio leads to a higher threshold voltage ( $V_{TH}$ ), higher low noise margin (NML), and lower high noise margin (NMH). Conversely, increasing the NMOS to PMOS ratio results in a lower  $V_{TH}$ , lower NML, and higher high noise margin (NMH). The results from our CMOS build on the breadboard matched with our LTspice simulation results.