

ECE 10BL - Lab 2

Introduction:

This lab session provided us with the opportunity to become familiar with the I-V curves of both NMOS and PMOS, including the triode and saturation regions. We also studied the characteristics of MOSFETs connected in parallel and the impact on drain-to-source current. In addition, we explored the concepts of current mirrors and analyzed the effective current flow in each branch.

Pre-Lab 1 I-V Characteristics

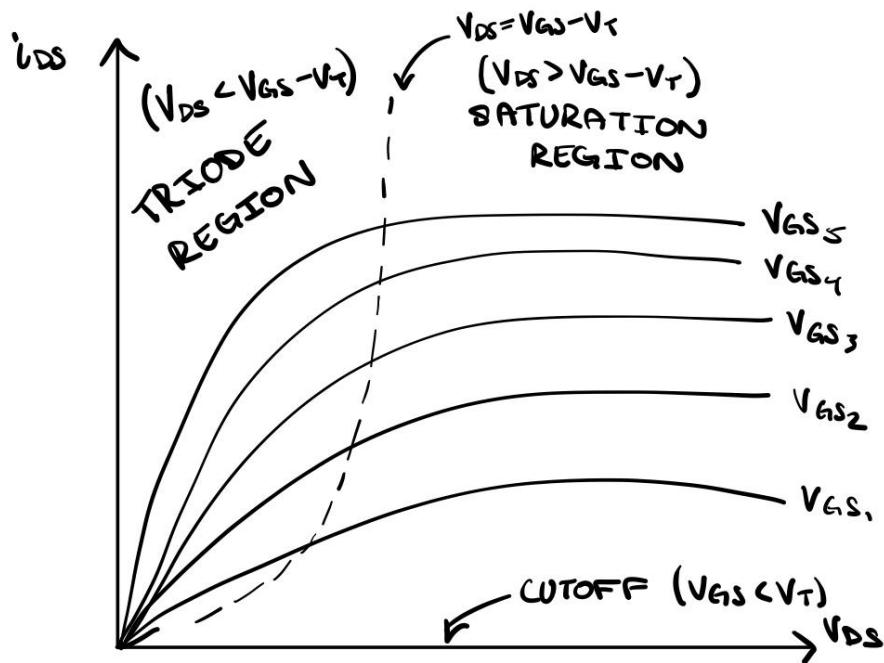


Figure 1. I-V characteristics of a NMOS with regions and conditions labeled [RP1]

Parallel Connections of MOSFETs

In a n -parallel PMOS circuit the value of K_p will increase by a factor of n and this will also cause the value of the i_{DS} to increase by a factor of n . For example if we have 3 parallel connected PMOS circuits the value of K_p will be increased by a factor of 3, resulting in a value of $3K_p$. This will also cause the value of the drain to source current to increase by a factor of 3 to $3i_{DS}$. [RP2]

Current Mirror

Given that the two NMOS in the current mirror have the same parameters and the resistors are the same, the current in each of the NMOS will be the same. This means that the ammeter will read I_{bias} . [RP3]

After removing the ammeter we can confirm that the current in the right branch is equal to I_{bias} using Ohm's Law. the current in the right branch would be equal to the voltage drop across R over R. $I_{DS2} = \frac{V_{dd} - V_{out}}{R}$ [RP4] $V_{out} = V_{DD} - nI_{Bias}R$ [RP5]

Pre-Lab 2

I-V Characteristics



Figure 2. NMOS Circuit I-V simulation in LTspice [RP6] [RP7]

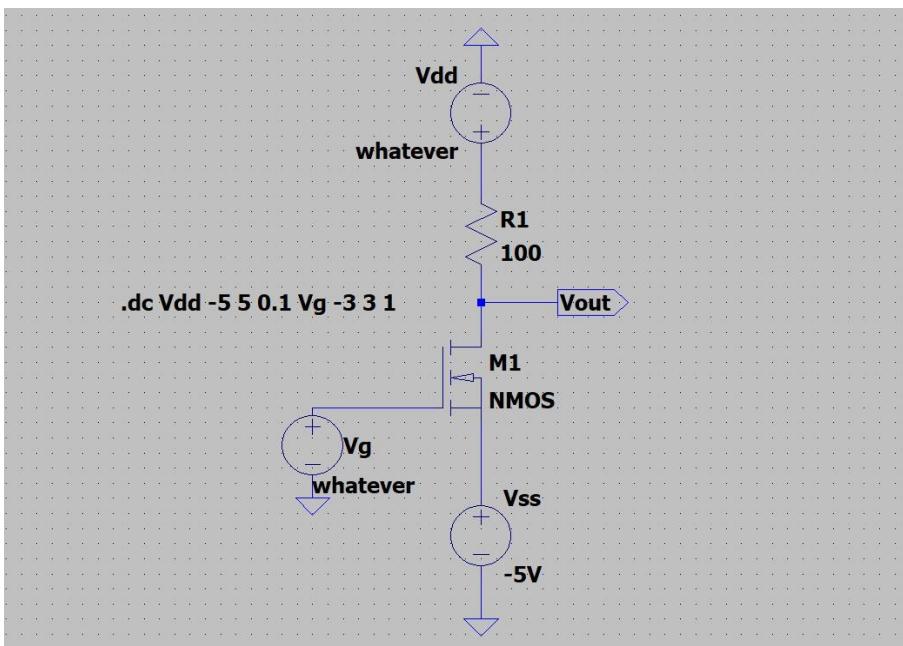


Figure 3. NMOS circuit schematic LTspice [RP6]

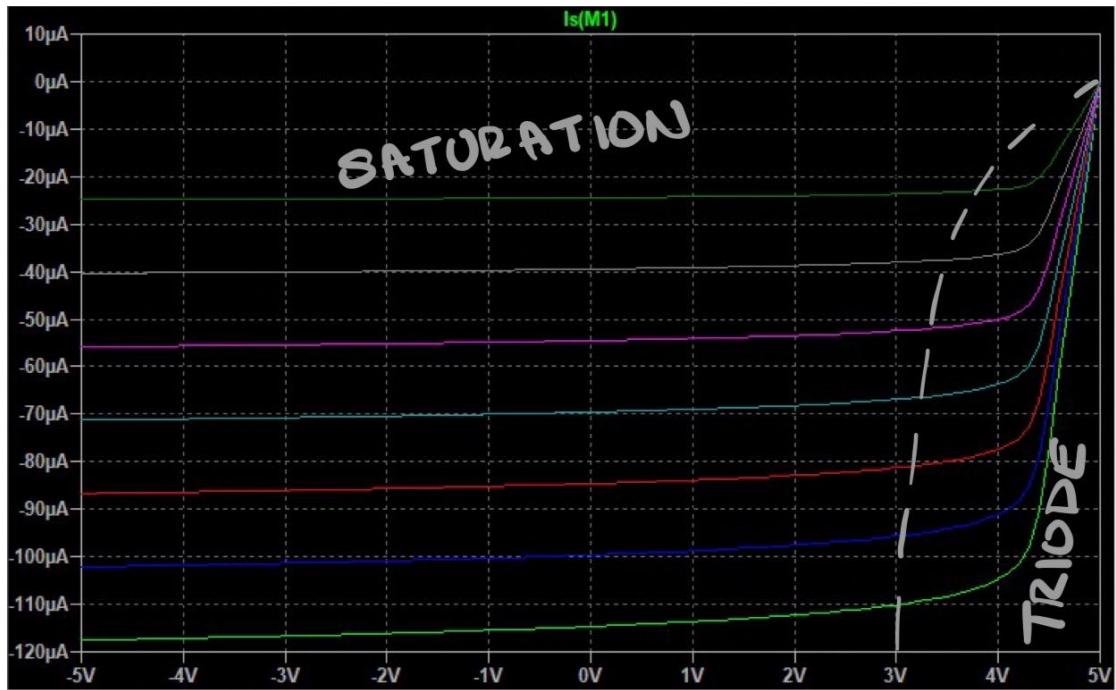


Figure 4. PMOS Circuit I-V simulation in LTspice [RP8] [RP9]

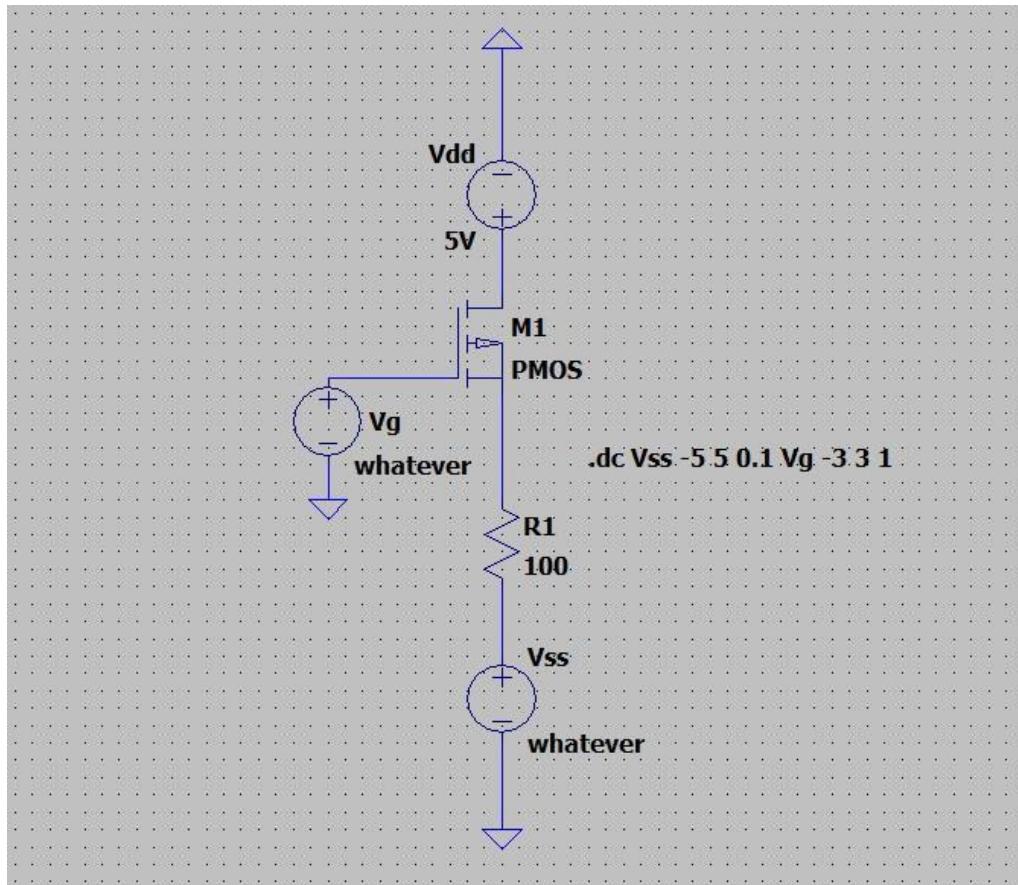


Figure 5. PMOS circuit schematic LTspice [RP8]

Lab 2

Current Mirror

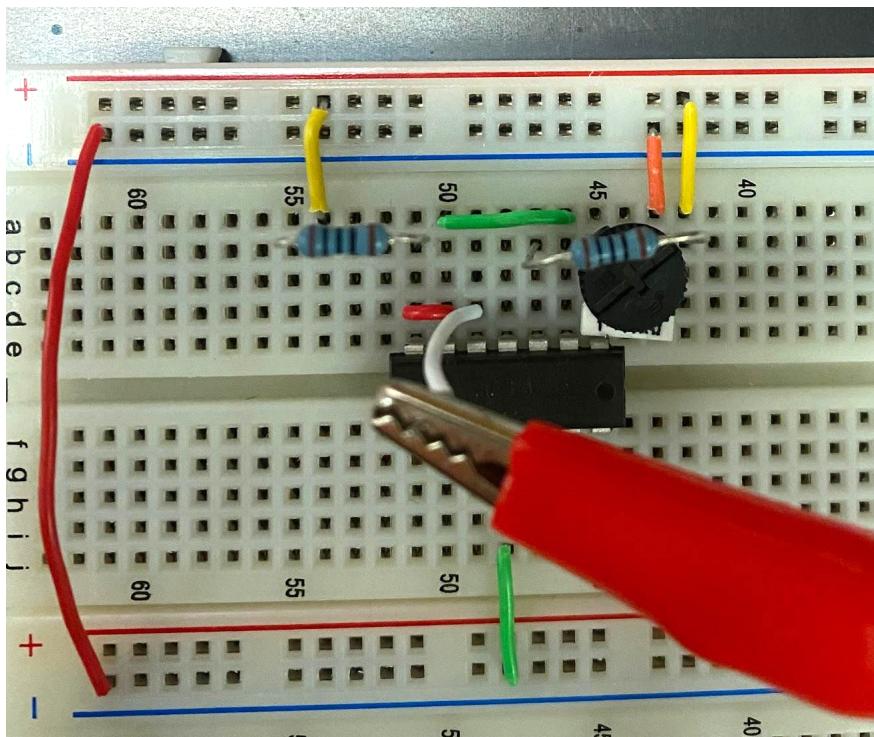


Figure 6. Current Mirror constructed on breadboard [RP10]

The current value in the left branch is 4.56mA. [RP11]

The value of R_p under this condition is 0.44692k Ω . [RP12]

In order to make the current in the right branch twice as much as the current in the left branch we can either change the mosfet parameters (which is not practical in the case of this lab), or we can connect the right branch in parallel with another NMOS. This is because we know that if n NMOS are connected in parallel, $I_{DS} = I_{DS1} + I_{DS2} + \dots + I_{DSn}$. The V_{out} under this condition is 4.1553 V. [RP13]

Conclusion

In this lab, we sketched an I-V plot for a NMOS, understood the parallel connection of MOSFETs, and analyzed the behavior of current mirrors. We also used LTspice to simulate NMOS and PMOS transistors and plotted their I-V characteristics using sweep simulations. The final circuit construction exercise tested our ability to control the current flow in the circuit in a practical lab manner by using parallel connected NMOS.