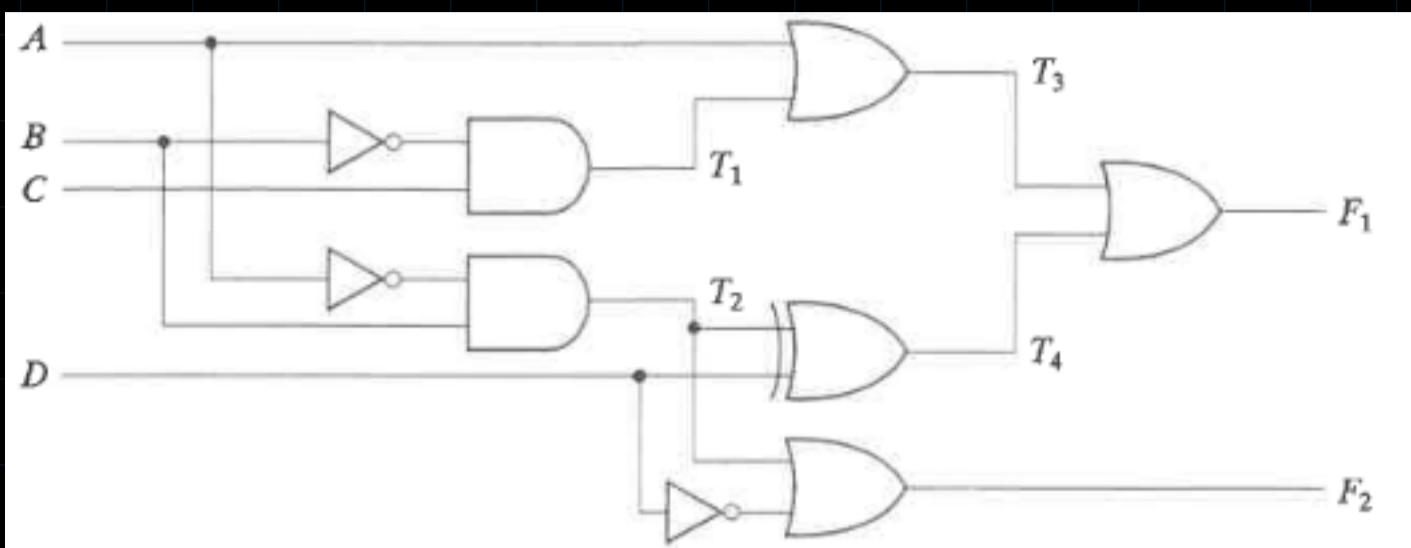


4.1 Consider the combinational circuit shown in Fig P4.1

a) Derive the boolean expression for T_1 through T_4 . Evaluate the outputs F_1 and F_2 as a function of four inputs

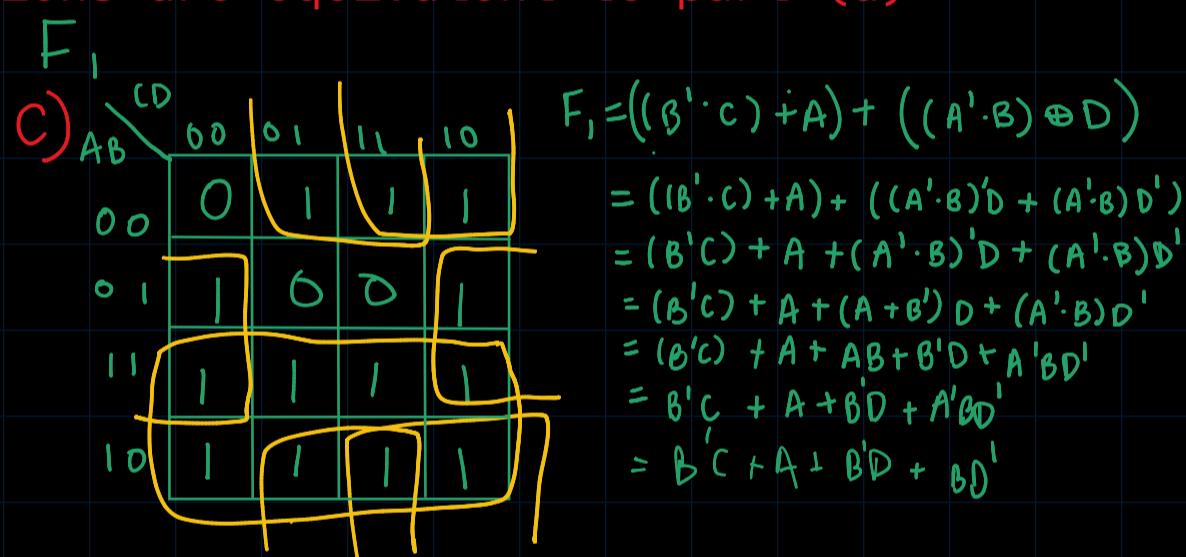


$$\begin{aligned}
 T_1 &= B' \cdot C \\
 T_2 &= A' \cdot B \\
 T_3 &= (B' \cdot C) + A \rightarrow (T_3 + A) \\
 T_4 &= (A' \cdot B) \oplus D \rightarrow (T_2 \oplus D) \\
 F_1 &= ((B' \cdot C) + A) + ((A' \cdot B) \oplus D) \\
 F_2 &= (A' \cdot B) + \overline{D} \Rightarrow T_2 + \overline{D}
 \end{aligned}$$

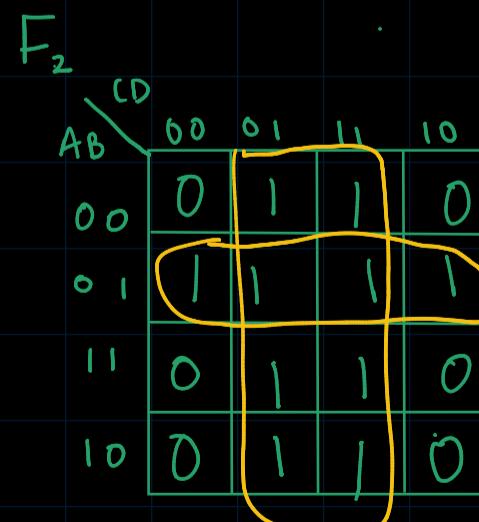
b) List the truth table with 16 binary combinations of the four input variables. Then list binary values for T_1-T_4 and F_1, F_2 on table

c) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified expressions are equivalent to part (a)

	A	B	C	D	T_1	T_2	T_3	T_4	F_1	F_2
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	1	1	
0	0	1	0	1	0	1	0	1	0	
0	0	1	1	1	0	1	1	1	1	
0	1	0	0	0	1	0	1	1	1	
0	1	0	1	0	1	0	0	0	1	
0	1	1	0	0	1	0	1	1	1	
1	0	0	0	0	0	1	0	1	0	
1	0	0	1	0	0	1	1	1	1	
1	0	1	0	1	0	1	0	1	0	
1	0	1	1	1	0	1	1	1	1	
1	1	0	0	0	0	1	0	1	0	
1	1	0	1	0	0	1	1	1	1	
1	1	1	0	0	1	0	1	0	0	
1	1	1	1	1	1	1	1	1	1	



$$F(A, B, C, D) = A + BD' + B'D + BC'$$

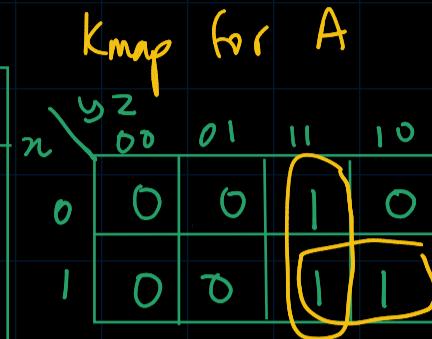


$$F(A, B, C, D) = D + A'B$$

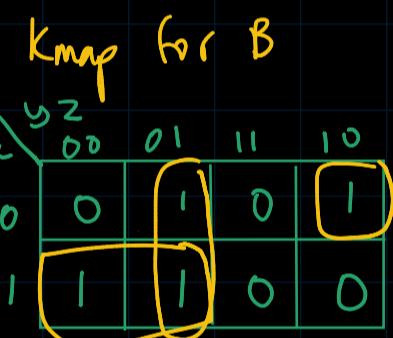
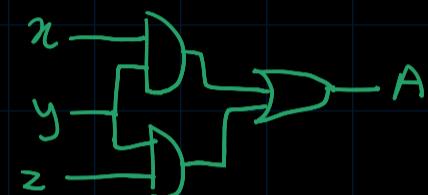
4.5 Design a combinational circuit with three inputs x,y and z and three outputs A,B,C. When the binary input is 0,1,2,or 3, the binary output is one greater than the input. When the binary input is 4,5,6 or 7, the binary output is two less than input

IN	OUT
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

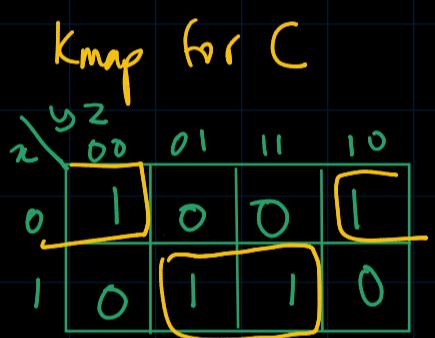
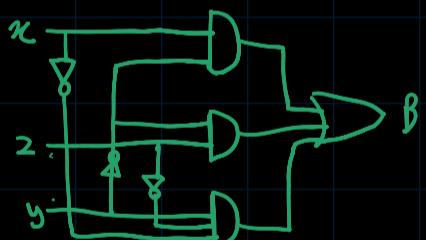
x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	1	0	1



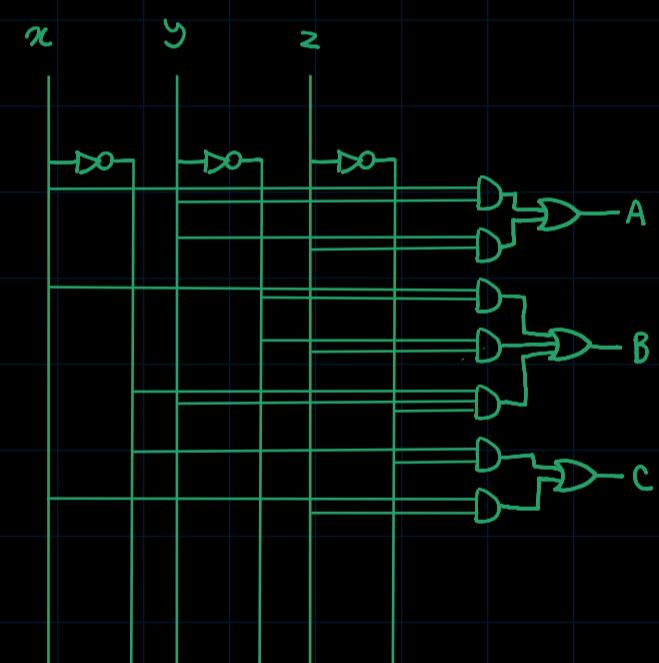
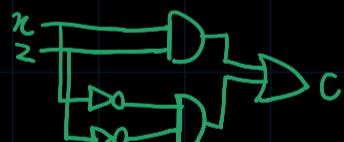
$$F_A(x, y, z) = xy + yz$$



$$F_B(x, y, z) = \bar{x}y + \bar{y}z + x\bar{y}z$$

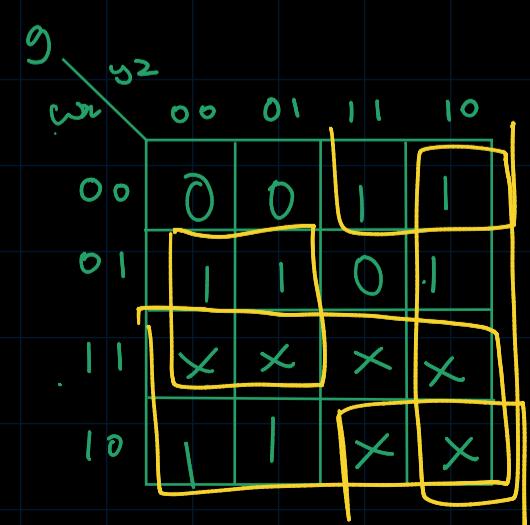


$$F_C(x, y, z) = \bar{x}\bar{z} + xz$$

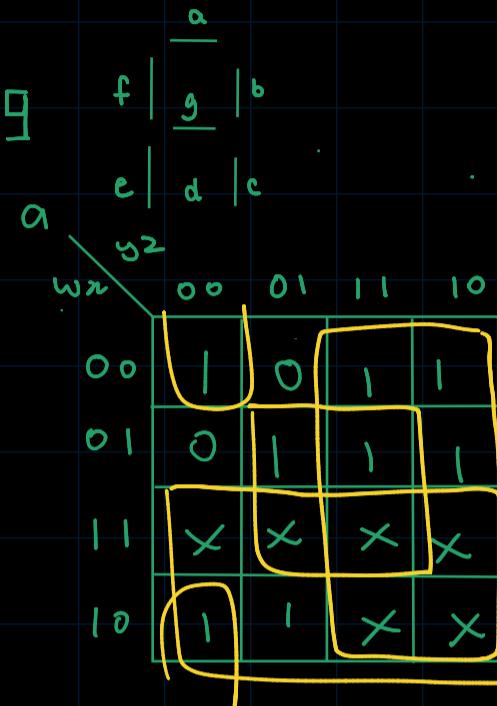


4.9 A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display. Using a truth table and Karnaugh maps, design the BCD-to-seven segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display

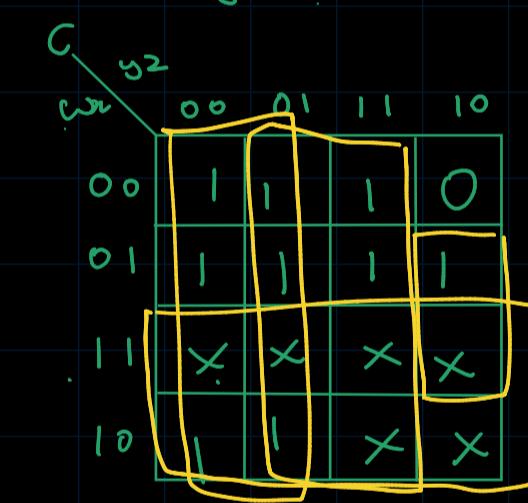
w	x	y	z	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	1	1	1	1	1	1	1	0	
0	0	0	1	0	1	1	0	0	0	0	0	0	
0	0	1	0	1	1	1	0	1	1	0	1		
0	0	1	1	1	1	1	1	0	0	1			
0	1	0	0	0	1	1	0	0	0	1			
0	1	0	1	1	0	1	1	0	1	1			
0	1	1	0	1	0	1	1	1	1	1			
0	1	1	1	1	1	1	1	0	0	0	0		
1	0	0	0	1	1	1	1	1	1	1	1		
1	0	0	1	1	1	1	1	0	1	1			
1	0	1	0	X	X	X	X	X	X	X			
1	0	1	1	X	X	X	X	X	X	X			
1	1	0	0	X	X	X	X	X	X	X			
1	1	0	1	X	X	X	X	X	X	X			
1	1	1	0	X	X	X	X	X	X	X			
1	1	1	1	X	X	X	X	X	X	X			



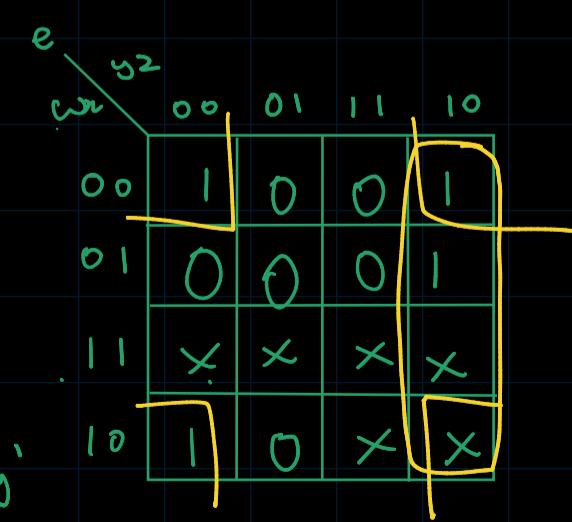
$$F_g = w + yz' + x'y + xy'$$



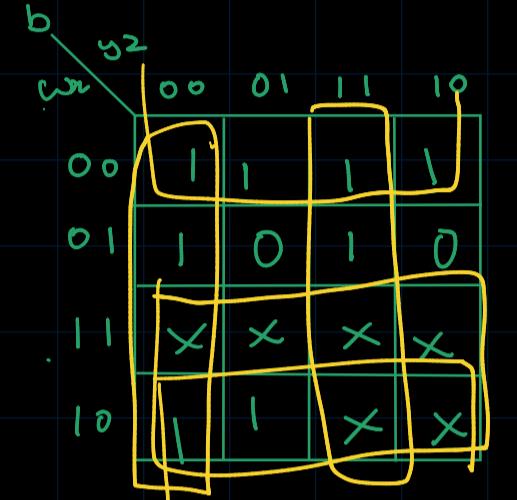
$$F_a = y + w + xz + x'y'z'$$



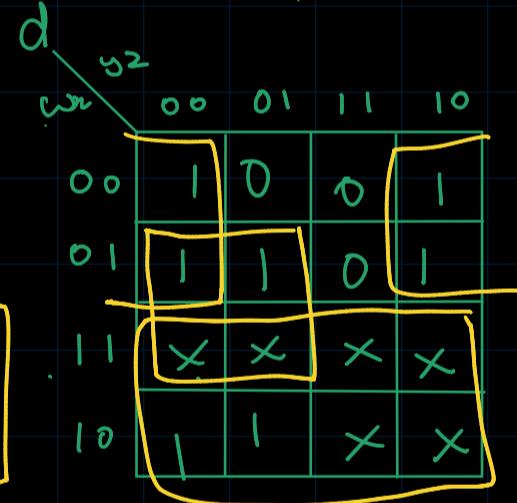
$$F_c = w + y' + z + xy'z'$$



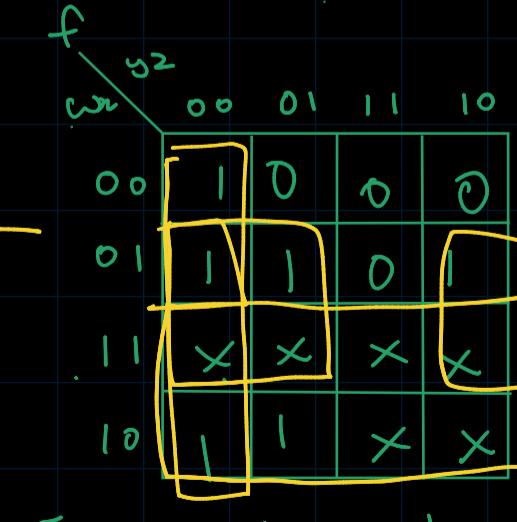
$$F_e = yz' + x'z'$$



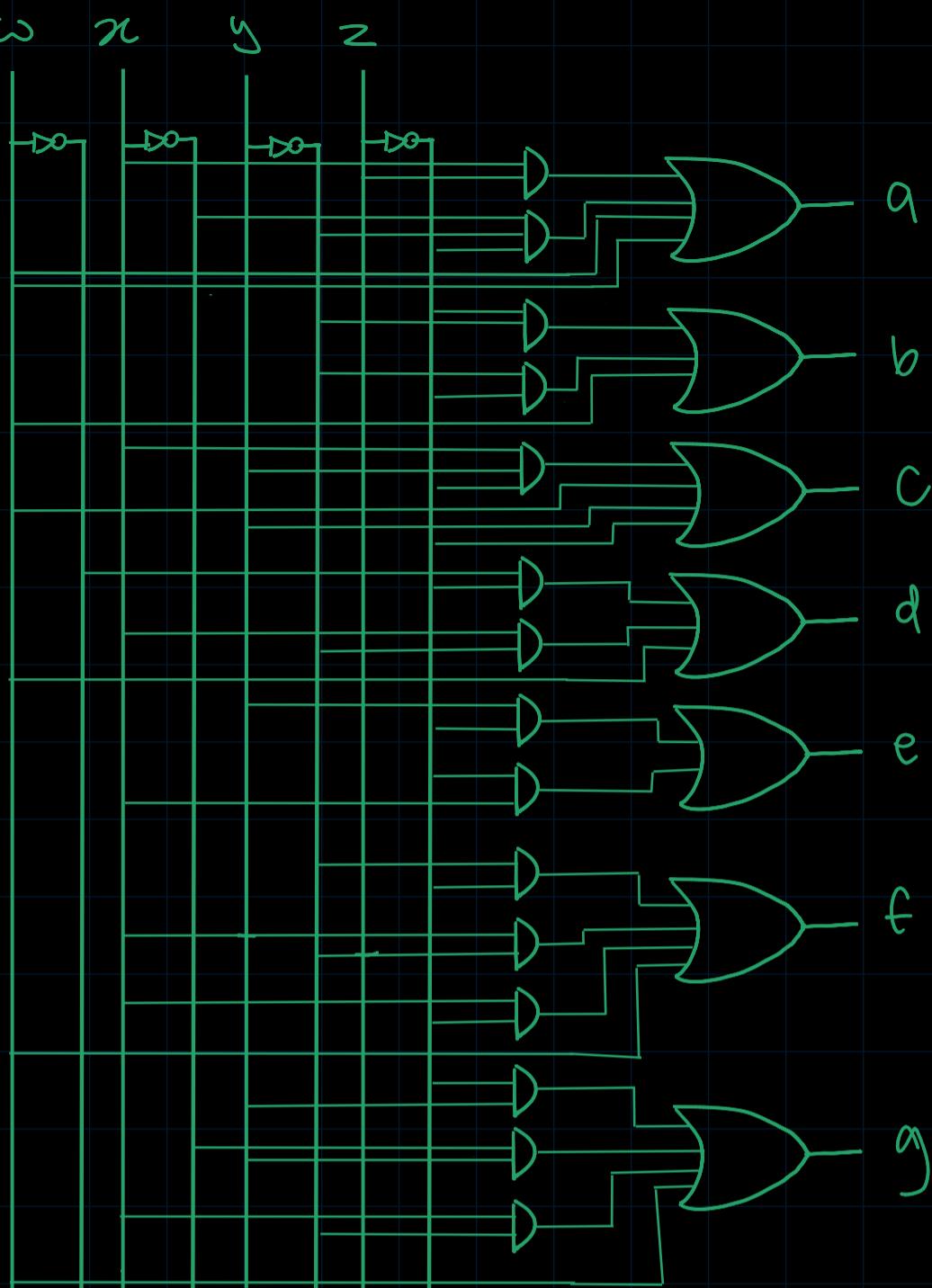
$$F_b = w + x' + y'z' + yz$$



$$F_d = w + w'z' + xy'$$



$$F_f = w + y'z' + xy' + xz'$$

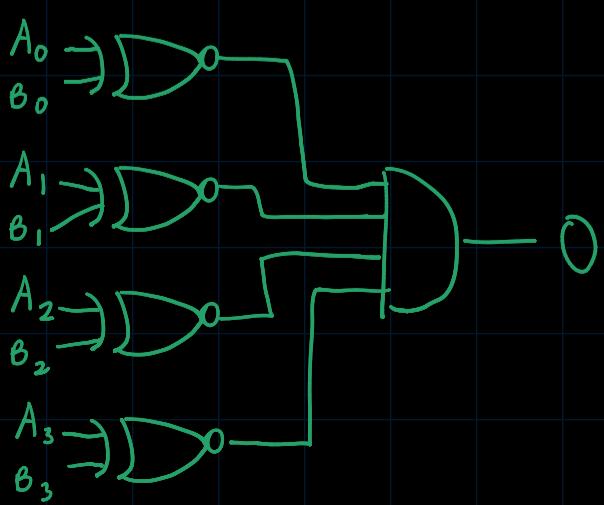


4.21 Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise

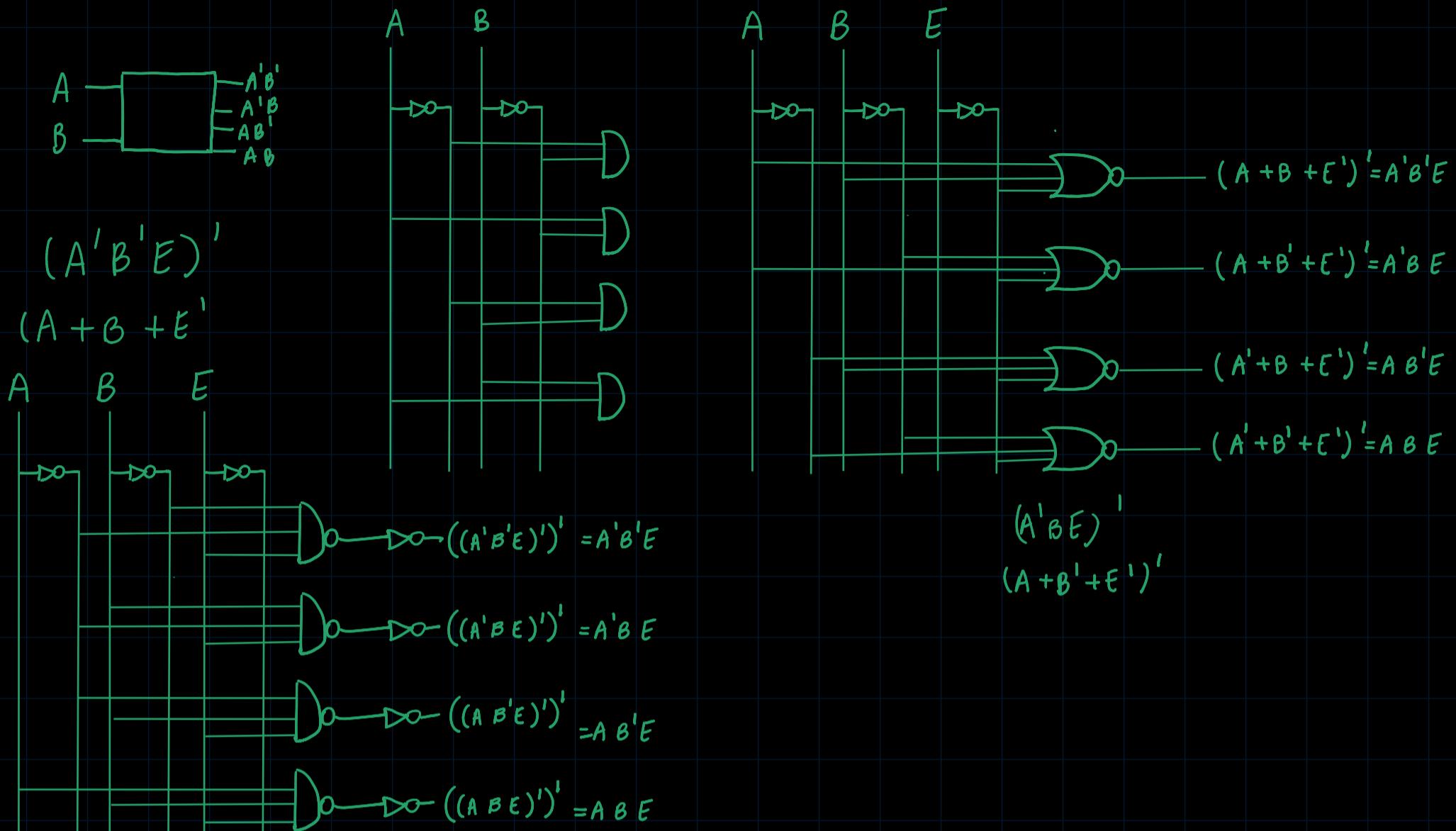
$$A: A_0, A_1, A_2, A_3$$

$\text{xNOR}(\text{if } x == y)$

$$B: B_0, B_1, B_2, B_3$$



4.23 Draw the logic diagram 2-to-4 line decoder using (a) NOR gates only and (b) NAND gates only. Include an enable input



4.27 A combinational circuit is specified with three Boolean functions. Implement the circuit with a decoder constructed with NAND gates and NAND or AND gates connected to decoder. Minimize number of inputs in the external gates

$$F_1(A, B, C) = \sum(1, 4, 6)$$

$$F_2(A, B, C) = \sum(3, 5)$$

$$F_3(A, B, C) = \sum(2, 4, 6, 7)$$

		BC			
		00	01	11	10
A	0	0	1	0	0
	1	1	0	0	1

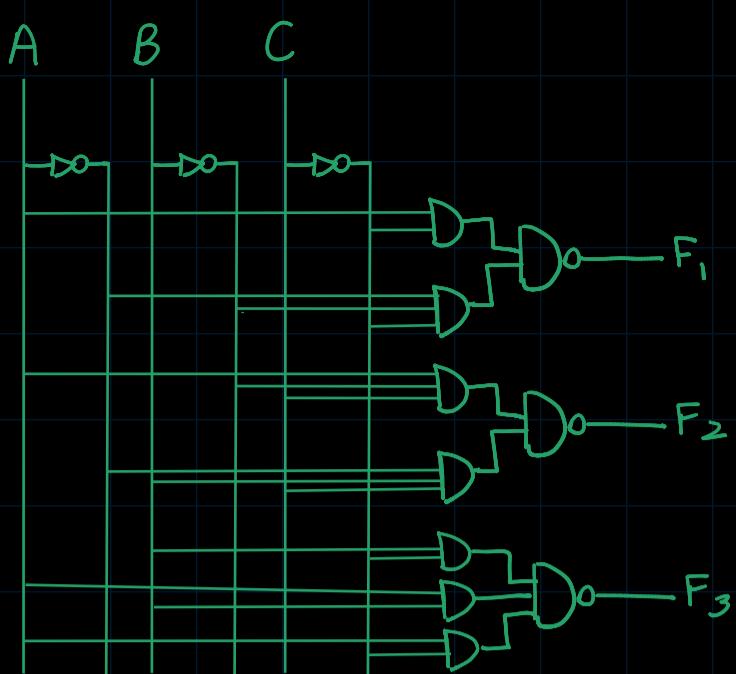
		BC			
		00	01	11	10
A	0	0	0	1	0
	1	0	1	0	0

		BC			
		00	01	11	10
A	0	0	0	0	1
	1	1	0	1	1

$$F_1 = AC' + A'B'C$$

$$F_2 = AB'C + A'BC$$

$$F_3 = BC' + AB + AC'$$



4.28 Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

$$\begin{aligned} a) \quad F_1 &= x'y_2' + xz \\ F_2 &= xy_2' + x'y \\ F_3 &= x'y_1'z' + xy \end{aligned}$$

	x	y	z	00	01	11	10
F_1	0	0	0	0	0	0	1
	1	0	1	0	1	1	0

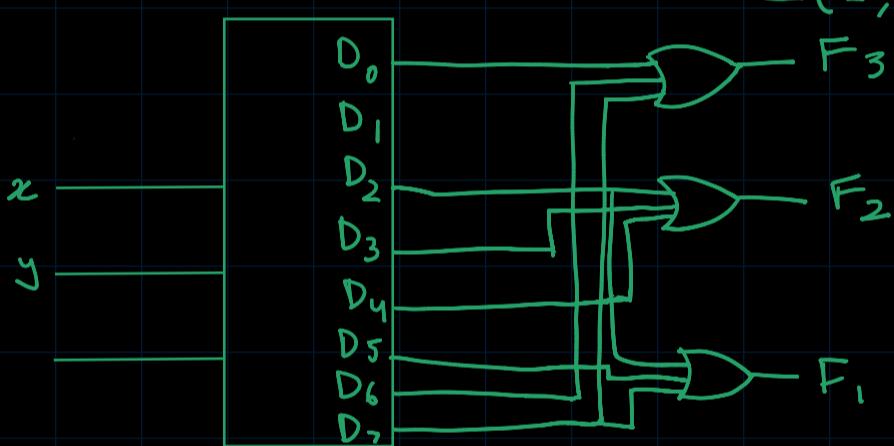
$\Sigma(2, 5, 7)$

	x	y	z	00	01	11	10
F_2	0	0	0	0	0	1	1
	1	0	1	0	1	0	0

$\Sigma(2, 3, 5)$

	x	y	z	00	01	11	10
F_3	0	1	0	0	1	0	0
	1	0	0	1	0	1	1

$\Sigma(0, 6, 7)$



4.33 Implement a full adder with two 4×1 multiplexers

x	y	z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = z'$, $C = 0$

$S = z'$, $C = z$

$S = z'$, $C = z$

$S = z$, $C = 1$

