Part 1

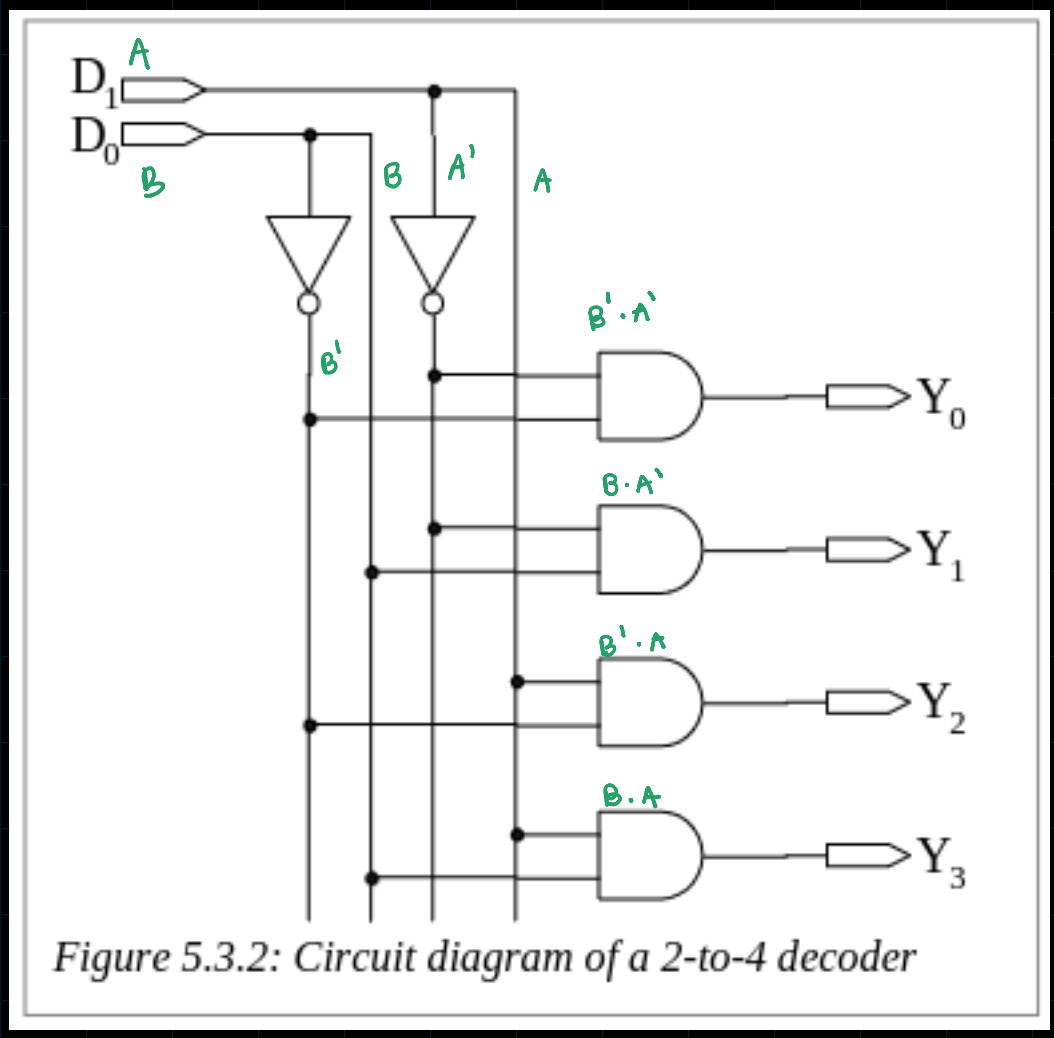

Figure 5.3.2: Circuit diagram of a 2-to-4 decoder

$Y_0 = D_1' \cdot D_0'$

$Y_1 = D_1' \cdot D_0$

$Y_2 = D_1 \cdot D_0'$

$Y_3 = D_1 \cdot D_0$

Y0 Output		
D1	D0	D1'.D0'
0	0	1
0	1	0
1	0	0
1	1	0

Y1 Output		
D1	D0	D1'.D0'
0	0	0
0	1	1
1	0	0
1	1	0

Y2 Output		
D1	D0	D1.D0'
0	0	0
0	1	0
1	0	1
1	1	0

Y3 Output		
D1	D0	D1.D0
0	0	0
0	1	0
1	0	0
1	1	1

Part 3

a) 4-1 Multiplexer

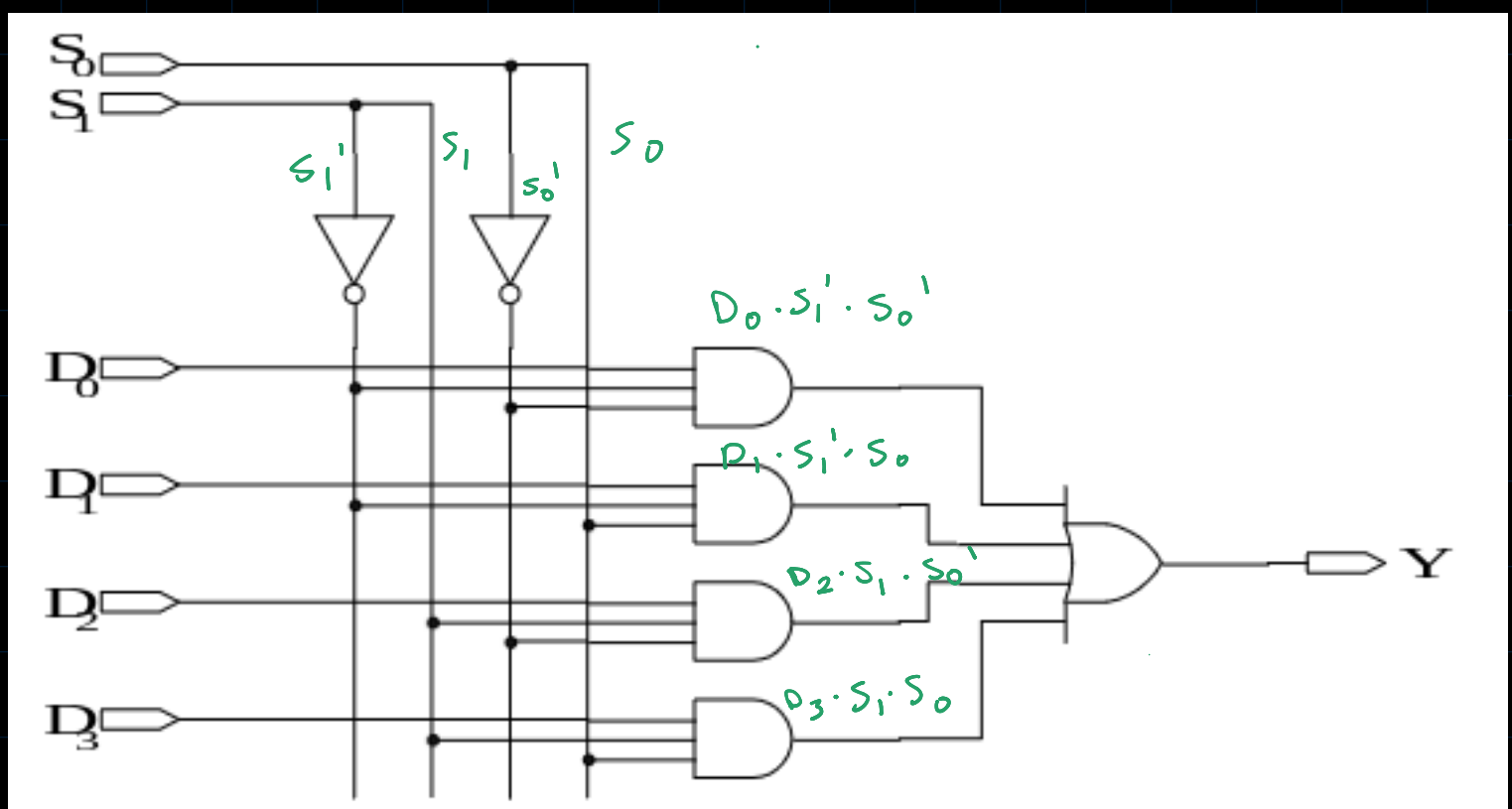

Figure 5.3.5: Multiplexer

S1	S0	D0	D1	D2	D3
0	0	0	X	X	X
0	0	1	X	X	X
0	1	X	0	X	X
0	1	X	1	X	X
1	0	X	X	0	X
1	0	X	X	1	X
1	1	X	X	X	0
1	1	X	X	X	1

$Y = (D_0 S_1' S_0') + (D_1 S_1' S_0) + (D_2 S_1 S_0') + (D_3 S_1 S_0)$

3. D_1