Iti1100 final exam pdf

Digital Systems I (University of Ottawa)

Université d'Ottawa
Faculté de génie

École de science informatique
et de génie électrique

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Canada's university

University of Ottawa
Faculty of Engineering

School of Electrical Engineering
and Computer Science

Student Name (Please print)_____

Student Number_____ Section:_____

ITI1100-Digital Systems I

FINAL EXAMINATION

(closed-book)

Winter 2021

Duration : 3 hours

+ 1 hour for printing, scanning and uploading the exam paper

Instructions:

- Write your name, student number and section as well as all of your answers on this examination handout only.
- Answer ALL questions and state any assumptions that are utilized in your answers.
- **This is a closed-book examination.**
- Use the provided space to answer the following questions. If more space is needed, use the back of the pages, however indicate doing so.
- Show all your calculations to obtain full marks.
- **Calculators are NOT allowed.**
- Read all the questions carefully before you start.

Question	Points	Percentage
1		20 %
2		30%
3		20%
4		20%
5		10%
Total		100%

Question 1 (20 points)

a) The subsequent numbers are represented in signed 2's complement notation. Perform the following operations (your results should be represented using the same notation as the operands).

(i) $(001011)_2 - (111011)_2$

(ii) $(011111)_2 + (010000)_2$

(iii) $(100111)_2 + (101000)_2$

b) **Check your operations** by converting both your operands and your results into decimal numbers and indicate the cases **where overflow occurs**.

c) Convert the following two numbers, $(8.5)_{10}$ and $(2.25)_{10}$, into binary and perform the following operations in signed binary number format using 1's complement:

(i) $(8.5)_{10} + (2.25)_{10}$ (ii) $(2.25)_{10} - (8.5)_{10}$

Question 2 (30 points)

Part-A

Given the logic function $F(A,B,C,D) = \Sigma m(1,3,5,8)$ together with the *don't care* conditions $d(A,B,C,D) = \Sigma d(2,7,12,13,14)$,

(i) Fill in completely the truth table of the logic function. Use the Karnaugh-map method to find the simplest sum-of-products expression of function ***F.***

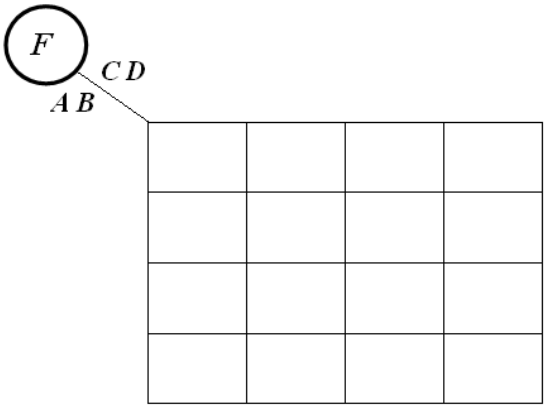
(ii) Implement the minimized function with NAND gates only.

Note: You can use NAND gates with any number of inputs you may need. Assume that the input variables are available in both true and complemented form

(iii) Using the truth table from part (i), express the same logic function in a product of sums (maxterms) form.

(iv) Simplify your function in product of sums by using the Karnaugh-map.

A	B	C	D	F



Part-B

(i) Given the following Boolean function

$F(A,B,C,D) = \Sigma m(0,3,4,7,12)$ together with the *don't care* conditions $d(A,B,C,D) = \Sigma d(1, 6, 9, 10, 11, 13, 14)$,

Implement the function ***F*** constructed with a 4-to-16 active high decoder and OR gate (with required number of inputs) only.

(ii) Given the following Boolean function

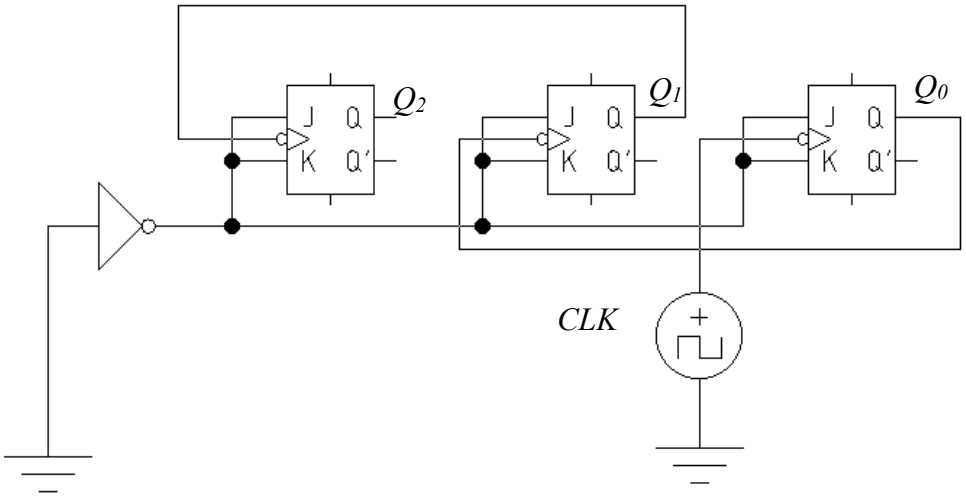
$$F(A,B,C) = \Sigma m(0,1,3,6)$$

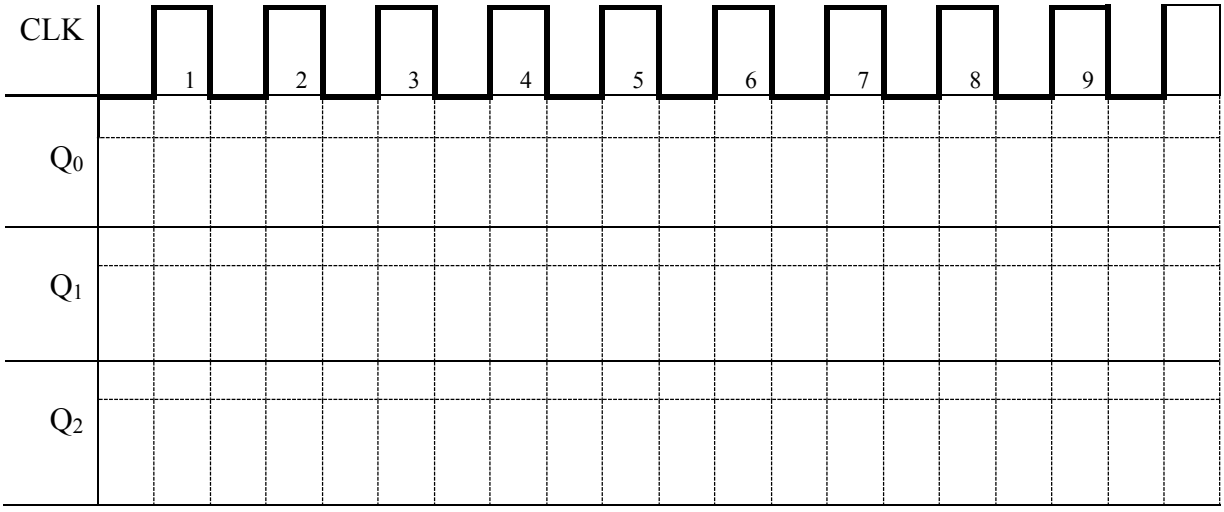
Build the truth table and implement the function F using a **4-to-1 multiplexer**.

Question 3 (20 points)

The following figure represents a sequential circuit. This circuit is built from 3 J-K flip-flops to perform a specific function.

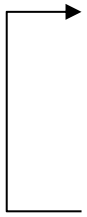
- **(i)** Draw the timing diagram of the flip-flop outputs through the first 9 clock pulses, considering that the initial state of every flip-flop is 0.
- **(ii)** Draw the state diagram of the circuit
- **(iii)** Explain the function implemented by this circuit.
- **(iv)** Add the necessary logic gate, to the figure, with asynchronous inputs to CLEAR (**Q_0=0,Q_1=0, Q_2=0**) the J-K flip-flops when **Q_2=1 and Q_1=0, and Q_0=1**





Question 4 (20 points)

Design a synchronous counter having the count sequence given by the following table. **Use negative edge-triggered T flip-flops.**



Q_2	Q_1	Q_0
0	0	0
0	1	0
1	1	0
0	1	1
1	0	1
1	1	1

(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the T flip-flops as well.
(iii) Using Karnaugh-maps, find the minimal **sum-of-products (SOP)** form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states".
(iv) Draw the logic circuit of the counter.

Question 5 (10 points)

Design a sequential circuit with two JK flip-flops A and B, and one input W. When W = 0, the state of the circuit remains the same. When W = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

(i) Give a table that shows:
   a. the input values
   b. the states (present and next) for the J-K flip-flop

(ii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the J-K flip-flops.