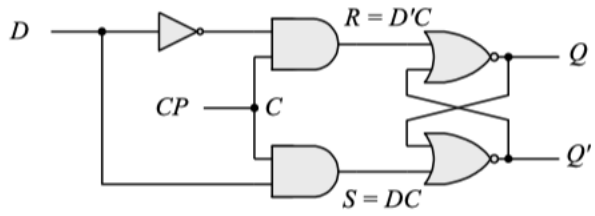
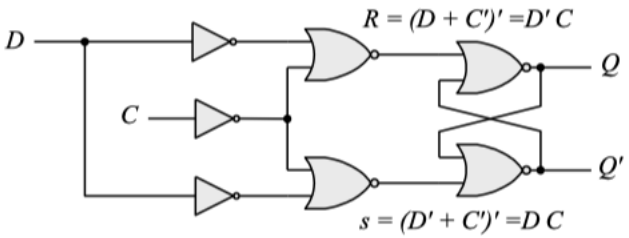
Synchronous Sequential Logic

1) The D latch of Fig. 5.6 is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.

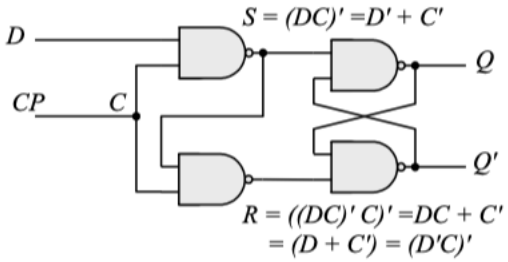
(a)



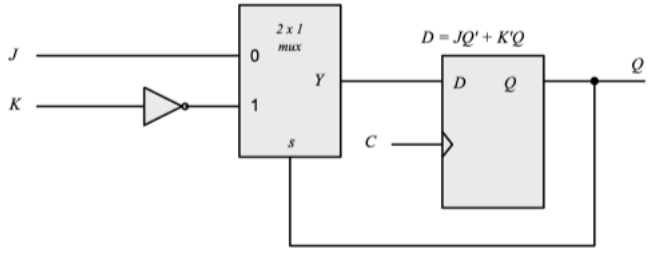
(b)



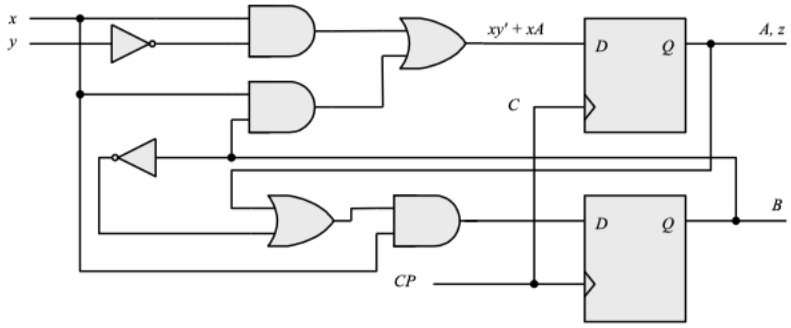
(c)



2) Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.



3) A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations:

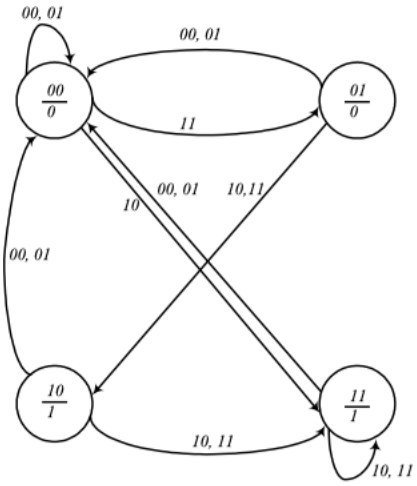


(b)

$A(t+1) = xy' + xB$
$B(t+1) = xA + xB'$
$z = A$

Present state		Inputs		Next state		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

(c)



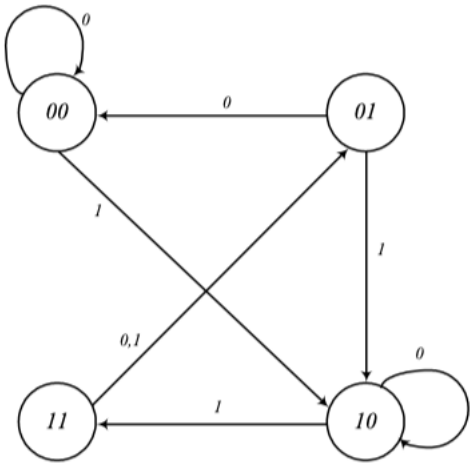
4) A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

Answer of (a) on the left, and the answer of (b) on the right:

$J_A = x$ $\quad K_A = B$
$J_B = x$ $\quad K_B = A'$

$A(t+1) = J_A A' + K_A' A = xA' + B'A$
$B(t+1) = J_B B' + K_B' B = xB' + AB$

x	A	B	$xA' + B'A$	$xB' + AB$
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1



5) A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

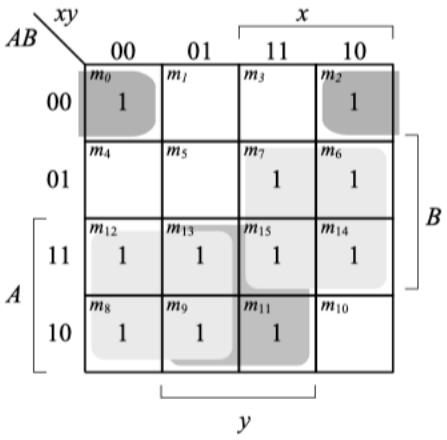
(a) $J_A = Bx + B'y'$ $\quad J_B = A'x$

$K_A = B'xy'$ $\quad K_B = A + xy'$ $\quad z = Axy + Bx'y'$

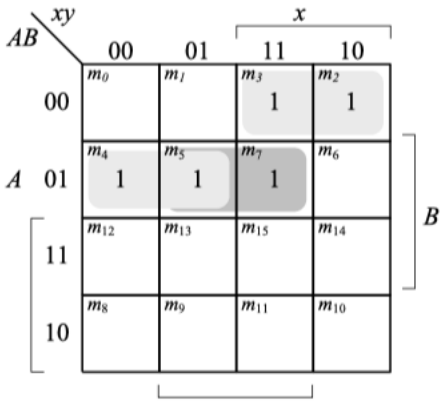
(b)

Present state		Inputs		Next state		Output	FF Inputs			
A	B	x	y	A	B	z	J_A	K_A	J_A	J_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	0
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	1	1	0	0	1

(c)



$A(t+1) = Ax' + Bx + Ay + A'B'y'$



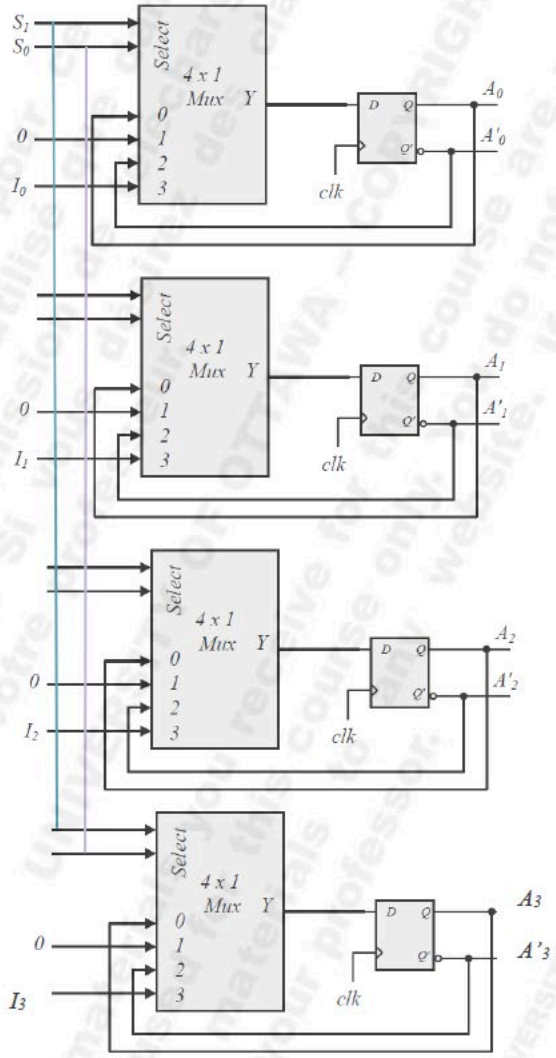
$B(t+1) = A'B'x + A'B'(x' + y)$

Registers and Counters

6) Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs s_1 and s_0 . The register operates according to the following function table.

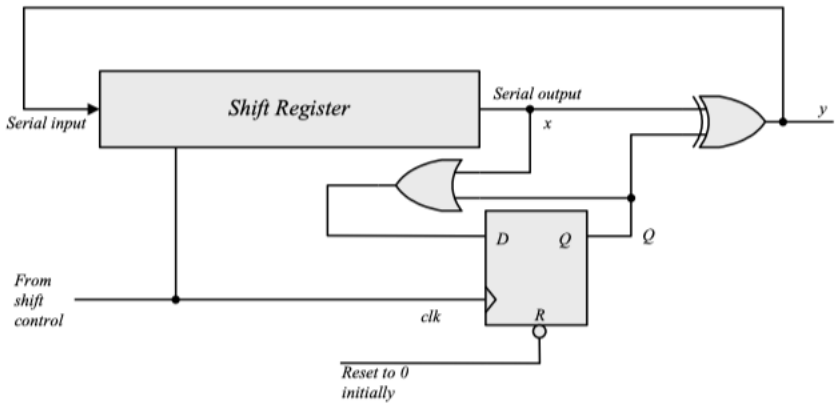
Stage of register: (s1, s0): (0,0) – no change, (1,0) – complement outputs (0,1) – Synchronous clear, (1,1) = Load parallel data.

Stage logic diagram:



7) Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.

Note that y = x if Q = 0, and y = x' if Q = 1. Q is set on the first 1 from x.
Note that x ⊕ 0 = x, and x ⊕ 1 = x'.



8) A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if:

Answer:

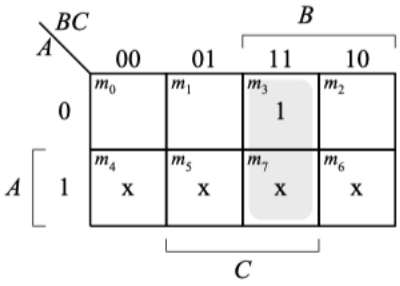
(a) A count down counter.

(b) A count up counter.

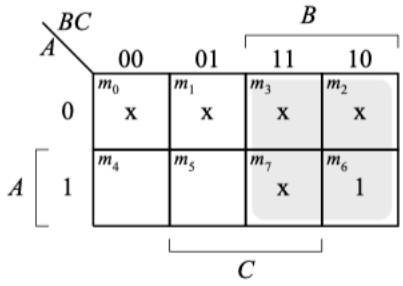
9) A digital system has a clock generator that produces pulses at a frequency of 80 MHz. Design a circuit that provides a clock with a cycle time of 50 ns.

10) Using JK flip flops, design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6.

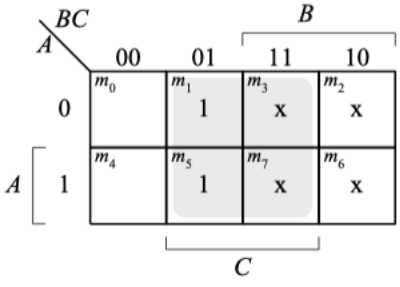
Present state *ABC*	*Next state* *ABC*	*Flip-flop inputs* J_A	K_A	J_B	K_B	J_C	K_C
000	001	0	x	0	x	1	x
001	010	0	x	1	x	x	1
010	011	0	x	x	0	1	x
011	100	1	x	x	1	x	1
100	100	x	x	0	0	1	x
101	110	x	x	1	x	x	1
110	000	x	x	x	1	0	x
111	xxx	x	x	x	x	x	x



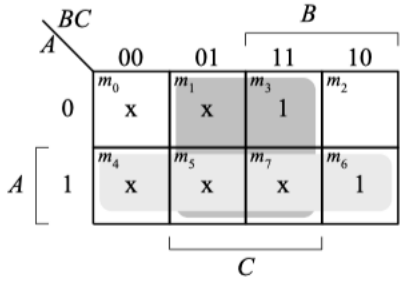
$J_A = BC$



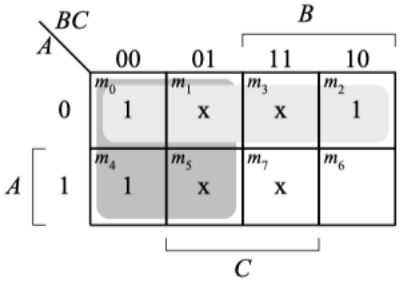
$K_A = B$



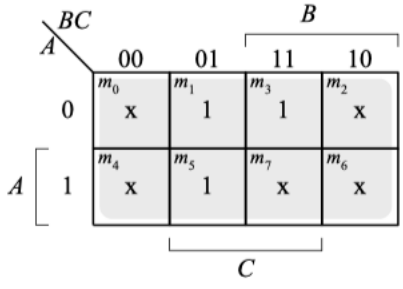
$J_B = C$



$K_B = A + C$



$J_C = A' + B'$



$K_C = 1$