Université d'Ottawa · University of Ottawa

Faculté de Génie - Faculty of Engineering
ITI1100C Digital Systems I –Assignment 4

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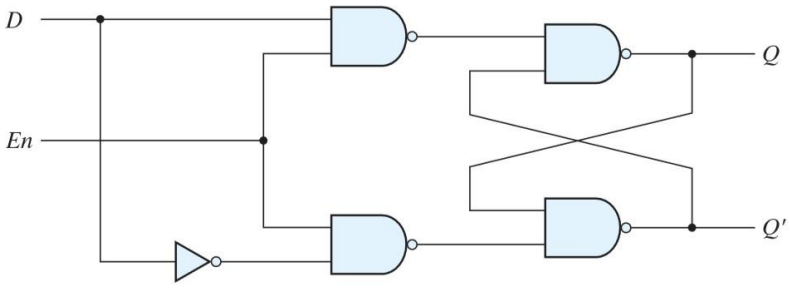
Professor: Mohammad Al Ridhawi
(malridha@uottawa.ca)

Synchronous Sequential Logic

1) The D latch of Fig. 5.6 is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.

(a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.
(b) Use NOR gates for all four gates. Inverters may be needed.
(c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate in Fig. 5.6 (the gate that goes to the SR latch) to the input of the lower gate (instead of the inverter output).



(a) Logic diagram

En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

FIGURE 5.6

2) Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

3) A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations:

$$A(t + 1) = xy' + xB$$
$$B(t + 1) = xA + xB'$$
$$z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

4) A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

$$J_A = x \qquad K_A = B$$
$$J_B = x \qquad K_B = A'$$

(a) Derive the state equations $A(t + 1)$ and $B(t + 1)$ by substituting the input equations for the J and K variables.
(b) Draw the state diagram of the circuit.

5) A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$

$$J_B = A'x \qquad K_B = A + xy'$$

$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c) Derive the state equations for A and B.

Registers and Counters

6) Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs s_1 and s_0 . The register operates according to the following function table.

s_1	s_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

7) Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.

8) A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if:
(a) the normal outputs of the flip-flops are connected to the clock and
(b) the complement outputs of the flip-flops are connected to the clock?

9) A digital system has a clock generator that produces pulses at a frequency of 80 MHz. Design a circuit that provides a clock with a cycle time of 50 ns.

10) Using JK flip-flops, design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6.