Lab 4 – ARITHMETIC CIRCUITS

ITI 1100A- Digital Systems
Winter 2024

School of Electrical Engineering and Computer Science
University of Ottawa

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Experiment Date:09/03/2024
Submission Date:19/03/2024

Objectives:

1. Develop and simulate a complete full adder.
2. Integrate the full adder into an 8-bit adder/subtractor.
3. Construct a hierarchical design incorporating elements like full adders, subtractors, and parallel multipliers using the QUARTUS II graphical editor.
4. Devise an overflow detection mechanism for implementation within a two's complement adder/subtractor.

Equipment

- Quartus sp13.0 64bit
- Altera DE2-115 Cyclone IV E EP4CE115F28C7

Part I: 1 Bit full Adder

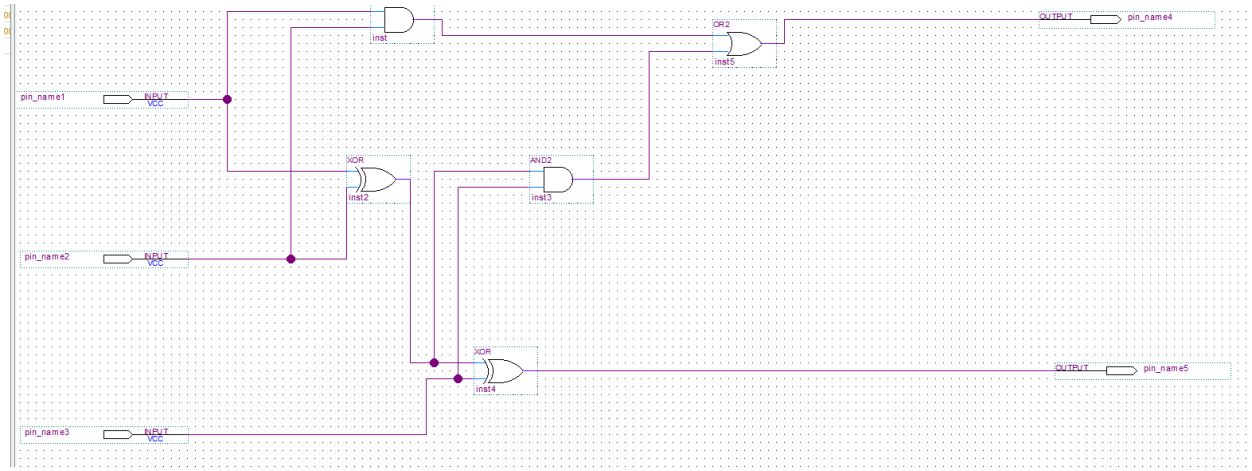

Figure 1:Full Bit Adder comprised of 2 NOR gates and 2 AND gates and 1 OR

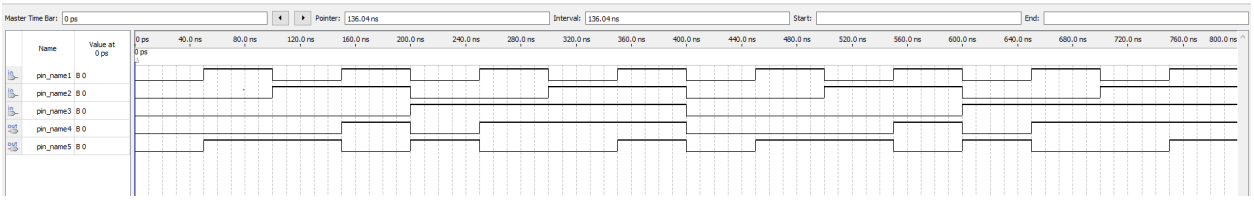

Figure 2: Simulation diagram of a circuit in Figure 1.

Part II: Parallel Adder:

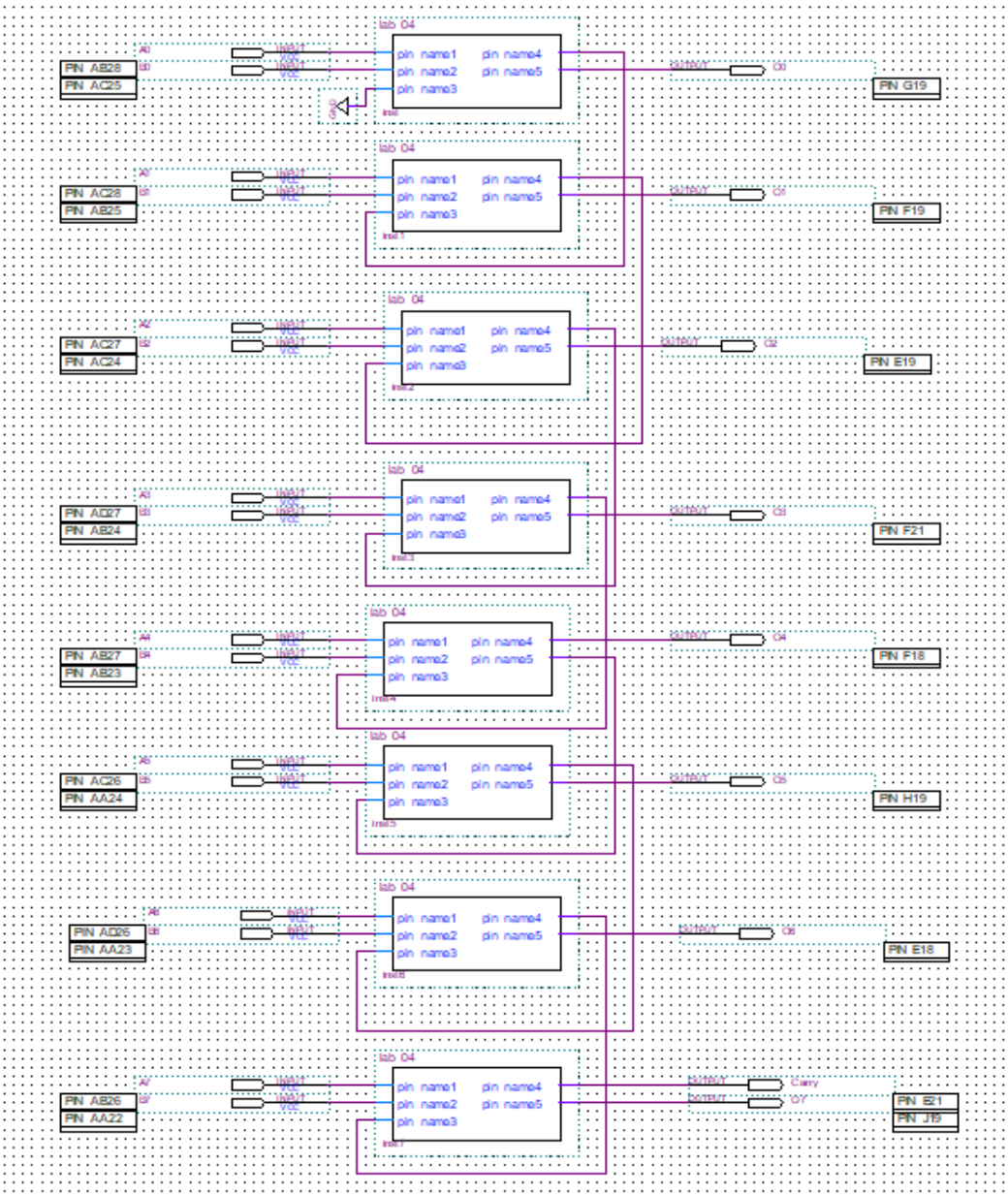

Figure 3: 8 parallel Full-Bit Adders

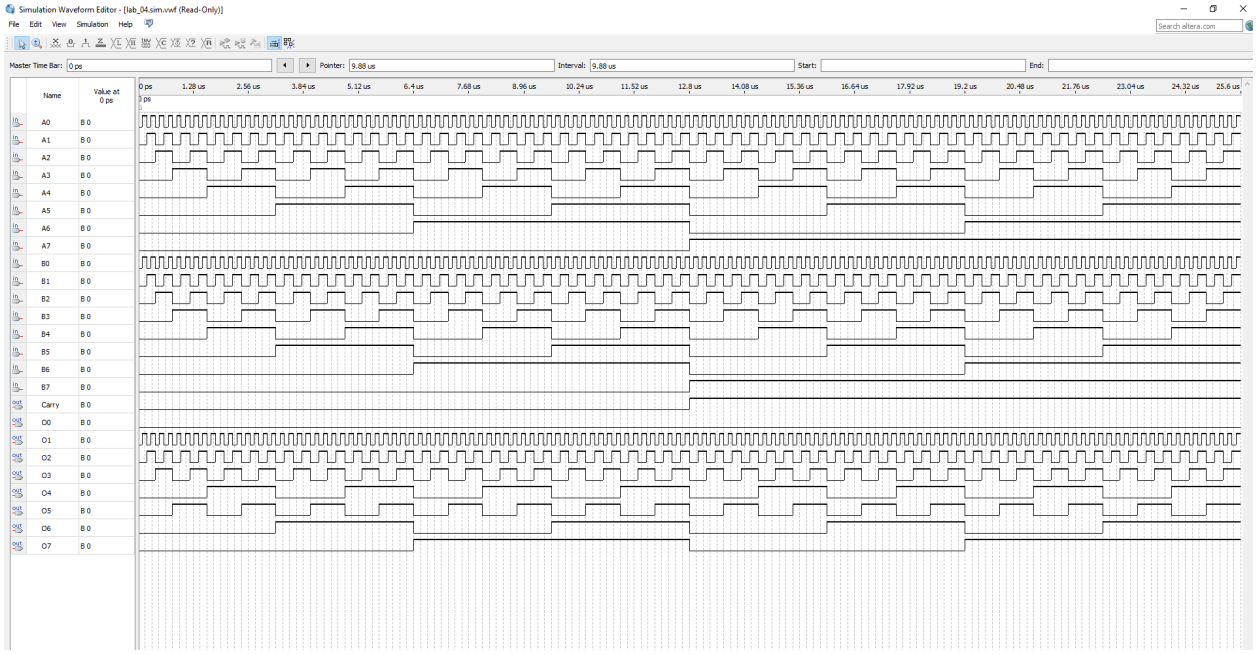

Figure 2: Simulation diagram of a circuit in Figure 1.

Table 1

Grid	Binary Inputs	Carry	Binary Sum	Hex Equivalent
1	01111111 + 00000001	0	10000000	(80)16
2	11111111 + 00000001	1	00000000	(0)16
3	11000000 + 01000000	1	00000000	(0)16
4	**11000000 + 10000000**	1	01000000	(40)16

Part III: Two's Complement Adder/Subtractor

Table 2						
Grid	Binary Inputs	Overflow	Carry	Binary Sum	Hex Equivalent	**Two's Compl.**
1	01111111 + 00000001	1	0	10000000	(80)16	10000000
2	11111111 + 00000001	1	1	00000000	(0)16	00000000
3	00000000 - 00000001	0	0	11111111	(FF)16	00000001
4	00000000 - 01111111	0	0	10000001	(81)16	01111111
6	11000000 + 01000000	1	1	00000000	(0)16	00000000
6	**11000000 + 10000000**	1	1	01000000	(40)16	11000000

Comparison of Expected Data and Processing Data

PART 1 – One-Bit Full Adder

A	B	C_IN	SUM	C_OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From analyzing the truth table, it becomes evident that the outputs of the circuits align with the anticipated outputs of a one-bit full adder.

PART 2 – Parallel Adder

Comparison of results simulation with table 1

Simulation results			
Grid	**Binary inputs (A7,A6,A5,A4,A3,A2,A1,A0 +B7,B6,B5,B4,B3,B2,B1,B0)**	**C_OUT (Carry)**	**Binary Sum (SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0)**
1 (0ps – 200ns)	01111111 + 00000001	0	10000000
2 (200ns-400ns)	11111111 + 00000001	1	00000000
3 (400ns-600ns)	11000000 + 01000000	1	00000000
4 (600ns-800ns)	11000000 + 10000000	1	01000000

Table 1

TABLE 1				
Grid	**Binary inputs**	**Carry**	**Binary Sum**	**Hex Equivalent**
1	01111111 + 00000001	0	10000000	7F + 01 = 80
2	11111111 + 00000001	1	00000000	FF + 01 = 00
3	11000000 + 01000000	1	00000000	C0 + 40 = 00
4	11000000 + 10000000	1	01000000	C0 + 80 = 40

The simulation outcomes correspond exactly to the data presented in Table 1.

PART 3 – Two's Complement Adder/Subtractor
Comparison of results simulation with Table 2

Simulation Results				
Grid	**Binary Inputs (A7,A6,A5,A4,A3,A2,A1,A0 +B7,B6,B5,B4,B3,B2,B1,B0)**	**V (Overflow)**	**C_OUT (Carry)**	**Binary Sum (SUM7, SUM6, SUM5, SUM4, SUM3, SUM2, SUM1, SUM0)**
1 (0ps-150ns)	01111111 + 00000001	1	0	10000000
2 (150ns-300ns)	11111111 + 00000001	0	1	00000000
3 (300ns-450ns)	00000000 - 00000001	0	0	11111111
4 (450ns-600ns)	00000000 - 01111111	0	0	10000001
5 (600ns-750ns)	11000000 + 01000000	0	1	00000000
6 (750ns-900ns)	11000000 + 10000000	1	1	01000000

Table 2

TABLE 2						
Grid	**Binary Inputs**	**Overflow**	**Carry**	**Binary Sum**	**Hex Equivalent**	**Two's Complement**
1	01111111 + 00000001	1	0	10000000	7F + 01 = 80	
2	11111111 + 00000001	0	1	00000000	FF + 01 = 00	
3	00000000 - 00000001	0	0	11111111	00 - 01 = FF	11111111 = FF = (-1)10
4	00000000 - 01111111	0	0	10000001	00 - 7F = 81	10000001 = 81 = (-127)10
5	11000000 + 01000000	0	1	00000000	C0 + 40 = 00	
6	11000000 + 10000000	1	1	01000000	C0 + 80 = 40	

As we can see the simulation results are the same as the data found in table 2.

As we can see the simulation results are the same as the data found in table 3.

Discussion and Conclusion

The experiment set out to accomplish multiple goals, beginning with the creation and simulation of a full adder and its integration into an 8-bit adder/subtractor. Additionally, it aimed to construct a hierarchical design incorporating full adders, subtractors, and parallel multipliers using the QUARTUS II graphic editor, while also designing an overflow detector for a two's complement adder/subtractor. Predicted outcomes were determined by calculating outputs for different combinations, including the carry input. Through the conducted experiments, these predictions were intended to be validated. In summary, the results matched the anticipated outcomes, effectively demonstrating the experiment's objectives without any deviations.

Challenges

No challenges were encountered

1.

Binary Inputs	Carry	Binary Sum	Hex Equivalent
01111111 + 0000000	0	10000000	(80)_H
11111111 + 0000000	1	00000000	(00)_H
11000000 + 0100000	1	00000000	(00)_H
11000000 + 1000000	1	01000000	(40)_H

2

Binary Inputs	Overflow	Carry	Binary Sum	Hex Equivalent	Two's Complement
01111111 + 00000001	1	0	010000000	(80)_16	10000000
11111111 + 00000001	0	1	100000000	(100)_16	100000000
00000000 - 00000001	1	0	11111111	(FF)_16	00000001
00000000 - 01111111	1	0	10000001	(81)_16	01111111
11000000 + 01000000	0	1	100000000	(100)_16	100000000
11000000 + 10000000	1	1	110000000	(180)_16	010000000