Iti1100 - FINAL EXAM WINTER22

Digital Systems I (University of Ottawa)

Université d'Ottawa
Faculté de génie

École de science informatique
et de génie électrique

uOttawa
L'Université canadienne
Canada's university

University of Ottawa
Faculty of Engineering

School of Electrical Engineering
and Computer Science

Student Name (Please print)_____

Student Number_____ Section:_____

ITI1100-Digital Systems I
Final Examination Winter 2022
Date: April 28, 2022

Time: 2:00PM-5:00PM (3 hours)

Professors: Ahmed Karmouch, Fadi Malek, Wassim El Ahmar

Instructions:

- Answer ALL questions.
- This final examination will last 180 minutes and has 5 main questions.
- This is a closed-book examination.
- Use the provided space to answer the following questions. If more space is needed, use the back of the page.
- State any assumptions and acronyms that are utilized in your answers.
- Write your name and student number
- Show all your calculations to obtain full marks.
- Calculators are NOT allowed.
- Read all the questions carefully before you start.

(The following space is reserved for the professor)

Question	Points	Percentage
1		20%
2		30%
3		15%
4		20%
5		15%
Total		100%

SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

Question 1: (20 points)

(i) The following two numbers are represented in unsigned binary:

A= $(10101)_2$
B= $(10011)_2$

Represent these two numbers in signed 1's complement form and perform the following binary arithmetic operations using the 1's complement method. Use a total of 7 bits to represent both numbers and results including the sign bit.

C = A + B;
D = A - B.

Important note: *Clearly explain your solution! else your mark for the question will be zero!*

Question 2: (30 points)

Given the logic function $F(A,B,C,D) = \Sigma m(1,2,3,4,9,10,11,12)$

(i) Write the truth table of the logic function.
(ii) Use the Karnaugh-map method to find the simplest sum-of-products (SOP) expression of function ***F*.**
(iii) Implement the minimized function with NAND gates only.
(iv) Show that the Boolean function **F** can be constructed using exclusive-OR gates
(v) Express the same logic function in a product-of-sums (POS) form.
(vi) Simplify your function in product-of-sums (POS).
(vii) Use a decoder with external AND gates only to implement F in its product-of-sums (POS) form (assume AND gates with any number of inputs are available).

Note: You can use NAND gates with any number of inputs you may need. Assume, as well, that the input variables are available in both true and complemented form.

Question 3: (15 points)

Design a modulo-5 ripple (asynchronous) down-counter with D flip-flops and draw the corresponding logic circuit.

(i) Build the state diagram and extract the state table
(ii) Draw the logic circuit
(iii) What is the maximum modulus of the counter?

Question 4: (20 points)

Design a synchronous binary up-counter using 4 negative edge-triggered JK flip-flops provided with a clock. The states (sequences) 1100, 1001 and 1000 are considered as unused states.

(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the JK flip-flops as well.
(iii) Using Karnaugh-maps, find the minimal sum-of-products (SOP) form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states".
(iv) Draw the logic circuit of the counter.

Question 5: (15 points)

Design a synchronous sequential circuit with two T flip-flops *A* and *B*, one input *y* and one output *Z*. When $y = 0$, the state of the circuit remains the same and $Z = 0$. When $y = 1$, the circuit goes through the following state transitions from 00 to 01 to 11 to 10 and back to 00, then repeats, while $Z = y$ for states 10 and 11 and $Z = \overline{y}$ for states 00 and 01. Assume that state 00 is in the initial state.

(i) Provide a table that shows:
  (a) the input and output values
  (b) the states (present and next) for the two T flip-flops

(ii) Using Karnaugh-maps, find the minimal sum-of-products (SOP) form of the equations for the inputs to the T flip-flops and the output (*Z*).

(iii) Draw the resulting logic circuit.

If needed, use these pages and indicate the question number.