Université d'Ottawa · University of Ottawa

Faculté de Génie - Faculty of Engineering
ITI1100C Digital Systems I –Assignment 3

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Gate-Level Minimization

1) Simplify the following Boolean functions, using *Karnaugh* maps:

$(a)\ \boldsymbol{F}\ (\boldsymbol{x}, \boldsymbol{y}, \boldsymbol{z}) = \sum (2, 3, 6, 7)$

$(b)\ \boldsymbol{F}\ (\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}, \boldsymbol{D}) = \sum (4, 6, 7, 15)$

$(c)\ \boldsymbol{F}\ (\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}, \boldsymbol{D}) = \sum (3, 7, 11, 13, 14, 15)$

$(d)\ \boldsymbol{F}\ (\boldsymbol{w}, \boldsymbol{x}, \boldsymbol{y}, \boldsymbol{z}) = \sum (2, 3, 12, 13, 14, 15)$

2) Find the minterms of the following Boolean expressions by first plotting each function in a map:

$(a) xy + yz + xy'z$

$(b)\ C'D + ABC' + ABD' + A'B'D$

$(c) wyz + w'x' + wxz'$

$(d)\ A'B + A'CD + B'CD + BC'D'$

3) Simplify the following Boolean functions by first finding the essential prime implicants:

$(a)\ F(w, x, y, z) = \sum (0, 2, 5, 7, 8, 10, 12, 13, 14, 15)$

$(b)\ F(A, B, C, D) = \sum (0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$

$(c)\ F(A, B, C, D) = \sum (1, 3, 4, 5, 10, 11, 12, 13, 14, 15)$

$(d)\ F(w, x, y, z) = \sum (0, 1, 4, 5, 6, 7, 9, 11, 14, 15)$

4) Simplify the following expressions to (1) sum-of-products and (2) products-of-sums:

(a) $x'z' + y'z' + yz' + xy$

(b) $ACD' + C'D + AB' + ABCD$

$(c)\ (A' + B + D')\ (A' + B' + C')(A' + B' + C)(B' + C + D')$

$(d)\ BCD' + ABC' + ACD$

5) Simplify the following Boolean function F, together with the don't-care conditions d, and then express the simplified function in sum-of-minterms form:

$(a)\ F(x, y, z) = \sum (0, 1, 4, 5, 6)$ $\quad d(x, y, z) = \sum (2, 3, 7)$

$(b)\ F\ (A, B, C, D) = \sum (0, 6, 8, 13, 14)$ $\quad d(A, B, C, D) = \sum (2, 4, 10)$

(c) $F(A,B,C,D) = \sum(5,6,7,12,14,15)$ $d(A,B,C,D) = \sum(3,9,11)$

(d) $F(A,B,C,D) = \sum(4,12,7,2,10)$ $d(A,B,C,D) = \sum(0,6,8)$

6) Simplify the following functions, and implement them with two-level NAND gate circuits:

(a) $F(A,B,C,D) = AC'D' + A'C + ABC + AB'C + A'C'D'$

(b) $F(A,B,C,D) = A'B'C'D + CD + AC'D$

7) Draw a logic diagram using only two-input NOR gates to implement the following function:

$F(A,B,C,D) = (A \oplus B)'(C \oplus D)$

Combinational Logic

8) Consider the combinational circuit shown in the following figure:

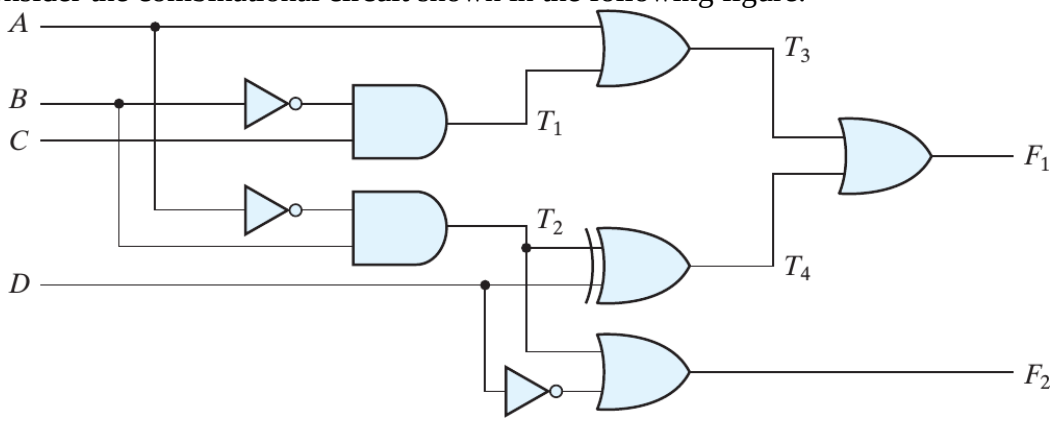


FIGURE P4.1

(a) Derive the Boolean expressions for $T1$ through $T4$. Evaluate the outputs $F1$ and $F2$ as a function of the four inputs.

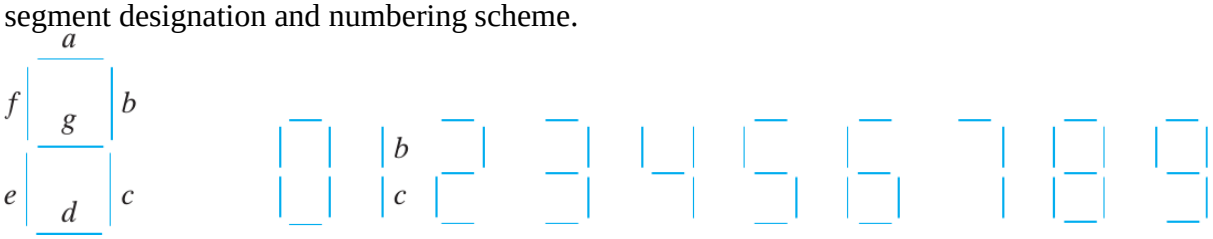
(b) List the truth table with 16 binary combinations of the four input variables. Then list the binary values for $T1$ through $T4$ and outputs $F1$ and $F2$ in the table.

(c) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).

9) Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

10) An BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in Fig. (a). The numeric display chosen

to represent the decimal digit is shown in Fig. (b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display. The following figure shows the segment designation and numbering scheme.



(a) Segment designation (b) Numerical designation for display

11) Draw the logic diagram of a 2-to-4-line decoder using (a) NOR gates only and (b) NAND gates only. Include an enable input.

12) A combinational circuit is specified by the following three Boolean functions:

$F1(A, B, C) = \boldsymbol{\Sigma}(1, 4, 6)$

$F2(A, B, C) = \boldsymbol{\Sigma}(3, 5)$

$F3(A, B, C) = \boldsymbol{\Sigma}(2, 4, 6, 7)$

Implement the circuit with a decoder constructed with NAND gates and NAND or AND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates.