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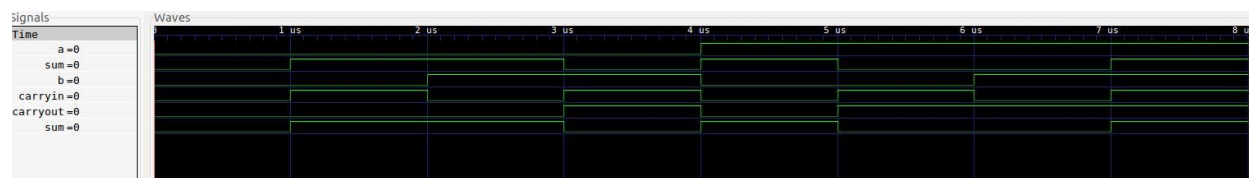
HW2: Verilog Building Blocks

Adder:

Below is the truth table with expected values for the full adder. In the expected values C is carryout and S is sum.

```
comparch@comparchVM:~/Documents/CompArch/HW2$ /home/comparch/Documents/CompArch/HW2/adders
VCD info: dumpfile adder.vcd opened for output.
Carryin A B | Carryout sum | Expected C Expected S
  0  0  0 |      0  0 | Expected 0 Expected 0
  1  0  0 |      0  1 | Expected 0 Expected 1
  0  0  1 |      0  1 | Expected 0 Expected 1
  1  0  1 |      1  0 | Expected 1 Expected 0
  0  1  0 |      0  1 | Expected 0 Expected 1
  1  1  0 |      1  0 | Expected 1 Expected 0
  0  1  1 |      1  0 | Expected 1 Expected 0
  1  1  1 |      1  1 | Expected 1 Expected 1
comparch@comparchVM:~/Documents/CompArch/HW2$
```

Below is the GTK simulation.

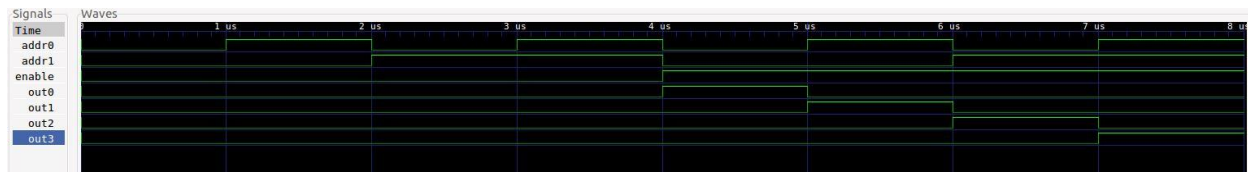


Decoder:

Below is the truth table and expected values for the 2-bit decoder. This decoder takes a 2 bit number and decodes it with 4 outputs.

```
comparch@comparchVM:~/Documents/CompArch/HW2$ /home/comparch/Documents/CompArch/HW2/decoders
VCD info: dumpfile decoder.vcd opened for output.
En A0 A1 | 00 01 02 03 | Expected Output
  0  0  0 |  0  0  0  0 | All false
  0  1  0 |  0  0  0  0 | All false
  0  0  1 |  0  0  0  0 | All false
  0  1  1 |  0  0  0  0 | All false
  1  0  0 |  1  0  0  0 | 00 Only
  1  1  0 |  0  1  0  0 | 01 Only
  1  0  1 |  0  0  1  0 | 02 Only
  1  1  1 |  0  0  0  1 | 03 Only
```

Below is the GTK simulation of the decoder.



Multiplexer:

Below is a truth table for a 4:1 multiplexer.

```
comparch@comparchVM:~/Documents/CompArch/HW2$ /home/comparch/Documents/CompArch/HW2/multiplexerS
VCD info: dumpfile multiplexer.vcd opened for output.
in0 in1 in2 in3 | add0 add1 | out | Expected Output
0 0 0 0 | 0 0 | 0 | False
1 0 0 0 | 0 0 | 1 | True
0 1 0 0 | 0 0 | 0 | False
0 0 1 0 | 0 0 | 0 | False
0 0 0 1 | 0 0 | 0 | False
1 0 0 0 | 1 0 | 0 | False
0 1 0 0 | 1 0 | 1 | True
0 0 1 0 | 1 0 | 0 | False
0 0 0 1 | 1 0 | 0 | False
1 0 0 0 | 0 1 | 0 | False
0 1 0 0 | 0 1 | 0 | False
0 0 1 0 | 0 1 | 1 | True
0 0 0 1 | 0 1 | 0 | False
1 0 0 0 | 1 1 | 0 | False
0 1 0 0 | 1 1 | 0 | False
0 0 1 0 | 1 1 | 0 | False
0 0 0 1 | 1 1 | 1 | True
comparch@comparchVM:~/Documents/CompArch/HW2$
```

Below is the GTK wave simulation for the 4:1 multiplexer.

