Samantha Young and Emma Westerhoff Work Plan

Lab 2 SPI

Input Conditioning: **DUE Tuesday 9th**

Verilog .v & Test bench:

1 hour Verilog

.5 hour Test Cases

- Input Synchronization - 1.5 hour
- Debouncing - 1.5 hour
- Edge Detection - 1.5 hour

Shift Register: **DUE Tuesday 9th**

Verolog .v: & Test Bench: 3 hours

- Testcases: 1 hour

Midpoint: **DUE Friday 12th**

- FPGA:
  - 2 hours

SPI Memory: **DUE SUNDAY 14th**

- Schematic - 1 hour
- Write/ Read Verilog - 2 hours
- Finite State Machine - 2 hours
- Verilog - 2 hours
- FPGA Testing Debugging -3 - **DUE Monday 15th**

Report: 3 hours -**DUE Wednesday 17th**