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CS3421 Comp Org

HW3

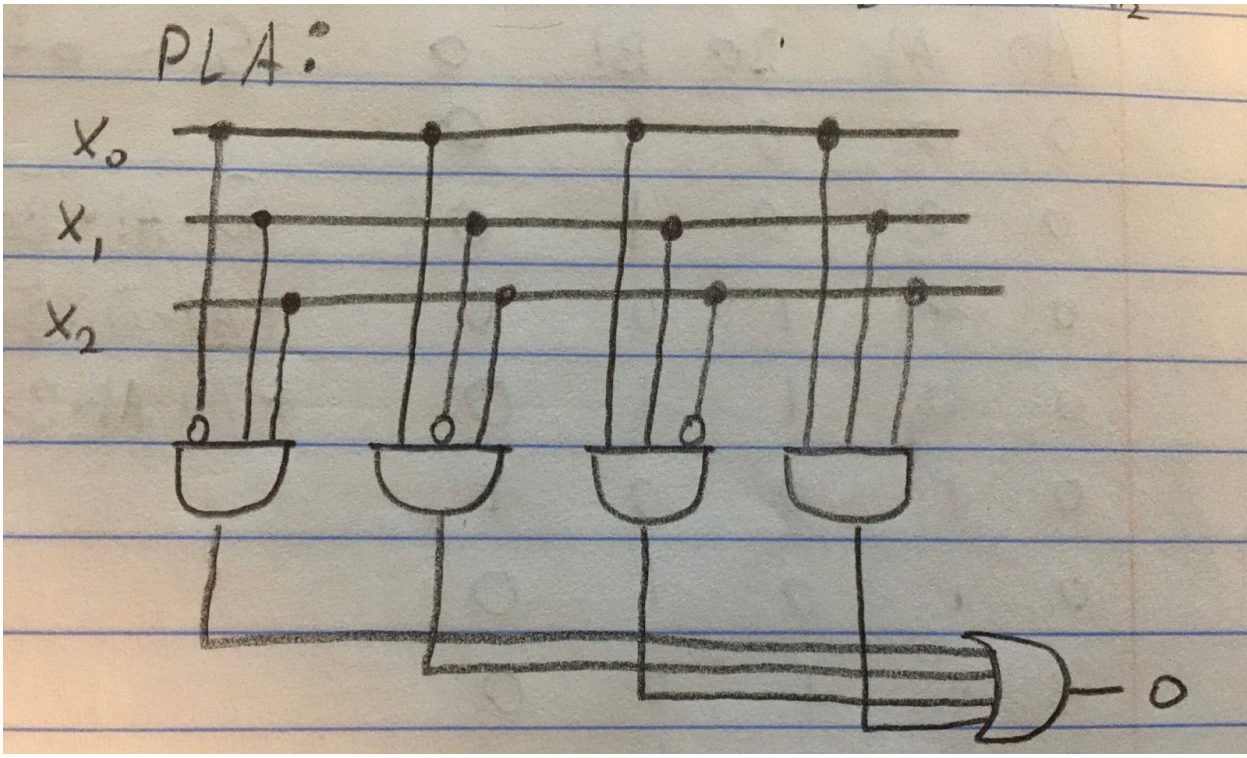
1. Design a circuit that takes three bits (X2, X1, X0) as input and produces one bit (O) as output. O is 1 if and only if the number of ones in X2, X1, and X0 is two or more.

a.

X0	X1	X2	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

b. $\overline{x_0} \cdot x_1 \cdot x_2 + x_0 \cdot \overline{x_1} \cdot x_2 + x_0 \cdot x_1 \cdot \overline{x_2} + x_0 \cdot x_1 \cdot x_2$

c.



2.

a. $((A \bullet \overline{B}) \bullet B \bullet (B + \overline{C})) \bullet D$

b.

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

c. Propagation delay: 65ns
Critical path is from B through NOT then AND then NOT then AND then OR gates

3. Design a comparator that takes four bits (A1, A0, B1, B0) as input and produces one bit (O) as output. O is 1 if and only if the binary value of A1A0 is less than the B1B0 when both pairs of bits are interpreted as 2-bit unsigned integers.

a.

A0	A1	B0	B1	O
0	0	0	0	0
0	0	0	1	0

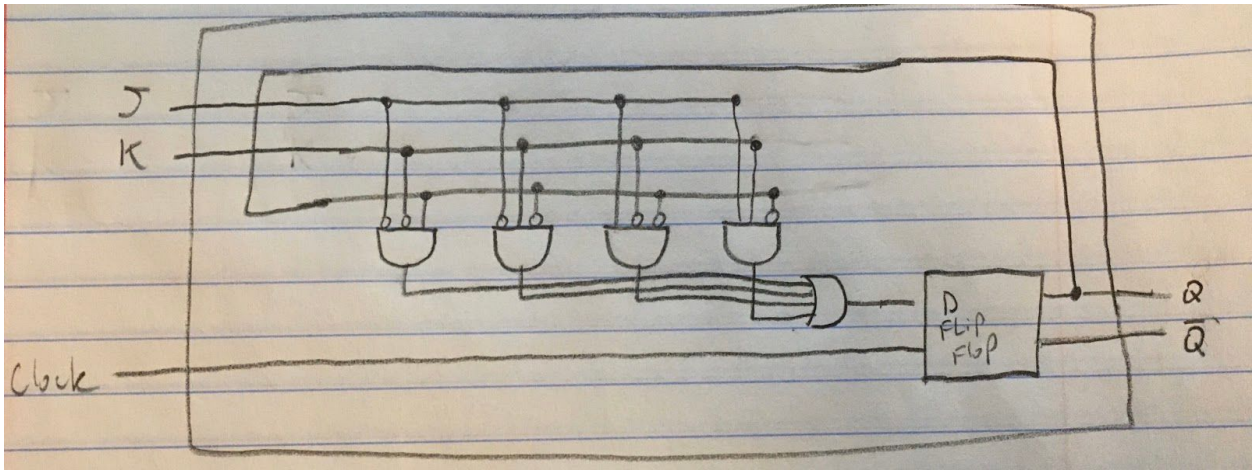
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

b.

c. $\overline{A0} \bullet A1 \bullet \overline{B0} \bullet \overline{B1} + A0 \bullet \overline{A1} \bullet B0 \bullet \overline{B1} \; + \; \overline{A0} \bullet A1 \bullet B0 \bullet \overline{B1} + A0 \bullet A1 \bullet \overline{B0} \bullet \overline{B1} \; + \; A0 \bullet A1 \bullet \overline{B0} \bullet B1 + A0 \bullet A1 \bullet \overline{B0}$

4. A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates its output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state. Construct a JK flip-flop using a D flip-flop and some additional combinational logic.

a.



b. $\overline{J} \bullet \overline{K} \bullet Q + \overline{J} \bullet K \bullet \overline{Q} + J \bullet \overline{K} \bullet \overline{Q} + J \bullet K \bullet \overline{Q}$
(Q is output from D Flip-FLop)

5.

a. Ainvert and Binvert should be 1, Operator should be 1
b. Ainvert and B invert can be 1 or 0 as long as they are both the same. Operator should be 2, CarryIn needs to be zero.