# IBEX based SoC - MILESTONE 3


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1. **PLAN:**

STEP 1: Hardening the IBEX core with a clean layout. **[Done ]**
STEP 2: Changing the configurations of IBEX core and reporting on the results. **[Done ]**
STEP 2: IBEX AHB-Lite bus interface and the testbenches used for verification. **[Done ]**
STEP 3: SoC simulation for N5 based SoC generated by SoCGen. **[Done ]**
STEP 4: Simulate wrapper which contains IBEX core module, interface module and AHB bus. **[Undergoing ]**

## Harden teps:

1) First the part responsible for clock gating in the "prim_clock_gating" module in IBEX RTLs needed to be replaced by hand by the module responsible for clock gating in Sky-130. This is need because the synthesizer cannot translate clock gating
    a. To make this working with the Openlane flow the "SYNTH_READ_BLACKBOX_LIB" configuration needs to be set to 1
2) Then after running the flow an error was reported in the routing phase indicating that the design is a " congested design"
    a. To solve this the area of the core needs to be increased. This is done by decreasing the core utilization to 30
3) After word we had a clean layout but with a high delay
    a. To overcome this SYNTH_STRATEGY configuration is set to 0, so the flow can aim for the minimum delay
4) After word we tried a different set of configurations to minimize the slack so we can use fast clock, to minimize the antenna violations and to make sure that any magic violations are false positives.

**Notes**:

- All the magic violations are false positives because they are minimum hole violations.
- Going below 3.5 for PL_TARGET_DENSITY configuration or setting SYNTH_STRATEGY to 1 result in segmentation violation
- Since, segmentation violation is not a descriptive error, so the error is hard to be figured out. Setting PL_TARGET_DENSITY to 3.5 and SYNTH_STRATEGY to 1 needs to be avoided
- The best combination of configuration is highlighted

## Configurations:

| density | utilization | strategy | Diode Insertion Strategy | magic violations | antenna violations | Timing | Errors |
|---|---|---|---|---|---|---|---|
| 0.4 | 30 | 0 | 3 | 17 | 60 | 9.72 data required time<br>_____<br>-20.33 data arrival time<br>_____<br>-10.62 slack | None |
| 0.3 | 50 | 0 | 3 | - | - | - | Error log:<br>during executing: "Psn /openLANE_flow/scripts/openPhySyn.tcl \|& tee >&@stdout/openLANE_flow/designs/ibex/runs/01-12_14-34/logs /placement/openphysyn.log"<br>Last 10 lines:<br>child killed: segmentation violation |
| 0.3 | 30 | 0 | 3 | | | | Error log:<br>during executing: "Psn /openLANE_flow/scripts/openPhySyn.tcl \|& tee >&@stdout /openLANE_flow/designs/ibex/runs/01-12_14-56/logs/ placement/openphysyn.log"<br>Last 10 lines:<br>child killed: segmentation violation |
| 0.35 | 30 | 0 | 3 | 13576 | 63 | 9.70 data required time<br>_____<br>-19.71 data arrival time<br>_____<br>-10.01 slack | None |

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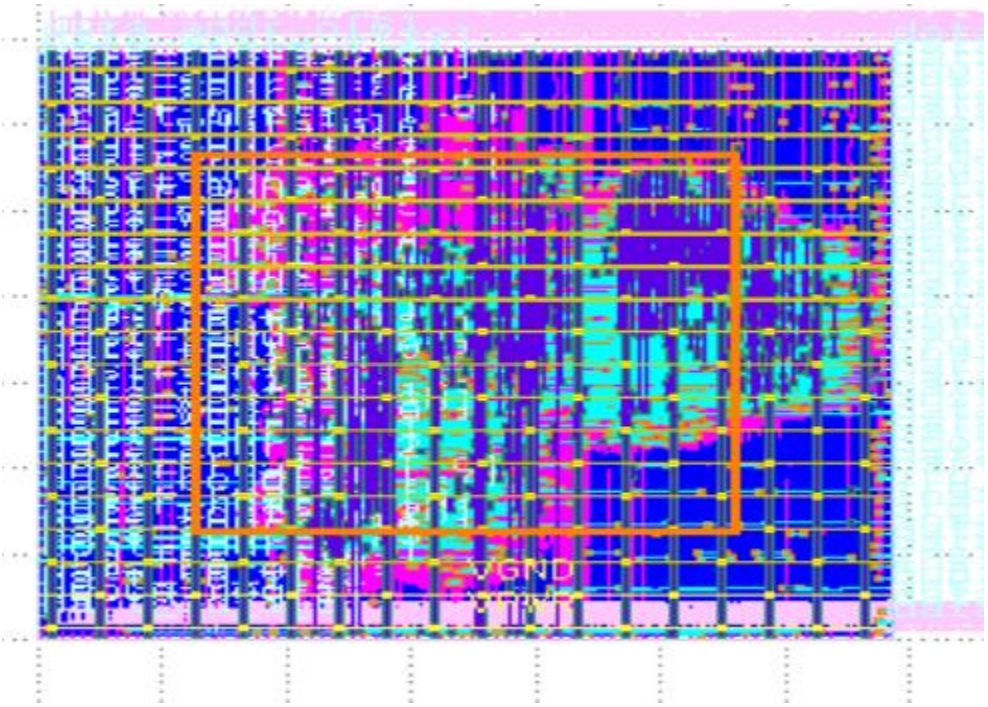
|---|---|---|---|---|---|---|---|
| 0.4 | 30 | 1 | 3 | -- | -- | -- | Error log:<br>during executing: "Psn /openLANE_flow/scripts/openPhySyn.tcl \|& tee >&@stdout / openLANE_flow/designs/ibex/runs/01-12_14-56/logs/ placement/openphysyn.log"<br>Last 10 lines:<br>child killed: segmentation violation |
| 0.35 | 25 | 0 | 3 | 19 | 57 | 9.70 data required time<br>_____<br>-19.71 data arrival time<br>_____<br>-10.01 slack | none |
| 0.4 | 25 | 0 | 3 | 19 | 67 | 9.68 data required time<br>_____<br>-19.77 data arrival time<br>_____<br>-10.09 slack | none |

Top modules layout:




The placement with 3.5 density: