EEE 3098S

Swicth Mode Power Supply -SMPS

July 22, 2023

1 Introduction

1.1 Scenario

Consider an industrial automation setup where a specific component, let's say a motor controller, requires a regulated supply voltage ranging between 5V and 9V to function optimally. However, the main power supply in the industrial facility provides a higher voltage level, such as 220 Vrms. To ensure that the motor controller receives the appropriate voltage within the specified range, a buck converter can be employed. In this scenario, a buck converter is integrated into the power distribution system of the industrial facility. It is connected to the main power supply and is responsible for stepping down the voltage to the desired range of 5V to 9V for the motor controller. Industrial automation systems often operate on a large scale, consuming significant amounts of electrical power. By improving the efficiency of the buck converter, less energy is wasted during the voltage conversion process. This translates to reduced overall energy consumption, leading to cost savings and environmental benefits. Monitoring the efficiency of the SMPS is of paramount importance.

1.2 Design Task

For the current year's assignment, your objective is to implement a Switched-Mode Power Supply (SMPS) for the conversion of a 220Vrms AC mains voltage to a 5V, 0-1A DC output. You are supposed to incorporate the ability of the converter to switch between 5V and 9V outputs. However, it is important to note that the minimum requirement is the 5V system. The successful completion of this project hinges upon your ability to design the electronic topology, ensuring the selection of appropriate component values and the preferred structure. Additionally, you will be responsible for developing the necessary software that controls the power supply and monitors the efficiency of the SMP using the UCT STM32 board. To provide a clear starting point and endpoint for this project, the block diagram depicted below illustrates the idealized configuration of the SMPS. It should be noted that this diagram does not represent the final representation of the device. In Figure 1 above, we present a schematic representation of a voltage source converter (VSC). The primary focus of this

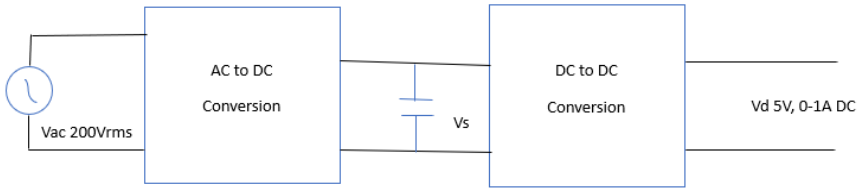

Figure 1: SMPS implemented with a voltage source converter

project revolves around the implementation of the DC-to-DC conversion block. Familiarity with the SMPS concept is expected, as it has been covered in previous electronics courses, thereby providing you with a sound understanding of its operation. Envisioning the SMPS as a block diagram, the final design representation for this project involves the SMPS delivering power to a load with feedback mechanisms incorporated to ensure optimal load management and monitoring the efficiency of the SMPS.

2 Switch Mode Power Supply

The most straightforward DC to DC converter that can be utilized is known as the Buck converter. To explain the operation of this device, a constant voltage source labelled Vs is employed. Our goal is to design this specific type of converter. Other converter configurations demand extensive planning and calculations during the physical implementation stage. The diagram below provides a visual representation of the Buck converter. The circuit operates by switching

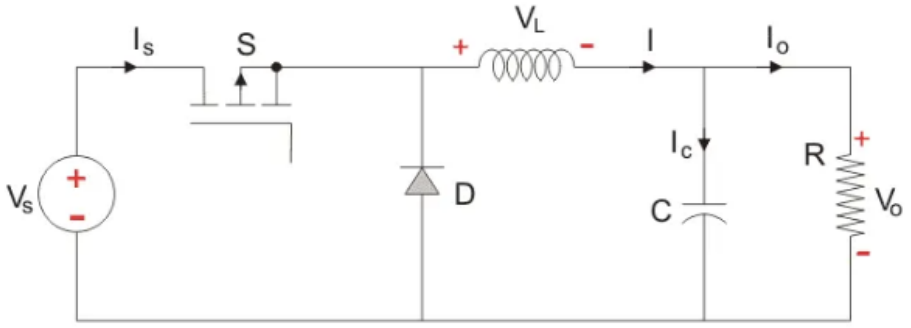

Figure 2: SMPS implemented with a voltage source converter

the power MOSFET on and off at a high frequency. When the MOSFET is turned on, it allows current to flow from the input source through an inductor and into the load. During this time, energy is stored in the inductor's magnetic field. When the MOSFET is turned off, the magnetic field collapses, and the energy is transferred to the load through the diode. The diode acts as a one-way valve, allowing current to flow only in the direction from the inductor to the load. This transfer of energy to the load results in a lower output voltage. By controlling the duty cycle of the MOSFET (the ratio of time it is on versus off), the average output voltage can be adjusted. The buck converter circuit efficiently converts higher input voltages to lower output voltages by minimizing power losses and maintaining high efficiency. **Remember the other goal of this design besides building an SMPS is also to analyse the efficiency of the buck converter.** The PWM that is switching the Power MOSFET can be turned on/off by using frequency-based modulation or time-based modulation. Time-based Modulation is mostly used for DC-DC converters. It is simple to construct and use. The frequency remains constant in this type of PWM modulation. Frequency-based modulation has disadvantages like a wide range of frequencies to achieve the desired control of the switch which in turn will give the desired output voltage. This leads to a complicated design for the low-pass LC filter which would be required to handle a large range of frequencies.

2.1 Mode 1: Switch ON/Diode OFF

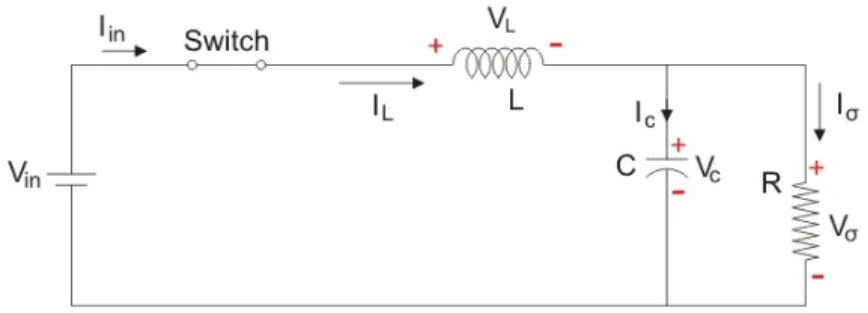

Figure 3: Buck Converter Mode 1 of Operation

The voltage across the capacitance in a steady state is equal to the output voltage. Let us say the switch is on for a time Ton and is off for a time Toff. We define the time period, T, as

$$T = T_{on} + T_{off}$$

and the switching frequency is given by

$$f_{swicthing} = \frac{1}{T}$$

The duty cycle is defined as

$$D = \frac{T_{on}}{T}$$

Using the KVL we will get the following equations.

$$V_{in} = V_L + V_o$$

$$V_L = L\frac{di_L}{dt}$$

$$\frac{di_L}{dt} = \frac{di_L}{Dt} = \frac{V_{in} - V_o}{L}$$

Since the switch is closed for a time Ton = DT, Δt = DT.

$$(\Delta i_L)_{closed} = (\frac{V_{in} - V_o}{L})DT$$

While performing the analysis of the Buck converter, we have to keep in mind that

1. The inductor current is continuous and, this is made possible by selecting an appropriate value of L
2. The inductor current in a steady state rises from a value with a positive slope to a maximum value during the ON state and then drops back down to the initial value with a negative slope. Therefore the net change of the inductor current over any complete cycle is zero.

2.2 Mode 2: Switch is OFF and Diode is ON

Here, the energy stored in the inductor is released and is ultimately dissipated in the load resistance, and this helps to maintain the flow of current through the load. But for analysis, we keep the original conventions to analyse the circuit using KVL. Let us now analyse the Buckconverterin steady state operation for Mode II using KVL.

$$0 = V_L + V_o$$

$$V_L = L\frac{di_L}{dt} = -V_o$$

$$\frac{di_L}{dt} = \frac{di_L}{(1-D)T} = \frac{-V_o}{L}$$

Since the switch is open for a time

$$T_{OFF} = T - T_{ON} = T - DT = (1-D)T$$

we know that Δt =(1-DT)

$$(\Delta i_L)_{open} = -(\frac{V_o}{L})(1-D)T$$

It is already established that the net change of the inductor current over any complete cycle is zero.

$$(\Delta i_L)_{closed} + (\Delta i_L)_{open} = 0$$

$$\frac{V_o}{V_{in}} = D$$

$$\frac{V_in - V_o}{L} DT + \frac{-V_o}{L}(1-D)T = 0$$

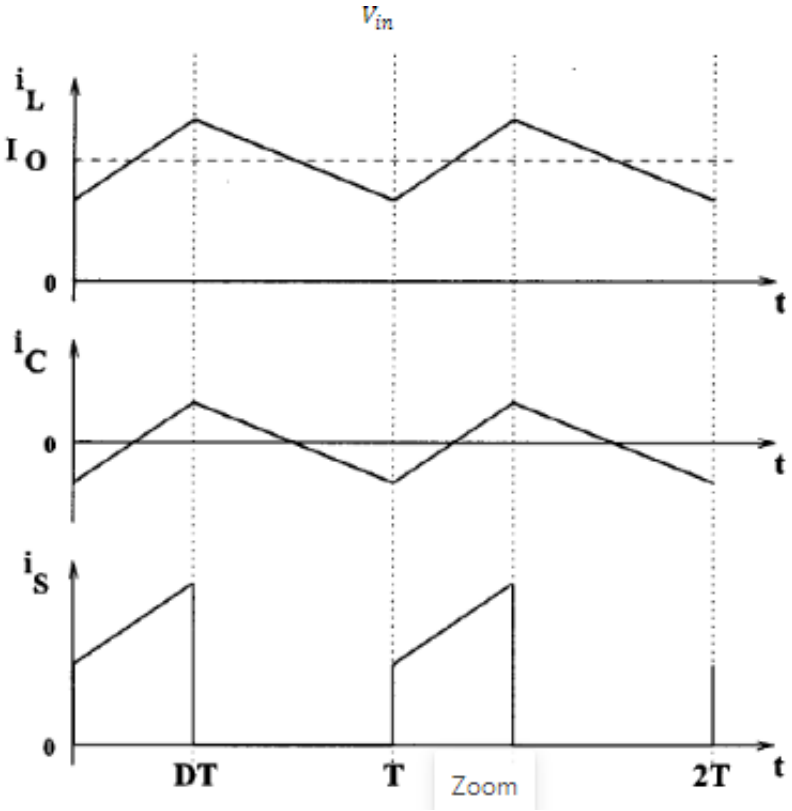

Figure 4: Buck Converter Mode 2 Operation

3 Mictrocontroller - UCT STM 32F051C6T6

You will be running your embedded software UCT STM32 board, the one you used in your second year. Here is the link for you to get started and refresh your STM32 knowledge-STM32F051C6T6 link

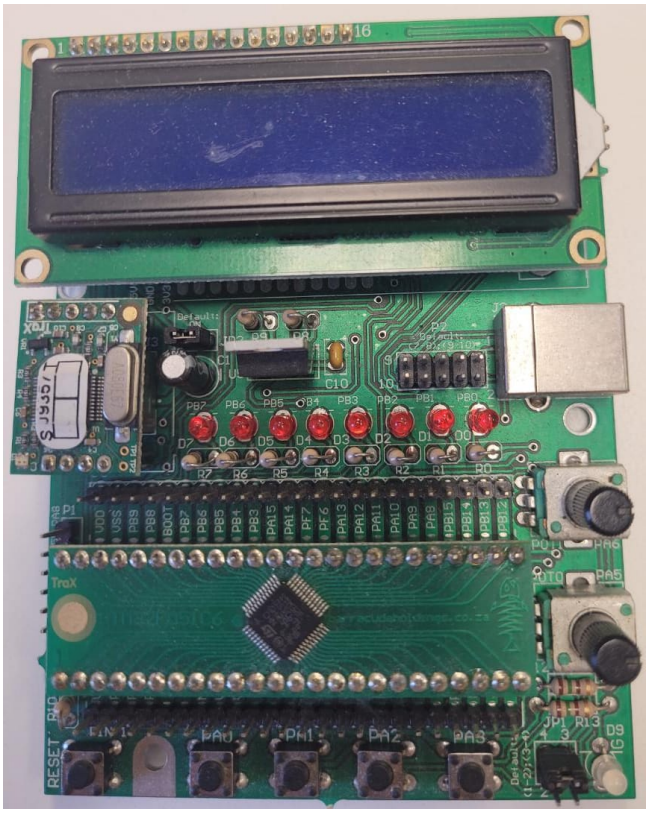

Figure 5: UCT STM32F051C6T6

4 Measuring the efficiency of the SMPS

For measuring the efficiency of the SMPS you will be using an i2c digital wattmeter shown in the image below.

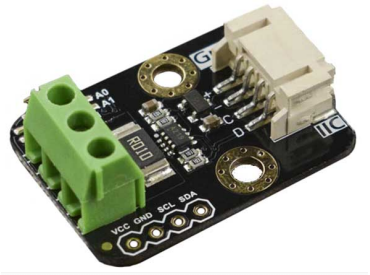

Figure 6: GRAVITY: I2C DIGITAL WATTMETER

5 Marks

The calculation for the final marks for EEE3098S will be as follows:

1. Project Milestone 1: Paper Design, Project plan, Circuit Design, Simulink Onramp, Simscape onramp, Matlab Onramp -**25%**.
2. Project Milestone 2: Progress Report 1 - **25%**
3. Project Milestone 3: Progress Report 3 - **25%**
4. Project Milestone 4: Final Report - **25%**

6 Key Dates

Milestone	**Deadline**
Milestone 1: Paper Design, Project plan, Circuit Design, Onramp course	14 August
Project Milestone 2: Progress Report 1	14 September
Project Milestone 2: Progress Report 2	13 October
Project Milestone 4: Final Report	20 October

7 Penalties

1. Each day of late submission translates to a penalty of 5% (max five days).
2. 10% will be deducted if a report includes any hand-drawn diagram or diagram that is not visible if printed.