

# VDF Project Part 2

Group 7:

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## **Project Goal:**

The goal of the project is to acquire practical knowledge of VLSI design flow. The main goal of this project is State-of-the-art CAD tools used for physical design and understanding of various things Trade-offs associated with physical design. We need to analyze and record timing reports results.

## **Project Part-1:**

Detailed design specifications were proposed in Part-1 of the project. The Verilog HDL code is written to meet all specifications. The test bench is created to run the simulation and the simulation tool used is Nclaunch. Three different test benches were created to check code coverage. We investigated and analyzed the impact of various test patterns on code coverage. In the next part of the project, we had to perform the next steps of the VLSI design flow. These steps included logic synthesis, formal equivalence checking, static timing analysis, and design for testability. The DFT step included the insertion of a scan chain. Each step included a detailed analysis of the results obtained through CAD tools

Our design consists of

- **Frequency Divider by 6**
- **Four bit Comparator**
- **Bitwise XOR**
- **Addition block**

## **Project Part-2:**

In this part of the project, the design goes through the physical design flow. The physical design includes floorplanning, placement, clock tree synthesis and detailed routing. Physical design is the process of transforming the netlist into the final layout. We have used the netlist which was generated after scan insertion in Project Part-1 for the physical design.

# Interpretations of results obtained in various steps of Physical Design

**Worst Path:** As we progress in the design flow our worst path incase of both setup and hold keep on varying. This is because as we keep on adding more stuff to our design, we move closer towards the reality and then delays of different paths will change depending upon the placement of other signals which control them.

**Post Placement:** Post placement *setup slack* reduced as now we are physically placing cells in the core area and depending on how close they are, the delays would be defined. We move closer towards a more realistic result of slack value. We observe that area increases very slightly post placement as compared to the post scan insertion stage. In the layout using the INNOVUS tool, we observe that a design is initialized and all the pins are visible on the design. As we move further our whole layout is initialized and all the layers and instances or standard cells are visible. The tool was successfully able to minimize/optimize for power after placement in comparison to the post scan insertion stage.

**Post CTS:** For most of the time the '*Hold Slack*' was negative. However, after CTS the hold slack became positive. This is because post CTS, we have buffers introduced in the datapath of our system. This results in our data coming slowly and hence we no longer have hold violations. However, post CTS because of these buffers, the setup slack reduced. We observe that area increases significantly after we have performed the clock tree synthesis as compared to that in the post placement stage which is essentially due to the addition of buffers and delay cells which have been added to fix or prevent timing violations. Area of each standard cell remains the same however which means the basic structure is not changed in this step. The number of buffers added is less when core utilization is increased due to tighter area constraints. In the layout we observe that a clock tree is generated which gets connected to the clock pin and we have shown the related screenshot in this report. CTS consists of two steps, synthesis of the clock tree and then the optimization of the clock tree which handles and balances the skew. After the Clock Tree Synthesis was done, additional buffers were added, due to which power consumption increased.

# Interpretations of Routability on the change in Floor Plan

Routability is majorly affected by the core utilization factor. Routability also introduces parasitics of the design which further affect timing and power of the system.

## **Timing**

Post routability our slack has further increased for setup. This is because as we use higher metal layers, we need more vias. Vias have a significant resistance and hence they cause more delays in the system.

## **Area**

Post routability we observe that increase in area is very less or in high utilization area does not increase at all. In some cases the tool can remove some buffers as well if the timing slack is much more positive in order to optimize the area. However, for the large core utilization part, no change in area is observed due to very strict rules and tight area constraint.

## **Power**

We have noticed that due to the usage of Metal 1 and Metal 2 for routing, due to which the power consumption has increased for the various core utilizations as we need our design to be more dense, the amount of Metal 1 & Metal 2 being varied the increase in power consumption.

## **Layout**

We observe that there is a huge difference in the layout for different core utilizations post routing. The design with large core utilization results in a much denser layout with close packed interconnects and instances which results in more parasitics and which shows less empty space is available in the design for routing and that over the cell routing has to be used in order to meet the design requirements.

# Before Physical Design

## Test Insertion

**Aim:** To analyse the new netlist generated after DFT insertion in terms of Area, power and TIming.

**Tool:** Cadence Genus

### TCL Script

```
set attr lib_search_path ..//lib/90/lib
set_attr hdl_search_path ..//rtl/testbench1
set_attr library slow_wlm.lib

read_hdl top.v

elaborate
read_sdc ..//constraints/constraints_project_3c.sdc
report timing -lint
set_attribute dft_scan_style muxed_scan
define_dft shift_enable -active high -create_port scan_en
define_dft test_mode -active high -create_port test_mode
define_dft test_clock clk
report dft_setup
check dft_rules >dft_report/dft_rules_report
fix dft_violations -test_control test_mode -async_set -async_reset -clock
synthesize -to_mapped
set_attr dft_min_number_of_scan_chains 2 rtl_module
set_attr dft_mix_clock_edges_in_scan_chains true rtl_module
#replace_scan
connect_scan_chains -auto_create_chains -preview
connect_scan_chains -auto_create_chains
report qor
write_atpg -cadence > rtl_module.atpg

write_atpg -stil > rtl_module_still.atpg
write_scandef dft_report/rtl_module.def
write_sdf -timescale ns -nonegchecks -recrm split -edges check_edge > dft_report/syn_report/delays.sdf
write_hdl > dft_report/synthesised_netlist.v
write_sdc > dft_report/sdc_file_for_physical_design.sdc
write_script > dft_report/synthesis_script_sdc.g
report timing > dft_report/synthesis_timing_report.rep
report power > dft_report/synthesis_power_report.rep
report gates > dft_report/synthesis_cell_report.rep
report area > dft_report/synthesis_area_report.rep
```

### WIRE DELAY MODEL

```
/* wire-loads Custom Made */
/* wire-loads */
wire_load("wlm") {
    resistance : 8.5e-8;
    capacitance : 1.5e-4;
    area : 0.7;
    slope : 1.5;
    fanout_length (1, 0.003);
    fanout_length (2, 0.006);
    fanout_length (3, 0.009);
    fanout_length (4, 0.012);
    fanout_length (5, 0.015);
    fanout_capacitance (1,0.002);
    fanout_capacitance (2,0.004);
    fanout_capacitance (3,0.006);
    fanout_capacitance (4,0.008);
    fanout_capacitance (5,0.010);
    fanout_resistance (1,0.02);
    fanout_resistance (2,0.025);
    fanout_resistance (3,0.03);
    fanout_resistance (4,0.035);
    fanout_resistance (5,0.04);
}
```

## Power Report

Instance: /rtl\_module

Power Unit: W

PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	6.03202e-06	2.29126e-04	6.52775e-06	2.41686e-04	74.02%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	3.13918e-06	4.92062e-05	1.77386e-05	7.00840e-05	21.46%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	1.47420e-05	1.47420e-05	4.51%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	9.17120e-06	2.78332e-04	3.90084e-05	3.26512e-04	99.99%
Percentage	2.81%	85.24%	11.95%	100.00%	100.00%

## Power increases (Reason at the end)

## Area Report

Generated by: Genus(TM) Synthesis Solution 19.13-s073\_1  
Generated on: Apr 07 2022 11:27:35 pm  
Module: rtl\_module  
Technology library: slow  
Operating conditions: slow (balanced\_tree)  
Wireload mode: enclosed  
Area mode: timing library

---

Instance	Module	Cell Count	Cell Area	Net Area	Total Area	Wireload
rtl_module		201	1617.495	0.000	1617.495	<none> (D)
in1	clk_divider_div_value3	8	82.502	0.000	82.502	<none> (D)

(D) = wireload is default in technology library

## Area Increases (reason at the end)

## Cell Report

```
=====  
Generated by:          Genus(TM) Synthesis Solution 19.13-s073_1  
Generated on:         Apr 07 2022 11:27:35 pm  
Module:               rtl_module  
Technology library:   slow  
Operating conditions: slow (balanced_tree)  
Wireload mode:        enclosed  
Area mode:            timing library  
=====
```

Gate	Instances	Area	Library
AND2X1	1	4.541	slow
AND2XL	24	108.994	slow
AOI211X1	1	5.298	slow
AOI21X1	7	31.790	slow
AOI21XL	6	27.248	slow
AOI22X1	3	18.166	slow
AOI32X1	1	6.812	slow
CLKINVX1	4	9.083	slow
INVX1	6	13.624	slow
INVXL	1	2.271	slow
MXI2XL	3	18.166	slow
NAND2BX1	10	45.414	slow
NAND2XL	11	33.304	slow
NAND3X1	1	4.541	slow
NAND4XL	4	21.193	slow
NOR2BX1	8	36.331	slow
NOR2XL	28	84.773	slow
NOR3X1	1	4.541	slow
OAI211X1	3	15.895	slow
OAI21X1	11	49.955	slow
OAI21XL	1	4.541	slow
OAI222XL	1	8.326	slow
OAI22X1	3	18.166	slow
OAI22XL	7	42.386	slow
OAI2BB1X1	2	10.597	slow
OR2XL	3	13.624	slow
SDFFQX1	36	735.707	slow
SDFFQXL	1	20.436	slow
SDFFTRX1	6	163.490	slow
XNOR2X1	3	24.978	slow
XNOR2XL	3	24.978	slow

```
total           201  1617.495
```

Type	Instances	Area	Area %
sequential	43	919.633	56.9
inverter	11	24.978	1.5
logic	147	672.884	41.6
physical_cells	0	0.000	0.0
total	201	1617.495	100.0

## STA AFTER DFT INSERTION

### Theory

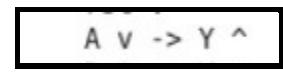
**Static Timing Analysis** is the design step in which we check for timing violations across different paths (especially the worst path) in our circuit design. STA gives the bounds of delay essential to meet timing constraints and for our circuit to function as we intend. The delays might change in the later phases of design. However, we must ensure that whatever we have designed so far is well between the safe window.

**Setup Analysis:** The data on the input pin of the capture flip flop must arrive ‘Setup Time’ before the next clock edge arrives on the flip flop.

**Hold Analysis:** A new data must not arrive on the input pin of the capture flip flop for ‘Hold Time’ after the clock edge has arrived on the flip flop.

The slack in both cases must be positive to ensure that no timing violation has occurred in the design. In general, Setup violations can be removed by making the design slower (i.e. increasing the clock period). However, hold violations are much harder or even impossible to remove. You must redesign the system to correct hold violations.

Arc:

  $A \downarrow \rightarrow Y \uparrow$   $\Rightarrow A$  has the falling edge, which leads to  $Y$  having a rising edge.

**Graph-Based Analysis vs Path-based Analysis:**

GBA	PBA
Loose Bound	Tight Bound
Computationaly Less Expensive	Computationaly More Expensive
Considers a more pessimistic view	Gives the real violation condition
Considers the max delay at every node	Considers the real delay at every node

## Slew || Load || Delay -Report per Cell

Generated by:	Genus(TM) Synthesis Solution 19.13-s073_1				
Generated on:	Apr 07 2022 11:27:35 pm				
Module:	rtl_module				
Technology library:	slow				
Operating conditions:	slow (balanced_tree)				
Wireload mode:	enclosed				
Area mode:	timing library				
Pin	Type	Fanout	Load	Slew	Delay Arrival
		(fF)	(ps)	(ps)	(ps)
(clock clk)	launch				0 R
(constraints_project_line_7)	latency		+500	500	R
rst	ext delay		+1200	1700	F
g538/A	in port	2	4.4	1200	+0
g538/Y				+0	1700
g2617/D				+0	2451
g2617/Y	CLKINVX1	32	57.2	632	+751
g2610/B1				+0	2451
g2610/Y	NAND4XL	11	18.2	933	+760
out_reg[2]/D	OAI222XL	1	1.8	386	+328
out_reg[2]/CK	<<< SDFQX1			+0	3538
	setup		500	+260	3798 R
(clock clk)	capture				4000 R
	latency		+500	4500	R
	uncertainty		-500	4000	R
Cost Group : 'clk' (path_group 'clk')					
Timing slack : 202ps					
Start-point : rst					
End-point : out reg[2]/D					

**Slew:** It is the transition time taken, i.e. the time taken for a signal to rise or fall. A lower value of slew would ensure better performance of the system. The delay of any cell is proportional to the Slew of the signal at its input.

**Rise Time:** Time taken for the signal to transition from 20% to 80% of its value.

**Fall Time :** Time taken for the signal to transition from 80% to 20% of its value.

Both Rise and Fall Times are dependent on the Load.

**Load:** As the load on the output of a cell increases, this leads to an increase in the slew of the cell, which causes an increase in the delay caused by that cell, thus increasing the arrival time of the signal on the next cell.

**Unate-ness:** How the output changes wrt to the transition in the input. Unate-ness can be positive (same transitions in the input and the output) or negative (opposite transition in the output to that of the input).  $A^+ -- B^+$  is positive unate-ness.  $A^- -- B^+$  is negative unate-ness.

Unate-ness is decided by seeing the timing arcs and then delay is calculated as per the unate-ness. Depending on whether the unateness is positive or negative, the delay of the cell would be calculated accordingly and hence varies.

The delay initially of the cell is present in the SDF (Standard Delay Format), but later the net delay is calculated while considering the unate-ness too.

# Analysis Coverage Report

```
1 #####
2 # Generated by: Cadence Tempus 20.10-p003_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Fri Apr 29 19:53:49 2022
5 # Design: rtl_module
6 # Command: report_analysis_coverage > $report_dir/analysis_coverage.rpt
7 #####
8 -----
9          TIMING CHECK COVERAGE SUMMARY
10 -----
11     Check Type          No. of   Met           Violated      Untested
12                  Checks
13 -----
14     ExternalDelay (Early)    11      11 (100%)    0 (0%)       0 (0%)
15     ExternalDelay (Late)     11      11 (100%)    0 (0%)       0 (0%)
16     Hold                   135      46 (34%)     89 (65%)      0 (0%)
17     PulseWidth              86      86 (100%)    0 (0%)       0 (0%)
18     Setup                   135     135 (100%)   0 (0%)       0 (0%)
19 -----
```

# All Violations Report

```
1 #####
2 # Generated by: Cadence Tempus 20.10-p003_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Fri Apr 29 19:53:49 2022
5 # Design: rtl_module
6 # Command: report_constraints -all_violators > sta_after_dft/reports/allviolations.rpt
7 #####
8 # format : frame 0 : split 1
9
10 max_delay/setup
11 -----
12 No paths found
```

```
14 min_delay/hold
15 -----
16
17     End Point          Slack      Cause
18 -----
19     B_reg_reg[2]/SE f   -1.148    VIOLATED
20     B_reg_reg[0]/SE f   -1.148    VIOLATED
21     A_reg_reg[8]/SE f   -1.148    VIOLATED
22     A_reg_reg[6]/SE f   -1.148    VIOLATED
23     A_reg_reg[4]/SE f   -1.148    VIOLATED
24     A_reg_reg[1]/SE f   -1.148    VIOLATED
25     out_reg[10]/SE f   -1.055    VIOLATED
26     out_reg[9]/SE f    -1.055    VIOLATED
27     out_reg[8]/SE f    -1.055    VIOLATED
28     out_reg[7]/SE f    -1.055    VIOLATED
29     out_reg[6]/SE f    -1.055    VIOLATED
30     out_reg[5]/SE f    -1.055    VIOLATED
31     out_reg[4]/SE f    -1.055    VIOLATED
32     out_reg[3]/SE f    -1.055    VIOLATED
33     out_reg[2]/SE f    -1.055    VIOLATED
34     out_reg[1]/SE f    -1.055    VIOLATED
35     out_reg[0]/SE f    -1.055    VIOLATED
36     C_reg_reg[8]/SE f   -1.055    VIOLATED
37     C_reg_reg[7]/SE f   -1.055    VIOLATED
38     C_reg_reg[6]/SE f   -1.055    VIOLATED
39     C_reg_reg[5]/SE f   -1.055    VIOLATED
40     C_reg_reg[4]/SE f   -1.055    VIOLATED
41     C_reg_reg[3]/SE f   -1.055    VIOLATED
42     C_reg_reg[2]/SE f   -1.055    VIOLATED
43     C_reg_reg[1]/SE f   -1.055    VIOLATED
44     C_reg_reg[0]/SE f   -1.055    VIOLATED
45     B_reg_reg[9]/SI f   -1.055    VIOLATED
```

46	B_reg_reg[9]/SE f	-1.055	VIOLATED
47	B_reg_reg[8]/SE f	-1.055	VIOLATED
48	B_reg_reg[7]/SE f	-1.055	VIOLATED
49	B_reg_reg[6]/SE f	-1.055	VIOLATED
50	B_reg_reg[5]/SE f	-1.055	VIOLATED
51	B_reg_reg[4]/SE f	-1.055	VIOLATED
52	B_reg_reg[3]/SE f	-1.055	VIOLATED
53	B_reg_reg[1]/SE f	-1.055	VIOLATED
54	A_reg_reg[9]/SE f	-1.055	VIOLATED
55	A_reg_reg[7]/SE f	-1.055	VIOLATED
56	A_reg_reg[5]/SE f	-1.055	VIOLATED
57	A_reg_reg[3]/SE f	-1.055	VIOLATED
58	A_reg_reg[2]/SE f	-1.055	VIOLATED
59	A_reg_reg[0]/SE f	-1.055	VIOLATED
60	in1/count_reg_reg[0]/SE f	-1.055	VIOLATED
61	in1/count_reg_reg[1]/SE f	-1.055	VIOLATED
62	in1/clk_out_reg/SI f	-1.055	VIOLATED
63	in1/clk_out_reg/SE f	-1.055	VIOLATED
64	out_reg[10]/SI f	-0.203	VIOLATED
65	out_reg[9]/SI f	-0.203	VIOLATED
66	out_reg[8]/SI f	-0.203	VIOLATED
67	out_reg[7]/SI f	-0.203	VIOLATED
68	out_reg[6]/SI f	-0.203	VIOLATED
69	out_reg[5]/SI f	-0.203	VIOLATED
70	out_reg[4]/SI f	-0.203	VIOLATED
71	out_reg[3]/SI f	-0.203	VIOLATED
72	out_reg[2]/SI f	-0.203	VIOLATED
73	out_reg[1]/SI f	-0.203	VIOLATED
74	B_reg_reg[3]/SI f	-0.190	VIOLATED
75	B_reg_reg[1]/SI f	-0.190	VIOLATED
76	A_reg_reg[9]/SI f	-0.190	VIOLATED
77	A_reg_reg[7]/SI f	-0.190	VIOLATED

78	A_reg_reg[5]/SI f	-0.190	VIOLATED
79	A_reg_reg[2]/SI f	-0.190	VIOLATED
80	A_reg_reg[0]/SI f	-0.169	VIOLATED
81	in1/count_reg_reg[0]/SI f	-0.163	VIOLATED
82	C_reg_reg[2]/SI f	-0.158	VIOLATED
83	in1/count_reg_reg[0]/D f	-0.158	VIOLATED
84	C_reg_reg[1]/SI f	-0.157	VIOLATED
85	C_reg_reg[6]/SI f	-0.144	VIOLATED
86	B_reg_reg[5]/SI f	-0.142	VIOLATED
87	C_reg_reg[8]/SI f	-0.141	VIOLATED
88	B_reg_reg[0]/SI f	-0.134	VIOLATED
89	C_reg_reg[3]/SI f	-0.131	VIOLATED
90	in1/count_reg_reg[1]/SI f	-0.131	VIOLATED
91	C_reg_reg[0]/SI f	-0.121	VIOLATED
92	out_reg[0]/SI f	-0.117	VIOLATED
93	A_reg_reg[8]/SI f	-0.114	VIOLATED
94	A_reg_reg[6]/SI f	-0.114	VIOLATED
95	B_reg_reg[4]/SI f	-0.113	VIOLATED
96	A_reg_reg[3]/SI f	-0.111	VIOLATED
97	C_reg_reg[5]/SI f	-0.106	VIOLATED
98	C_reg_reg[7]/SI f	-0.103	VIOLATED
99	C_reg_reg[4]/SI f	-0.103	VIOLATED
100	B_reg_reg[8]/SI f	-0.103	VIOLATED
101	B_reg_reg[6]/SI f	-0.103	VIOLATED
102	B_reg_reg[7]/SI f	-0.103	VIOLATED
103	in1/count_reg_reg[1]/D f	-0.102	VIOLATED
104	A_reg_reg[1]/SI f	-0.101	VIOLATED
105	A_reg_reg[4]/SI f	-0.093	VIOLATED
106	B_reg_reg[2]/SI f	-0.086	VIOLATED
107	in1/clk_out_reg/D f	-0.026	VIOLATED
108			

```

109 check_type : clock_period
110 -----
112 No paths found
113
114 Check type : skew
115 -----
116 No paths found
117
118 Check type : pulse_width
119 -----
120 No violating Checks with given description found
121
122 Check type : max_transition
123 -----
124 No Violations found
125
126 Check type : min_transition
127 -----
128 No Violations found
129
130 Check type : max_capacitance
131 -----
132 No Violations found
133
134 Check type : min_capacitance
135 -----
136 No Violations found
137
138 Check type : max_fanout
139 -----
140 No Violations found
141
142 Check type : min_fanout
143 -----

```

## Timing Report

```
1 #####
2 # Generated by: Cadence Tempus 20.10-p003_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Fri Apr 29 19:53:49 2022
5 # Design: rtl_module
6 # Command: report_timing > $report_dir/timing_report.rpt
7 #####
8 Path 1: MET Setup Check with Pin out_reg[2]/CK
9 Endpoint: out_reg[2]/D (^) checked with leading edge of 'clk'
10 Beginpoint: rst (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Other End Arrival Time 0.500
13 - Setup 0.262
14 + Phase Shift 4.000
15 - Uncertainty 0.500
16 = Required Time 3.738
17 - Arrival Time 3.680
18 = Slack Time 0.058
19     Clock Rise Edge 0.000
20     + Input Delay 1.200
21     + Network Insertion Delay 0.500
22     = Beginpoint Arrival Time 1.700
23 -----
24     Instance Arc Cell Delay Arrival Required
25                 Time Time
26 -----
27     -      rst v   -    -  1.700  1.758
28     g538   A v -> Y ^ CLKINVX1 0.819  2.519  2.576
29     g2617   D ^ -> Y v NAND4XL 0.817  3.336  3.393
30     g2610   B1 v -> Y ^ OAI222XL 0.344  3.680  3.738
31     out_reg[2] D ^ SDFFQX1 0.000  3.680  3.738
32 -----
```

### Slack Computation (worst path):

Tclk= 4ns      Tsu= 0.262ns      Begin\_point: rst      End\_point: out\_reg[2]

**Required Time:** The data must reach the next flip flop ‘setup time’ before the next clock edge arrives. Since  $T_{clk}=4\text{ns}$  and we have an uncertainty of 0.5. In the worst case for setup analysis, the clock can only come after 3.5ns (4-0.5). However, we have a delay of 0.5ns too. This delay and uncertainty cancel, and we are left with 4ns as the time to the next clock edge. The setup time of a flip flop is 0.262ns. Hence, we want our data to be available within 3.738ns (4-0.262) from when the current clock edge has arrived.

**Arrival Time:** This is the time our data took to reach the input pin of the flip flop. It is estimated as 3.680ns by the tool. We wanted our data to come before 3.738ns, and it came at 3.680ns only. This implies our constraint is met, and we don’t have a violation.

**Slack:** Required Time - Arrival Time= 3.738 - 3.680= 0.058ns

## GBA (Worst Path)

```
1 #####
2 # Generated by: Cadence Tempus 20.10-p003_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Fri Apr 29 19:53:49 2022
5 # Design: rtl_module
6 # Command: report_timing -late -max_paths 30 -nworst 30 -path_type full_clock -net > $report_dir/
  gba_setup.rpt
7 #####
8 Path 1: MET Setup Check with Pin out_reg[2]/CK
9 Endpoint: out_reg[2]/D (^) checked with leading edge of 'clk'
10 Beginpoint: rst (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Other End Arrival Time 0.500
13 - Setup 0.262
14 + Phase Shift 4.000
15 - Uncertainty 0.500
16 = Required Time 3.738
17 - Arrival Time 3.680
18 = Slack Time 0.058
19   Clock Rise Edge 0.000
20   + Input Delay 1.200
21   + Network Insertion Delay 0.500
22   = Beginpoint Arrival Time 1.700
```

```
23 Timing Path:
24 -----
25   Pin      Edge Net   Cell      Delay Arrival Required
26                           Time     Time
27 -----
28   rst       v    rst   -        -      1.700  1.758
29   g538/A   v    rst   CLKINVX1  0.000  1.700  1.758
30   g538/Y   ^    n_7   CLKINVX1  0.819  2.519  2.576
31   g2617/D   ^    n_7   NAND4XL  0.000  2.519  2.576
32   g2617/Y   v    n_159  NAND4XL  0.817  3.336  3.393
33   g2610/B1  v    n_159  OAI222XL 0.000  3.336  3.393
34   g2610/Y   ^    n_165  OAI222XL 0.344  3.680  3.738
35   out_reg[2]/D ^    n_165  SDFFQX1  0.000  3.680  3.738
36 -----
37   Clock Rise Edge          0.000
38   + Network Insertion Delay 0.500
39   = Beginpoint Arrival Time 0.500
40 Other End Path:
41 -----
42   Pin      Edge Net   Cell      Delay Arrival Required
43                           Time     Time
44 -----
45   clk       ^    clk   -        -      0.500  0.442
46   out_reg[2]/CK ^    clk   SDFFQX1  0.000  0.500  0.442
47 -----
```

## PBA (Worst Path)

```
8 Path 1: MET Setup Check with Pin out_reg[2]/CK
9 Endpoint: out_reg[2]/D (^) checked with leading edge of 'clk'
10 Beginpoint: rst (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Retime Analysis { Data Path-Slew }
13 Other End Arrival Time 0.500
14 - Setup 0.262
15 + Phase Shift 4.000
16 - Uncertainty 0.500
17 = Required Time 3.738
18 - Arrival Time 3.681
19 = Slack Time 0.057
20 = Slack Time(original) 0.058
21   Clock Rise Edge 0.000
22   + Input Delay 1.200
23   + Network Insertion Delay 0.500
24 = Beginpoint Arrival Time 1.700
25 -----
26   Instance Arc Cell Retime Arrival Required
27           Delay Time Time
28 -----
29   -      rst v - 1.700 1.757
30   g538   - CLKINVX1 0.000 1.700 1.757
31   g538   A v -> Y ^ CLKINVX1 0.818 2.519 2.576
32   g2617  - NAND4XL 0.000 2.519 2.576
33   g2617  D ^ -> Y v NAND4XL 0.818 3.336 3.393
34   g2610  - OAI222XL 0.000 3.336 3.393
35   g2610  B1 v -> Y ^ OAI222XL 0.345 3.681 3.738
36   out_reg[2] - SDFFQX1 0.000 3.681 3.738
37 -----
```

## Analysis For The Worst Path

We can see that using GBA, we got the slack as 0.058ns and using PBA, we got the slack as 0.057ns. Although for the worst path they are more or less the same, still PBA gave a tighter constraint than GBA, which is consistent with what we have described in the theory section of STA after DFT.

**Worst Path:  $\text{rst} \rightarrow \text{out\_reg}[2]$**

**GBA Slack: 0.058ns**

**PBA Slack: 0.057ns**

## GBA vs PBA Comparison on Path-2 for better understanding

Timing Path:						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
rst	v	rst	-	-	1.700	1.770
g538/A	v	rst	CLKINVX1	0.000	1.700	1.770
g538/Y	^	n_7	CLKINVX1	0.819	2.519	2.588
g2617/D	^	n_7	NAND4XL	0.000	2.519	2.588
g2617/Y	v	n_159	NAND4XL	0.817	3.336	3.405
g2604/A1N	v	n_159	OA12BB1X1	0.000	3.336	3.405
g2604/Y	v	n_171	OA12BB1X1	0.276	3.612	3.682
g2600/C0	v	n_171	OA1211X1	0.000	3.612	3.682
g2600/Y	^	n_174	OA1211X1	0.865	3.677	3.746
out_reg[0]/D	^	n_174	SDFFQX1	0.000	3.677	3.746
<hr/>						
Clock Rise Edge						
+ Network Insertion Delay				0.500		
= Beginpoint Arrival Time				0.500		
Other End Path:						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk	-	-	0.500	0.430
out_reg[0]/CK	^	clk	SDFFQX1	0.000	0.500	0.430
<hr/>						
38 Path 2: NET Setup Check with Pin out_reg[0]/CK						
39 Endpoint: out_reg[0]/D (^) checked with leading edge of 'clk'						
40 Beginpoint: st (v) triggered by leading edge of 'clk'						
41 Path Groups: {clk}						
42 Retime Analysis { Data Path-Slew }						
43 Other End Arrival Time				0.500		
44 - Setup				0.221		
45 + Phase Shift				4.000		
46 - Uncertainty				0.500		
47 = Required Time				3.779		
48 - Arrival Time				3.677		
49 = Slack Time				0.102		
50 = Slack Time(original)				0.070		
51 Clock Rise Edge				0.888		
52 + Input Delay				1.200		
53 + Network Insertion Delay				0.500		
54 = Beginpoint Arrival Time				1.700		
55						
56 Instance	57 Arc	58 Cell	59 Retime	60 Arrival	61 Required	62 Time
56			57	Delay	Time	Time
58			59	-	-	-
60	g538	-	61	rst v	1.700	1.802
61	g538	A v -> Y ^	62	CLKINVX1	0.818	2.519
62	g2617	-	63	NAND4XL	0.000	2.519
63	g2617	D ^ -> Y v	64	NAND4XL	0.818	3.336
64	g2604	-	65	OA12BB1X1	0.000	3.336
65	g2604	A1N v -> Y v	66	OA12BB1X1	0.276	3.613
66	g2600	-	67	OA1211X1	0.865	3.613
67	g2600	C0 v -> Y ^	68	OA1211X1	0.865	3.677
68	out_reg[0]	-	69	SDFFQX1	0.000	3.677

For this path we can clearly see the difference between slack computed using GBA vs slack computed using PBA. Slack using PBA is 0.07ns, and Slack using GBA is 0.102ns. This gives a clear picture that GBA gives a more relaxed bound as it considers the max delay at every node of the path.

## Hold Analysis (GBA vs PBA)

```
8 Path 1: VIOLATED Hold Check with Pin B_reg_reg[2]/CK
9 Endpoint: B_reg_reg[2]/SE (v) checked with leading edge of 'clk'
10 Beginpoint: scan_en (v) triggered by leading edge of '@'
11 Path Groups: {clk}
12 Other End Arrival Time      0.500
13 + Hold                      0.148
14 + Phase Shift                0.000
15 + Uncertainty                 0.500
16 = Required Time              1.148
17 Arrival Time                 0.000
18 Slack Time                  -1.148
19   Clock Rise Edge            0.000
20   + Input Delay               0.000
21   = Beginpoint Arrival Time   0.000
22   Timing Path:
23   -----
24   Pin          Edge Net     Cell     Delay Arrival Required
25   -----        -       -       -       -       -       -
26   -----
27   scan_en      v    scan_en   -      -  0.000  1.148
28   B_reg_reg[2]/SE v    scan_en   SDFFTRX1 0.000  0.000  1.148
29   -----
30   Clock Rise Edge            0.000
31   + Network Insertion Delay 0.500
32   = Beginpoint Arrival Time 0.500
33   Other End Path:
34   -----
35   Pin          Edge Net     Cell     Delay Arrival Required
36   -----        -       -       -       -       -       -
37   -----
38   clk          ^    clk   -      -  0.500  -0.648
39   B_reg_reg[2]/CK ^    clk   SDFFTRX1 0.000  0.500  -0.648
40   -----
```

```
#####
2# Generated by: Cadence Tempus 26.10 p603_1
3# OS: Linux x86_64 (Host ID edaserver4)
4# Generated on: Fri Apr 29 19:53:49 2022
5# Design: rtl_module
6# Command: report_timing -early -max_path 30 -nworst 30 -retime path_slew_propagation > $report_dir/
pba_hold.rpt
7 #####
8 Path 1: VIOLATED Hold Check with Pin B_reg_reg[2]/CK
9 Endpoint: B_reg_reg[2]/SE (v) checked with leading edge of 'clk'
10 Beginpoint: scan_en (v) triggered by leading edge of '@'
11 Path Groups: {clk}
12 Retime Analysis { Data Path-Slew }
13 Other End Arrival Time      0.500
14 + Hold                      0.148
15 + Phase Shift                0.000
16 + Uncertainty                 0.500
17 = Required Time              1.148
18 Arrival Time                 0.000
19 Slack Time                  -1.148
20 = Slack Time(original)      -1.148
21   Clock Rise Edge            0.000
22   + Input Delay               0.000
23   = Beginpoint Arrival Time   0.000
24   -----
25   Instance Arc    Cell     Retime Arrival Required
26   -----        -       -       -       -       -       -
27   -----
28   scan_en v      0.000  1.148
29   B_reg_reg[2] -  SDFFTRX1 0.000  0.000  1.148
30   -----
```

For this path both PBA and GBA gave the same slack for hold analysis. However, hold time is anyways violated. This would however, become positive in the later phase of the design.

Slack: -1.148ns

## ANALYSIS

### Netlist

```

module clk_divider_div_value3(clk_in, clk_out, DFT_sdi, DFT_sen,
    DFT_sdo);
    input clk_in, DFT_sdi, DFT_sen;
    output clk_out, DFT_sdo;
    wire clk_in, DFT_sdi, DFT_sen;
    wire clk_out, DFT_sdo;
    wire [1:0] count_reg;
    wire n_0, n_1, n_5, n_9, n_11;
    SDFFQX1 clk_out_reg(.CK (clk_in), .D (n_9), .SI (DFT_sdi), .SE
        (DFT_sen), .Q (clk_out));
    SDFFQX1 \count_reg_reg[1] (.CK (clk_in), .D (n_11), .SI
        (count_reg[0]), .SE (DFT_sen), .Q (DFT_sdo));
    SDFFQX1 \count_reg_reg[0] (.CK (clk_in), .D (n_5), .SI (clk_out), .SE
        (DFT_sen), .Q (count_reg[0]));
    NOR2XL g62(.A (count_reg[0]), .B (n_0), .Y (n_5));
    NOR2XL g67(.A (count_reg[0]), .B (n_1), .Y (n_0));
    CLKINVX1 g69(.A (DFT_sdo), .Y (n_1));
    XOR2XL g2(.A (clk_out), .B (n_0), .Y (n_9));
    AND2XL g72(.A (count_reg[0]), .B (n_1), .Y (n_11));
endmodule

```

The following generated netlist has extra input ports as the scan chain works in different modes. So, we need a MuX to select the mode of operation, and this causes extra input ports to be considered in the top module generated via DFT.

### Comparison Table

	<b>WITHOUT DFT</b>	<b>DFT</b>
<b>AREA →</b>	1395.724	1617.495
<b>CELLS →</b>	171	201
<b>TIMING SLACK →</b>	320 ps	58 ps
<b>POWER →</b>	0.293510 mW	0.326512 mW

### **When we introduced DFT: -**

- *Area Increased*
- *Number of Cells Increased*
- *Timing slack Reduced*
- *Power consumption increased*

## **CONCLUSION (QoR)**

### **Power Consumption**

Since we are increasing the total number of cells in our system, this means we increase the leakage that can occur through these devices and through the routing of these devices. The switching power has increased as well, now we have MuXed cells, and we have more possibilities of flipping. We have more input signals as well. This would cause an increase in the activity factor, and as a result, the switching power has increased too.

### **Area and Number of Cells**

Since, we have increased the total number of inputs on our system, and we are using scan flip flops, this has caused an increase in the area as well as the number of cells after we have synthesised the netlist for DFT. We are now using MuXed cells (as explained in the theory part), resulting in an increased area.

### **Timing Slack**

Since we have increased the load on the devices, the slew and delays in the system have increased post DFT. This results in arrival time increasing, and as a result, the slack of the system is reduced. It is still positive, and hence we do not have any setup violations, but the slack has reduced in comparison to synthesis without DFT due to the less load on the devices.

# Core Utilization = 0.5

## Post Placement

### Timing (Effect of Placement on Timing)

#### SETUP

```
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:08:28 2022
5 # Design: rtl_module
6 # Command: optDesign -preCTS
7 #####
8
9 -----
10 optDesign Final Summary
11 -----
12
13 +-----+-----+-----+-----+
14 | Setup mode | all | req2reg | default |
15 +-----+-----+-----+-----+
16 | WNS (ns): | 0.094 | 0.438 | 0.094 |
17 | TNS (ns): | 0.000 | 0.000 | 0.000 |
18 | Violating Paths: | 0 | 0 | 0 |
19 | All Paths: | 146 | 55 | 102 |
20 +-----+-----+-----+-----+
21
22 +-----+-----+-----+
23 | | Real | Total |
24 | DRVs | +-----+-----+
25 | | Nr nets(terms) | Worst Vio | Nr nets(terms) |
26 +-----+-----+-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 +-----+-----+-----+
32 Density: 49.907%
33 Routing Overflow: 0.00% H and 0.00% V
```

```
1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:08:28 2022
5 # Design: rtl_module
6 # Command: optDesign -preCTS
7 #####
8 Path 1: MET Setup Check with Pin out_reg[2]/D
9 Endpoint: out_reg[2]/D (^) checked with leading edge of 'clk'
10 Beginpoint: rst (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time 0.500
14 - Setup 0.261
15 + Phase Shift 4.000
16 - Uncertainty 0.500
17 = Required Time 3.739
18 - Arrival Time 3.645
19 = Slack Time 0.094
20 Clock Rise Edge 0.000
21 + Input Delay 1.200
22 + Network Insertion Delay 0.500
23 = Beginpoint Arrival Time 1.700
```

```
24 Timing Path:
25 +-----+-----+-----+-----+-----+-----+-----+
26 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
27 | | | | | | Time | Time |
28 +-----+-----+-----+-----+-----+-----+-----+
29 | rst | v | rst | | | 1.700 | 1.794 |
30 | g538/A | v | rst | CLKINVX1 | 0.000 | 1.700 | 1.794 |
31 | g538/Y | ^ | n_7 | CLKINVX1 | 0.880 | 2.580 | 2.674 |
32 | g2617/D | ^ | n_7 | NAND4X1 | 0.000 | 2.581 | 2.675 |
33 | g2617/Y | v | n_159 | NAND4X1 | 0.695 | 3.276 | 3.370 |
34 | g2610/B1 | v | n_159 | OAI222XL | 0.000 | 3.276 | 3.370 |
35 | g2610/Y | ^ | n_165 | OAI222XL | 0.369 | 3.645 | 3.739 |
36 | out_reg[2]/D | ^ | n_165 | SDFFQX1 | 0.000 | 3.645 | 3.739 |
37 +-----+-----+-----+-----+-----+-----+-----+
38 Clock Rise Edge 0.000
39 + Network Insertion Delay 0.500
40 = Beginpoint Arrival Time 0.500
41 Other End Path:
42 +-----+-----+-----+-----+-----+-----+-----+
43 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
44 | | | | | | Time | Time |
45 +-----+-----+-----+-----+-----+-----+-----+
46 | clk | ^ | clk | | | 0.500 | 0.406 |
47 | out_reg[2]/CK | ^ | clk | SDFFQX1 | 0.000 | 0.500 | 0.406 |
48 +-----+-----+-----+-----+-----+-----+-----+
```

**Analysis of STA:** We have no setup violations post placement. The timing report generated post placement is more realistic than before. Since, placement is the process where you actually place the cells somewhere and then depending on the distance between them you do STA. This means placement is a time driven phase of the design flow.

In Placement the tool first finds the critical path, then to every critical path it adds certain weight bias and then it tries to minimize the wire-length by placing cells closer.

$$\text{Slack} = \text{RT} - \text{AT} = 3.739 - 3.645 = 0.094\text{ps}$$

## Area

```
10 =====
11 General Design Information
12 =====
13 Design Status: Routed
14 Design Name: rtl_module
15 # Instances: 201
16 # Hard Macros: 0
17 # Std Cells: 201
18 -----
19 Standard Cells in Netlist
20 -----
21 | Cell Type | Instance Count | Area (um^2)
22 | OAI2BB1X1 | 2 | 10.5966
23 | | OR2XL | 3 | 13.6242
24 | OAI222XL | 1 | 8.3259
25 | AND2X1 | 1 | 4.5414
26 | OAI211X1 | 3 | 15.8949
27 | SDFFQX1 | 36 | 735.7068
28 | XNOR2X1 | 3 | 24.9777
29 | AND2XL | 24 | 108.9936
30 | XOR2XL | 1 | 8.3259
31 | OAI21X1 | 11 | 49.9554
32 | CLKINVX1 | 4 | 9.0828
33 | AOI211X1 | 1 | 5.2983
34 | NAND2BX1 | 10 | 45.4140
35 | SDFFQXL | 1 | 20.4363
36 | XNOR2XL | 3 | 24.9777
37 | NAND3X1 | 1 | 4.5414
38 | NAND2XL | 11 | 33.3036
39 | NOR2BX1 | 8 | 36.3312
40 | OAI22X1 | 3 | 18.1656
41 | OAI21XL | 1 | 4.5414
42 | AOI21X1 | 7 | 31.7898
43 | | INVXL | 1 | 2.2707
44 | NOR3X1 | 1 | 4.5414
45 | NAND4X1 | 1 | 6.0552
46 | | INVX1 | 6 | 13.6242
47 | SDFFTRX1 | 6 | 163.4904
48 | OAI22XL | 7 | 42.3864
49 | NOR2XL | 28 | 84.7728
50 | AOI22X1 | 3 | 18.1656
51 | AOI21XL | 6 | 27.2484
52 | AOI32X1 | 1 | 6.8121
53 | NAND4XL | 3 | 15.8949
54 | | MXI2XL | 3 | 18.1656
55 # Pads: 0
56 # Net: 248
57 # Special Net: 2
```

```

3436 =====
3437 Floorplan/Placement Information
3438 =====
3439 Total area of Standard cells: 1618.252 um^2
3440 Total area of Standard cells(Subtracting Physical Cells): 1618.252 um^2
3441 Total area of Macros: 0.000 um^2
3442 Total area of Blockages: 0.000 um^2
3443 Total area of Pad cells: 0.000 um^2
3444 Total area of Core: 3242.556 um^2
3445 Total area of Chip: 4233.938 um^2
3446 Effective Utilization: 4.9907e-01
3447 Number of Cell Rows: 21
3448 % Pure Gate Density #1 (Subtracting BLOCKAGES): 49.907%
3449 % Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 49.907%
3450 % Pure Gate Density #3 (Subtracting MACROS): 49.907%
3451 % Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 49.907%
3452 % Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 49.907%
3453 % Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 49.907%
3454 % Core Density (Counting Std Cells and MACROs): 49.907%
3455 % Core Density #2(Subtracting Physical Cells): 49.907%
3456 % Chip Density (Counting Std Cells and MACROs and IOs): 38.221%
3457 % Chip Density #2(Subtracting Physical Cells): 38.221%
3458 # Macros within 5 sites of IO pad: No
3459 Macro halo defined?: No
3460 =====
3461 =====
3462 Wire Length Distribution
3463 =====
3464 Total Metal1 wire length: 0.0000 um
3465 Total Metal2 wire length: 2109.3250 um
3466 Total Metal3 wire length: 1497.9050 um
3467 Total Metal4 wire length: 76.5600 um
3468 Total Metal5 wire length: 0.0000 um
3469 Total Metal6 wire length: 0.0000 um
3470 Total Metal7 wire length: 0.0000 um
3471 Total Metal8 wire length: 0.0000 um
3472 Total Metal9 wire length: 0.0000 um
3473 Total wire length: 3683.7900 um
3474 Average wire length/net: 14.8540 um
3475 Area of Power Net Distribution:
3476
3477 Area of Power Net Distribution
3478
3479 Layer Name Area of Power Net Routable Area Percentage
3480 Metal1 0.0000 3242.5596 0.0000%
3481 Metal2 0.0000 3242.5596 0.0000%
3482 Metal3 0.0000 3242.5596 0.0000%
3483 Metal4 0.0000 3242.5596 0.0000%
3484 Metal5 0.0000 3242.5596 0.0000%
3485 Metal6 0.0000 3242.5596 0.0000%
3486 Metal7 0.0000 3242.5596 0.0000%
3487 Metal8 378.5680 3242.5596 11.6750%
3488 Metal9 216.8170 3242.5596 6.6866% For more information click here
3489

```

## Area Analysis

The total number of instance increases have remained the same after placement as they were after the scan insertion stage. The total area has increased by 0.757 um square.

In the above screenshot, total effective utilization is mentioned as 0.49907 which is in accordance with the core utilization we have given as 0.5 . The distribution of different metal layers is also visible which shows that after placement only metal 2 - metal 4 layers have been used. The above screenshot also shows that no macro or pad cells have been used.

## Power

```

*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile ./PostPlacementPowerRpt/rtl_module_post_placement.rpt -rail_analysis_format VS
*
-----
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
B_reg_reg[2]	0.006367	0.0004143	0.006947	0.0001662	SDFFTRX1
B_reg_reg[0]	0.006425	0.0002744	0.006866	0.0001662	SDFFTRX1
out_reg[1]	0.006371	0.0002913	0.006799	0.0001363	SDFFQX1
A_reg_reg[8]	0.005977	0.0004095	0.006553	0.0001662	SDFFTRX1
A_reg_reg[4]	0.005978	0.0003978	0.006542	0.0001662	SDFFTRX1
A_reg_reg[6]	0.005977	0.0003867	0.00653	0.0001662	SDFFTRX1
A_reg_reg[1]	0.005978	0.0003752	0.006519	0.0001662	SDFFTRX1
out_reg[2]	0.006066	0.0002959	0.006498	0.0001363	SDFFQX1
out_reg[3]	0.00604	0.0002093	0.006382	0.0001363	SDFFQX1
out_reg[0]	0.005907	0.0002644	0.006307	0.0001363	SDFFQX1
out_reg[5]	0.005838	0.0002034	0.006178	0.0001363	SDFFQX1
out_reg[4]	0.005703	0.0002055	0.006044	0.0001363	SDFFQX1
in1/count_reg_reg[0]	0.005575	0.0002933	0.006004	0.0001363	SDFFQX1
in1/count_reg_reg[1]	0.005521	0.0003329	0.00599	0.0001363	SDFFQX1
out_reg[7]	0.005645	0.0002077	0.005989	0.0001363	SDFFQX1
out_reg[9]	0.005641	0.0001811	0.005958	0.0001363	SDFFQX1
out_reg[6]	0.005606	0.0001883	0.00593	0.0001363	SDFFQX1
out_reg[8]	0.005584	0.0001834	0.005903	0.0001363	SDFFQX1
in1/clk_out_reg	0.00533	0.0002081	0.005674	0.0001363	SDFFQX1
C_reg_reg[6]	0.005046	0.0004478	0.00563	0.0001363	SDFFQX1
B_reg_reg[8]	0.005056	0.0003407	0.005537	0.0001363	SDFFQX1
A_reg_reg[3]	0.005051	0.0003455	0.005533	0.0001363	SDFFQX1
C_reg_reg[3]	0.005051	0.0003448	0.005532	0.0001363	SDFFQX1
B_reg_reg[1]	0.005001	0.0003887	0.005526	0.0001363	SDFFQX1
A_reg_reg[2]	0.005052	0.0003267	0.005515	0.0001363	SDFFQX1
A_reg_reg[0]	0.005027	0.0003407	0.005504	0.0001363	SDFFQX1
A_reg_reg[5]	0.005052	0.0003129	0.005501	0.0001363	SDFFQX1
C_reg_reg[4]	0.005036	0.0003259	0.005498	0.0001363	SDFFQX1
B_reg_reg[3]	0.005056	0.0003005	0.005493	0.0001363	SDFFQX1
B_reg_reg[6]	0.00506	0.0002802	0.005476	0.0001363	SDFFQX1
A_reg_reg[9]	0.005051	0.0002802	0.005468	0.0001363	SDFFQX1
A_reg_reg[7]	0.005052	0.0002713	0.005459	0.0001363	SDFFQX1
B_reg_reg[4]	0.00505	0.0002489	0.005435	0.0001363	SDFFQX1
C_reg_reg[2]	0.005051	0.0002297	0.005417	0.0001363	SDFFQX1
C_reg_reg[1]	0.005051	0.0002231	0.00541	0.0001363	SDFFQX1
C_reg_reg[5]	0.005014	0.0002394	0.005389	0.0001363	SDFFQX1
C_reg_reg[0]	0.00505	0.0001803	0.005367	0.0001363	SDFFQX1
C_reg_reg[8]	0.004963	0.0002501	0.005349	0.0001363	SDFFQX1
B_reg_reg[5]	0.004856	0.0003135	0.005306	0.0001363	SDFFQX1
out_reg[10]	0.004994	7.039e-05	0.005194	0.0001296	SDFFQX1
C_reg_reg[7]	0.004849	0.0001943	0.005179	0.0001363	SDFFQX1
B_reg_reg[9]	0.0046	0.0002976	0.005034	0.0001363	SDFFQX1
B_reg_reg[7]	0.0046	0.0002183	0.004954	0.0001363	SDFFQX1
g538	0.000179	0.001597	0.001789	1.301e-05	CLKINVX1
g2617	0.000367	0.001244	0.001627	1.612e-05	NAND4X1
g2645	0.001027	0.0002093	0.001257	2.034e-05	NOR3X1
g2638	0.00059	0.0004298	0.001038	1.815e-05	AOI21X1
g2633	0.0007525	0.0001543	0.0009268	2.004e-05	NOR2BX1
g2629	0.0005061	0.0003832	0.0009023	1.299e-05	AOI21X1
g2632	0.0005848	0.0002877	0.0008906	1.815e-05	AOI21X1
g2679	0.0004911	0.0003789	0.0008899	2.004e-05	NOR2BX1
g2664	0.0006038	0.0002245	0.0008462	1.791e-05	AOI22X1
g2603	0.0005308	0.0002862	0.00083	1.299e-05	AOI21X1
g2676	0.0005998	0.0002079	0.0008278	2.004e-05	NOR2BX1
g2644	0.0006303	0.0001724	0.0008227	1.995e-05	AOI211X1
g2623	0.0004891	0.0002947	0.0007979	1.41e-05	AOI211X1

g2665	0.000615	0.0001366	0.0007698	1.815e-05	AOI21X1
g2688	0.0004907	0.000208	0.0007693	7.055e-05	XNOR2X1
g2685	0.0004893	0.0002083	0.0007682	7.055e-05	XNOR2X1
g2687	0.000492	0.0002054	0.0007679	7.055e-05	XNOR2X1
g2699	0.0004929	0.0002198	0.0007328	2.004e-05	NOR2BX1
g2651	0.0005032	0.0002107	0.000732	1.815e-05	AOI21X1
g2704	0.0002751	0.0004348	0.0007222	1.236e-05	NOR2XL
g2666	0.0004384	0.0002516	0.000703	1.299e-05	OAI21X1
g2649	0.0005265	9.949e-05	0.0006891	6.308e-05	XNOR2XL
g2681	0.0003417	0.0002988	0.0006755	3.499e-05	NAND2BX1
g2674	0.0005324	0.0001155	0.0006679	2.004e-05	NOR2BX1
g2650	0.0003927	0.0002619	0.0006675	1.299e-05	OAI21X1
g2600	0.0004397	0.000204	0.0006579	1.41e-05	OAI211X1
g2619	0.0002993	0.0003328	0.0006445	1.236e-05	NOR2XL
g2	0.0004831	9.329e-05	0.0006395	6.308e-05	XNOR2XL
g2806	0.0004824	8.827e-05	0.0006337	6.308e-05	XNOR2XL
g2777	0.0004824	0.000118	0.0006251	2.466e-05	AND2XL
g2695	0.0004913	0.0001121	0.0006234	2.004e-05	NOR2BX1
g2680	0.0002578	0.0003293	0.0006221	3.499e-05	NAND2BX1
g2772	0.0004831	0.0001127	0.0006204	2.466e-05	AND2XL
g2682	0.0004101	0.0001905	0.0006187	1.815e-05	AOI21X1
g2768	0.0004835	0.0001099	0.0006181	2.466e-05	AND2XL
g2624	0.0003315	0.0002696	0.0006152	1.41e-05	OAI211X1
g2775	0.0004844	0.0001028	0.0006118	2.466e-05	AND2XL
g2693	0.0004897	9.909e-05	0.0006088	2.004e-05	NOR2BX1
g2774	0.000487	9.383e-05	0.0006055	2.466e-05	AND2XL
g2612	0.0003553	0.0002317	0.0006054	1.833e-05	AOI22X1
g2621	0.000361	0.0002199	0.0005988	1.791e-05	OAI22X1
g2660	0.0003986	0.0001757	0.0005926	1.833e-05	AOI22X1
g2760	0.0004927	7.492e-05	0.0005923	2.466e-05	AND2XL
g2757	0.0004949	6.774e-05	0.0005873	2.466e-05	AND2XL
in1/g2	0.0004376	8.087e-05	0.0005867	6.826e-05	XOR2XL
g2602	0.0003737	0.0001895	0.0005811	1.791e-05	OAI22X1
g2773	0.0004981	5.688e-05	0.0005797	2.466e-05	AND2XL
g2675	0.0003438	0.0001941	0.0005728	3.499e-05	NAND2BX1
g2626	0.0003387	0.0002122	0.0005693	1.833e-05	AOI22X1
g2610	0.000368	0.0001667	0.0005469	1.224e-05	OAI222XL
g2641	0.0003611	0.0001621	0.0005356	1.236e-05	NOR2XL
g2711	0.0002748	0.0002349	0.000522	1.236e-05	NOR2XL
g2671	0.0003769	0.0001249	0.0005148	1.299e-05	OAI21X1
g2683	0.0002838	0.0002127	0.0005095	1.299e-05	OAI21X1
g2657	0.0003035	0.0001868	0.0005084	1.815e-05	AOI21X1
g2614	0.0003958	9.232e-05	0.0005066	1.851e-05	AOI32X1
g2700	0.000266	0.000205	0.0005061	3.499e-05	NAND2BX1
g2663	0.0003561	0.0001329	0.0005014	1.236e-05	NOR2XL
g2677	0.0003013	0.0001867	0.0005003	1.236e-05	NOR2XL
g2627	0.00037	0.0001155	0.0004977	1.22e-05	AOI21XL
g2689	0.0002575	0.00021	0.0004946	2.704e-05	MXI2XL
g2587	0.0003691	0.0001132	0.0004945	1.22e-05	AOI21XL
g2684	0.0002616	0.0001948	0.0004914	3.499e-05	NAND2BX1
g2656	0.0002936	0.0001741	0.0004858	1.815e-05	OAI21X1
g2608	0.000279	0.0001887	0.0004797	1.205e-05	OAI22XL
g2637	0.0003625	0.0001005	0.0004797	1.22e-05	AOI21XL
g2613	0.0003651	0.0001021	0.0004794	1.22e-05	AOI21XL
g2662	0.0003602	0.0001018	0.0004743	1.236e-05	NOR2XL
g2659	0.0003562	0.0001043	0.0004727	1.22e-05	AOI21XL
g2696	0.0002744	0.0001854	0.0004722	1.236e-05	NOR2XL
g2635	0.0002379	0.0002195	0.0004704	1.299e-05	OAI21X1
g2630	0.0002809	0.0001732	0.0004671	1.301e-05	INVX1
in1/g62	0.0003511	0.0001017	0.0004652	1.236e-05	NOR2XL
g2713	0.000275	0.0001743	0.0004617	1.236e-05	NOR2XL
g2710	0.0002754	0.0001709	0.0004587	1.236e-05	NOR2XL
g2591	0.0003486	8.733e-05	0.0004483	1.236e-05	NOR2XL
in1/g67	0.0002481	0.0001864	0.0004469	1.236e-05	NOR2XL
g2686	0.0002584	0.0001614	0.0004469	2.704e-05	MXI2XL
g2690	0.0002579	0.0001583	0.0004433	2.704e-05	MXI2XL
g2616	0.0003495	8.096e-05	0.0004428	1.236e-05	NOR2XL
g2628	0.0003437	8.286e-05	0.0004389	1.236e-05	NOR2XL
g2648	0.0002335	0.0001905	0.000437	1.299e-05	OAI21X1
g2639	0.0003435	7.836e-05	0.0004342	1.236e-05	NOR2XL
g2712	0.0002754	0.0001391	0.0004269	1.236e-05	NOR2XL
g2706	0.0002748	0.0001347	0.0004219	1.236e-05	NOR2XL
g2584	0.0002895	0.0001156	0.0004172	1.205e-05	OAI22XL
g2670	0.0002485	0.0001464	0.0004072	1.236e-05	NOR2XL
g2609	0.0002744	0.000118	0.0004044	1.205e-05	OAI22XL
g2604	0.0002829	9.623e-05	0.0004004	2.127e-05	OAI2BB1X1
g2607	0.0002668	0.0001148	0.0003936	1.205e-05	OAI22XL
g2601	0.0002892	9.085e-05	0.0003921	1.205e-05	OAI22XL
g2606	0.0002608	0.0001188	0.0003916	1.205e-05	OAI22XL
g2588	0.0002632	0.0001144	0.0003897	1.205e-05	OAI22XL
g2661	0.0002082	0.0001625	0.0003859	1.511e-05	NAND3X1

g2692	0.0002293	0.0001088	0.0003763	3.828e-05	OR2XL
g2738	0.00015	0.0002071	0.0003702	1.301e-05	INVX1
g2764	0.0002392	0.0001037	0.0003675	2.466e-05	AND2XL
g2708	0.0001254	0.0002258	0.0003605	9.289e-06	NAND2XL
g2654	0.0002347	0.0001124	0.0003595	1.236e-05	NOR2XL
g2673	0.0001768	0.000166	0.0003558	1.299e-05	OAI21X1
in1/g72	0.0002463	8.436e-05	0.0003553	2.466e-05	AND2XL
g2737	0.000153	0.0001874	0.0003534	1.301e-05	INVX1
g2765	0.0002407	8.39e-05	0.0003492	2.466e-05	AND2XL
g2636	0.0002187	0.000117	0.0003487	1.299e-05	OAI21X1
g2758	0.000241	7.988e-05	0.0003455	2.466e-05	AND2XL
g2755	0.0002411	7.813e-05	0.0003439	2.466e-05	AND2XL
in1/g69	0.0001897	0.0001409	0.0003436	1.301e-05	CLKINVX1
g2754	0.0002414	7.443e-05	0.0003405	2.466e-05	AND2XL
g2763	0.0002415	7.331e-05	0.0003395	2.466e-05	AND2XL
g2756	0.0002416	7.266e-05	0.0003389	2.466e-05	AND2XL
g2705	0.0002584	6.625e-05	0.000337	1.236e-05	NOR2XL
g2691	0.0002092	8.856e-05	0.0003361	3.828e-05	OR2XL
g2766	0.0002419	6.853e-05	0.0003351	2.466e-05	AND2XL
g2759	0.0002422	6.464e-05	0.0003315	2.466e-05	AND2XL
g2762	0.0002424	6.264e-05	0.0003297	2.466e-05	AND2XL
g2771	0.0002425	6.113e-05	0.0003283	2.466e-05	AND2XL
g2769	0.0002425	6.033e-05	0.0003275	2.466e-05	AND2XL
g2646	0.0002032	8.522e-05	0.0003234	3.499e-05	NAND2BX1
g2776	0.0002431	5.283e-05	0.0003206	2.466e-05	AND2XL
g2767	0.0002432	5.146e-05	0.0003194	2.466e-05	AND2XL
g2719	0.0001568	0.0001466	0.0003164	1.301e-05	INVX1
g2770	0.0002438	4.603e-05	0.0003145	2.466e-05	AND2XL
g2653	0.00016	0.0001365	0.0003058	9.289e-06	NAND2XL
g2720	0.0001546	0.0001351	0.0003027	1.301e-05	INVX1
g2701	0.0002077	7.497e-05	0.0003027	2.004e-05	NOR2BX1
g2715	0.000122	0.0001698	0.0003011	9.289e-06	NAND2XL
g2634	0.0002033	8.343e-05	0.0002991	1.236e-05	NOR2XL
g2707	0.0001744	8.173e-05	0.0002944	3.828e-05	OR2XL
g2721	0.0001569	0.0001207	0.0002906	1.301e-05	CLKINVX1
g2615	0.0001826	7.237e-05	0.0002899	3.499e-05	NAND2BX1
g2717	0.0001361	0.0001148	0.0002781	2.717e-05	AND2X1
g2618	0.0001975	6.628e-05	0.0002725	8.757e-06	INVXL
g2716	9.241e-05	0.0001591	0.0002608	9.289e-06	NAND2XL
g2672	0.0001762	7.025e-05	0.0002594	1.299e-05	OAI21X1
g2703	0.0001095	0.0001104	0.0002548	3.499e-05	NAND2BX1
g2647	0.0001498	9.238e-05	0.0002545	1.236e-05	NOR2XL
g2736	0.0001321	9.675e-05	0.0002418	1.301e-05	CLKINVX1
g2709	0.0001179	9.277e-05	0.000223	1.236e-05	NOR2XL
g2697	0.0001095	7.185e-05	0.0002163	3.499e-05	NAND2BX1
g2652	0.0001183	7.816e-05	0.0002089	1.236e-05	NOR2XL
g2678	6.617e-05	0.0001332	0.0002086	9.289e-06	NAND2XL
g2718	5.078e-05	0.0001446	0.0002047	9.289e-06	NAND2XL
g2714	0.0001121	7.53e-05	0.0001997	1.236e-05	NOR2XL
g2586	0.0001315	4.764e-05	0.0001914	1.22e-05	OAI21XL
g2643	0.0001147	4.892e-05	0.0001849	2.127e-05	OAI2BB1X1
g2761	9.071e-05	7.043e-05	0.0001704	9.289e-06	NAND2XL
g2640	0.0001143	4.17e-05	0.0001683	1.236e-05	NOR2XL
g2702	5.11e-05	9.78e-05	0.0001582	9.289e-06	NAND2XL
g2658	3.594e-05	8.201e-05	0.0001529	3.499e-05	NAND2BX1
g2592	9.548e-05	4.145e-05	0.0001457	8.728e-06	OAI21XL
g2698	5.105e-05	8.27e-05	0.000143	9.289e-06	NAND2XL
g2669	9.141e-05	3.292e-05	0.0001367	1.236e-05	NOR2XL
g2631	7.273e-05	5.324e-05	0.0001364	1.046e-05	NAND4XL
g2668	5.477e-05	4.298e-05	0.000107	9.289e-06	NAND2XL
g2694	5.391e-05	2.657e-05	8.977e-05	9.289e-06	NAND2XL
g2667	2.832e-05	4.275e-05	8.152e-05	1.046e-05	NAND4XL
g2642	2.887e-05	2.587e-05	6.52e-05	1.046e-05	NAND4XL
g2655	3.002e-05	1.149e-05	5.453e-05	1.301e-05	INVX1

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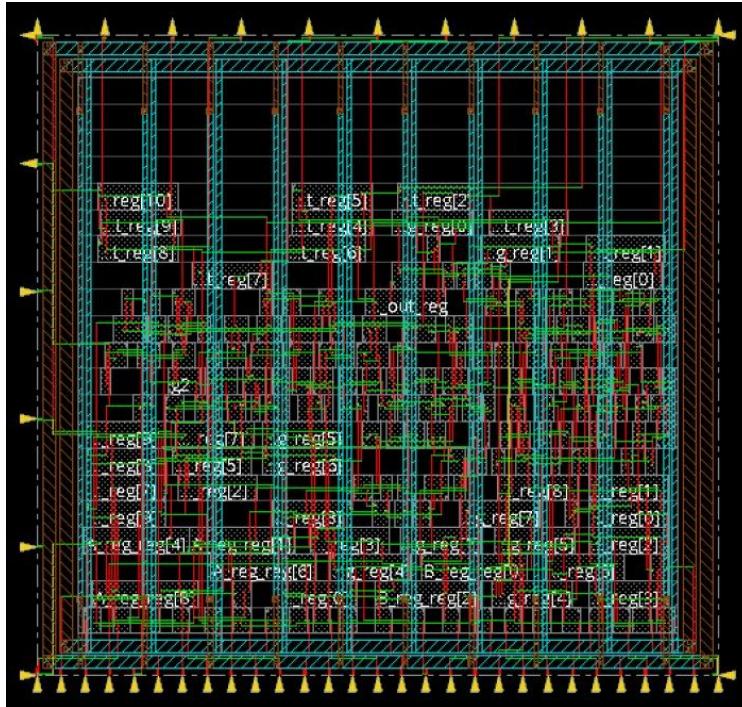
Total ( 201 of 201 )	0.2781	0.03659	0.3238	0.009177
Total Capacitance	1.304e-12 F			
Power Density	*** No Die Area ***			

## Power Analysis:

1. **Dynamic power** : the dynamic power depends upon the transition and the value of the load capacitance. Therefore, in the placement phase the tool tries to find the minimum dynamic power. For this the value of the activity factor should be fixed before finding its effect on the dynamic power. The toggle rate and the wire-length is optimized by the tool to get the minimum dynamic power dissipation. The dynamic power reported in this phase is 0.03659 mW
2. **Leakage power** : The leakage power is computed on the basis of the cells which dissipate power before they have been actually switched or any transition has occurred. The leakage power reported is 0.01584 mW.
3. It has been observed that the total power is 0.009177 mW which is greater than the power computed during the PRE-PLACE phase. Therefore, even after the tool optimizes the design for minimum power dissipation, the power after the placement increases as the cells are now physically placed on the die.
3. It has been observed that the total power is 0.3238mW which is lesser than the power computed during the PRE-PLACE phase. Therefore, the tool successfully optimized for minimum power.

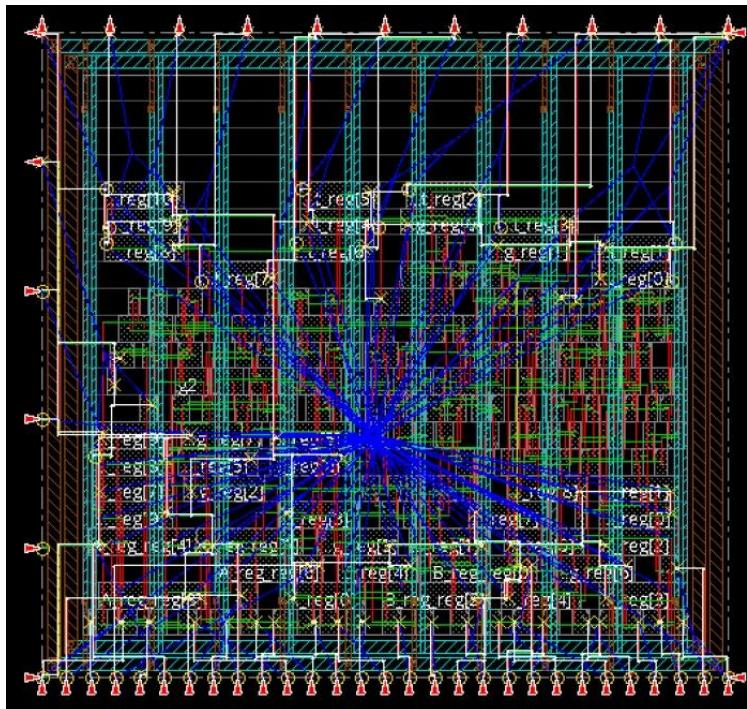
## Layout (Showing Fly Lines)

Below figure shows the layout of the design after the cells have been placed:

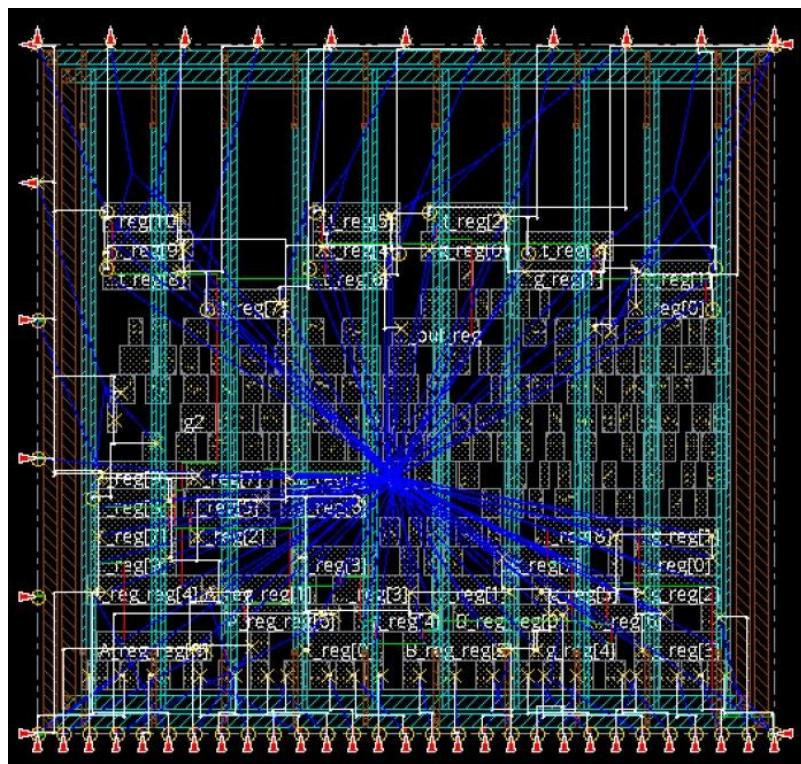


Below figures show the layout of the cells with the fly-lines

The fly-lines shows the connection between the different standard cells and the connection of the standard cells with the input and the output pins.



This shows the flylines without nets & only with standard cells placed



# Post CTS

- Timing (Effect of timing of the clock path on the overall layout)

## SETUP

```

2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:09:49 2022
5 # Design: rtl module
6 # Command: optDesign -postCTS -hold
7 #####
8
9 -----
10    optDesign Final Summary
11 -----
12
13 +-----+-----+-----+
14 | Setup mode | all | reg2reg | default |
15 +-----+-----+-----+
16 |      WNS (ns):| 0.083 | 0.417 | 0.083 |
17 |      TNS (ns):| 0.000 | 0.000 | 0.000 |
18 | Violating Paths:| 0 | 0 | 0 |
19 | All Paths:| 146 | 55 | 102 |
20 +-----+-----+-----+
21
22 +-----+-----+-----+
23 |           Real       | Total   |
24 | DRVs          | +-----+-----+
25 | | Nr nets(terms) | Worst Vio | Nr nets(terms) |
26 +-----+-----+-----+
27 | max_cap       | 0 (0)    | 0.000  | 0 (0)  |
28 | max_tran      | 0 (0)    | 0.000  | 0 (0)  |
29 | max_fanout    | 0 (0)    | 0      | 0 (0)  |
30 | max_length    | 0 (0)    | 0      | 0 (0)  |
31 +-----+-----+-----+
32
33 Density: 64.916%
34 Routing Overflow: 0.00% H and 0.00% V

```

```

1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:09:50 2022
5 # Design: rtl_module
6 # Command: optDesign -postCTS -hold
7 #####
8 Path 1: MET Setup Check with Pin out_reg[2]/CK
9 Endpoint: out_reg[2]/D (^) checked with leading edge of 'clk'
10 Beginpoint: rst (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time      0.500
14 - Setup                      0.265
15 + Phase Shift                 4.000
16 - Uncertainty                0.500
17 = Required Time              3.736
18 - Arrival Time               3.653
19 = Slack Time                 0.083
20     Clock Rise Edge          0.000
21     + Input Delay             1.200
22     + Network Insertion Delay 0.500
23     = Beginpoint Arrival Time 1.700

```

```

24 Timing Path:
25 +-----+-----+-----+-----+-----+-----+
26 | Pin   | Edge  | Net   | Cell   | Delay  | Arrival | Required |
27 |       |       |       |       |       | Time   | Time   |
28 +-----+-----+-----+-----+-----+-----+
29 | rst   | v     | rst   | CLKINVX1 | 0.000  | 1.700  | 1.783 |
30 | g538/A| v     | rst   | CLKINVX1 | 0.081  | 2.581  | 2.664 |
31 | g538/Y| ^     | n 7   | CLKINVX1 | 0.881  | 2.581  | 2.664 |
32 | g2617/D| ^     | n 7   | NAND4X1  | 0.000  | 2.582  | 2.664 |
33 | g2617/Y| v     | n 159 | NAND4X1  | 0.699  | 3.281  | 3.363 |
34 | g2610/B1| v     | n 159 | OA1222XL | 0.000  | 3.281  | 3.364 |
35 | g2610/Y | ^     | n 165 | OA1222XL | 0.372  | 3.653  | 3.735 |
36 | out_reg[2]/D | ^ | n 165 | SDFFQX1 | 0.000  | 3.653  | 3.736 |
37 +-----+-----+-----+-----+-----+-----+
38 Clock Rise Edge          0.000
39 + Source Insertion Delay  0.003
40 = Beginpoint Arrival Time 0.003
41 Other End Path:
42 +-----+-----+-----+-----+-----+-----+
43 | Pin   | Edge  | Net   | Cell   | Delay  | Arrival | Required |
44 |       |       |       |       |       | Time   | Time   |
45 +-----+-----+-----+-----+-----+-----+
46 | clk   | ^     | clk   | CLKBUFX2 | 0.003  | 0.003  | -0.079 |
47 | CTS_cdb_buf_00009/A | ^ | CTS_2 | CLKBUFX2 | 0.089  | 0.092  | 0.010 |
48 | CTS_cdb_buf_00009/Y | ^ | CTS_2 | CLKBUFX2 | 0.000  | 0.092  | 0.010 |
49 | CTS_cdb_buf_00008/A | ^ | CTS_2 | CLKBUFX2 | 0.407  | 0.499  | 0.416 |
50 | CTS_cdb_buf_00008/Y | ^ | CTS_1 | CLKBUFX2 | 0.001  | 0.500  | 0.418 |
51 | out_reg[2]/CK | ^ | CTS_1 | SDFFQX1 | 0.001  | 0.500  | 0.418 |
52 +-----+-----+-----+-----+-----+-----+

```

## HOLD

```

2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86 64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:09:49 2022
5 # Design: rtl module
6 # Command: optDesign -postCTS -hold
7 ######
8
9 -----
10 optDesign Final Summary
11 -----
12
13 +-----+-----+-----+-----+
14 | Hold mode | all | reg2reg | default |
15 +-----+-----+-----+-----+
16 | WNS (ns): | 0.006 | 0.006 | 0.024 |
17 | TNS (ns): | 0.000 | 0.000 | 0.000 |
18 | Violating Paths: | 0 | 0 | 0 |
19 | All Paths: | 146 | 55 | 102 |
20 +-----+-----+-----+-----+
21
22 +-----+-----+-----+
23 | | Real | | Total |
24 | DRVs | +-----+-----+-----+
25 | | Nr nets(terms) | Worst Vio | Nr nets(terms) |
26 +-----+-----+-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 +-----+-----+-----+
32
33 Density: 64.916%
34 Routing Overflow: 0.00% H and 0.00% V

```

```

1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86 64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:09:49 2022
5 # Design: rtl_module
6 # Command: optDesign -postCTS -hold
7 #####
8 Path 1: MET Hold Check with Pin A_reg_reg[1]/CK
9 Endpoint: A_reg_reg[1]/SI (v) checked with leading edge of 'clk'
10 Beginpoint: A_reg_reg[0]/Q (v) triggered by leading edge of 'clk'
11 Path Groups: {reg2reg}
12 Analysis View: view1
13 Other End Arrival Time 0.481
14 + Hold 0.076
15 + Phase Shift 0.000
16 + Uncertainty 0.500
17 = Required Time 1.057
18 Arrival Time 1.063
19 Slack Time 0.006
20 Clock Rise Edge 0.000
21 + Source Insertion Delay 0.003
22 = Beginpoint Arrival Time 0.003

```

Timing Path:

Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk	CLKBUFX2	0.000	0.003	-0.002
CTS_cdb_buf_00009/A	^	clk	CLKBUFX2	0.000	0.003	-0.002
CTS_cdb_buf_00009/Y	^	CTS_2	CLKBUFX2	0.089	0.092	0.087
CTS_cdb_buf_00008/A	^	CTS_2	CLKBUFX2	0.000	0.092	0.087
CTS_cdb_buf_00008/Y	^	CTS_1	CLKBUFX2	0.388	0.480	0.474
A_reg_reg[1]/CK	^	CTS_1	SDFFQX1	0.001	0.481	0.475
A_reg_reg[0]/Q	v	A_reg[0]	SDFFQX1	0.448	0.929	0.924
FE_PHN12_A_reg_0/A	v	A_reg[0]	CLKBUFX2	0.000	0.929	0.924
FE_PHN12_A_reg_0/Y	v	FE_PHN12_A_reg_0	CLKBUFX2	0.133	1.063	1.057
A_reg_reg[1]/SI	v	FE_PHN12_A_reg_0	SDFFTRX1	0.000	1.063	1.057
Clock Rise Edge				0.000		
+ Source Insertion Delay				0.003		
= Beginpoint Arrival Time				0.003		
Other End Path:						
Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk	CLKBUFX2	0.003	0.009	
CTS_cdb_buf_00009/A	^	clk	CLKBUFX2	0.000	0.003	0.009
CTS_cdb_buf_00009/Y	^	CTS_2	CLKBUFX2	0.089	0.092	0.098
CTS_cdb_buf_00008/A	^	CTS_2	CLKBUFX2	0.000	0.092	0.098
CTS_cdb_buf_00008/Y	^	CTS_1	CLKBUFX2	0.388	0.480	0.486
A_reg_reg[1]/CK	^	CTS_1	SDFFTRX1	0.001	0.481	0.487

**Analysis on STA:** During CTS the following parameters are considered:

- Skew
- Pulse Width
- Duty Cycle
- Latency
- Clock Tree Power
- Signal integrity and cross-talk

Post CTS the clock tree has been synthesized the ideal clock is converted into the propagated clock, i.e. clock containing buffers, delay elements in its path. Also, these delay elements are added to the certain inputs of the flip flop as well.

Due to the addition of these delay elements, the hold violations have gone post CTS for utilization of 0.5. Since, we have inserted delay in the data path, this means setup time of the data would increase and hence the setup slack would reduce.

**Setup Slack : 0.083ns**

**Hold Slack : 0.006ns**

By adding delay elements we are increasing the required time for the data. Hence, post CTS the setup slack goes down and hold slack increases.

- Area

```
10 =====
11 General Design Information
12 =====
13 Design Status: Routed
14 Design Name: rtl_module
15 # Instances: 255
16 # Hard Macros: 0
17 # Std Cells: 255
18 -----
19 Standard Cells in Netlist
20 -----
21          Cell Type   Instance Count   Area (um^2)
22          OAI2BB1X1      2            10.5966
23          DLY4X1        2            52.9830
24          CLKBUFX2      10           45.4140
25          OR2XL         3            13.6242
26          OAI222XL      1            8.3259
27          AND2X1        1            4.5414
28          OAI211X1      3            15.8949
29          SDFFQX1       36           735.7068
30          XNOR2X1       3            24.9777
31          DLY1X4         1            10.5966
32          AND2XL        24           108.9936
33          XOR2XL        1            8.3259
34          OAI21X1        11           49.9554
35          CLKINVX1       4            9.0828
36          AOI211X1       1            5.2983
37          NAND2BX1      10           45.4140
38          SDFFQXL        1            20.4363
39          XNOR2XL        3            24.9777
40          NAND3X1        1            4.5414
41          NAND2XL        11           33.3036
42          NOR2BX1        8             36.3312
43          OAI22X1        3            18.1656
44          OAI21XL         1            4.5414
45          AOI21X1        7             31.7898
46          INVXL          1            2.2707
47          NOR3X1          1            4.5414
48          NAND4X1          1            6.0552
49          INVX1          6             13.6242
50          SDFFTRX1        6            163.4904
51          OAI22XL         7            42.3864
52          NOR2XL          28           84.7728
53          AOI22X1         3            18.1656
54          AOI21XL         6             27.2484
55          AOI32X1         1            6.8121
56          DLY1X1          37           308.0583
57          DLY2X1          2            28.7622
58          NAND4XL          3            15.8949
59          DLY3X1          2            40.8726
60          MXI2XL          3            18.1656
61  # Pads: 0
62  # Net: 302
63  # Special Net: 2
```

```

3496 =====
3497 Floorplan/Placement Information
3498 =====
3499 Total area of Standard cells: 2104.939 um^2
3500 Total area of Standard cells(Subtracting Physical Cells): 2104.939 um^2
3501 Total area of Macros: 0.000 um^2
3502 Total area of Blockages: 0.000 um^2
3503 Total area of Pad cells: 0.000 um^2
3504 Total area of Core: 3242.560 um^2
3505 Total area of Chip: 4233.930 um^2
3506 Effective Utilization: 6.4916e-01
3507 Number of Cell Rows: 21
3508 % Pure Gate Density #1 (Subtracting BLOCKAGES): 64.916%
3509 % Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 64.916%
3510 % Pure Gate Density #3 (Subtracting MACROS): 64.916%
3511 % Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 64.916%
3512 % Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 64.916%
3513 % Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 64.916%
3514 % Core Density (Counting Std Cells and MACROs): 64.916%
3515 % Core Density #2(Subtracting Physical Cells): 64.916%
3516 % Chip Density (Counting Std Cells and MACROs and IOs): 49.716%
3517 % Chip Density #2(Subtracting Physical Cells): 49.716%
3518 # Macros within 5 sites of IO pad: No
3519 Macro halo defined?: No
3520
3521 =====
3522 Wire Length Distribution
3523 =====
3524 Total Metal1 wire length: 1.1600 um
3525 Total Metal2 wire length: 2520.4350 um
3526 Total Metal3 wire length: 1578.5350 um
3527 Total Metal4 wire length: 370.4750 um
3528 Total Metal5 wire length: 151.5250 um
3529 Total Metal6 wire length: 0.0000 um
3530 Total Metal7 wire length: 0.0000 um
3531 Total Metal8 wire length: 0.0000 um
3532 Total Metal9 wire length: 0.0000 um
3533 Total wire length: 4630.1300 um
3534 Average wire length/net: 15.3316 um
3535 Area of Power Net Distribution:
3536
3537 | Area of Power Net Distribution
3538 |
3539 | Layer Name Area of Power Net Routable Area Percentage
3540 | Metal1 0.0000 3242.5596 0.0000%
3541 | Metal2 0.0000 3242.5596 0.0000%
3542 | Metal3 0.0000 3242.5596 0.0000%
3543 | Metal4 0.0000 3242.5596 0.0000%
3544 | Metal5 0.0000 3242.5596 0.0000%
3545 | Metal6 0.0000 3242.5596 0.0000%
3546 | Metal7 0.0000 3242.5596 0.0000%
3547 | Metal8 378.5680 3242.5596 11.6750%
3548 | Metal9 216.8170 3242.5596 6.6866% For more information click here
3549

```

**Area Analysis:** The total number of instances have increased from 201 to 255 post the CTS stage as compared to post placement stage and no macros have been added. The total area has increased from 1618.252 um square to 2104.939 um square. Also the effective utilization has increased from 0.49 to 0.64 . We observe that the increase in area is mainly due to addition of Buffers and delay cells such as CLKBUFX2 and DLY1X1 which have been added by the tool in order to handle or fix the timing violations. Total metal wire length increases by approximately 1000 um since extra metal layers such as metal-1 and metal-5 have been added.

## ● Power

```

*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile ./PostCTSPowerRPT/rtl_module_post_cts.rpt -rail_analysis_format VS
*
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
CTS_cdb_buf_00008	0.003581	0.02205	0.02567	4.129e-05	CLKBUFX2
B_reg_reg[2]	0.00632	0.000449	0.006935	0.0001662	SDFFTRX1
out_reg[0]	0.006418	0.000295	0.006849	0.0001363	SDFFQX1
B_reg_reg[0]	0.00638	0.0002989	0.006845	0.0001662	SDFFTRX1
A_reg_reg[8]	0.005909	0.0004373	0.006513	0.0001662	SDFFTRX1
A_reg_reg[1]	0.005907	0.0003871	0.00646	0.0001662	SDFFTRX1
A_reg_reg[6]	0.005909	0.0003744	0.006449	0.0001662	SDFFTRX1
A_reg_reg[4]	0.005857	0.0004113	0.006434	0.0001662	SDFFTRX1
out_reg[1]	0.00593	0.0002665	0.006333	0.0001363	SDFFQX1
out_reg[2]	0.005826	0.0002505	0.006213	0.0001363	SDFFQX1
C_reg_reg[1]	0.00568	0.0003023	0.006119	0.0001363	SDFFQX1
out_reg[5]	0.005741	0.0002234	0.006101	0.0001363	SDFFQX1
out_reg[9]	0.005676	0.0001982	0.00601	0.0001363	SDFFQX1
out_reg[7]	0.005664	0.0002079	0.006008	0.0001363	SDFFQX1
out_reg[4]	0.005647	0.0002005	0.005984	0.0001363	SDFFQX1
out_reg[8]	0.005614	0.0002024	0.005953	0.0001363	SDFFQX1
out_reg[6]	0.005596	0.0001942	0.005926	0.0001363	SDFFQX1
in1/count_reg_reg[0]	0.005618	0.0001533	0.005908	0.0001363	SDFFQX1
C_reg_reg[8]	0.005319	0.0004192	0.005875	0.0001363	SDFFQX1
out_reg[3]	0.005554	0.000166	0.005856	0.0001363	SDFFQX1
in1/clk_out_reg	0.005417	0.0002519	0.005805	0.0001363	SDFFQX1
in1/count_reg_reg[1]	0.005524	8.49e-05	0.005746	0.0001363	SDFFQX1
C_reg_reg[3]	0.004973	0.0004306	0.005539	0.0001363	SDFFQX1
C_reg_reg[6]	0.004963	0.0004293	0.005528	0.0001363	SDFFQX1
A_reg_reg[0]	0.004972	0.0003861	0.005495	0.0001363	SDFFQX1
A_reg_reg[3]	0.004972	0.0003748	0.005483	0.0001363	SDFFQX1
C_reg_reg[4]	0.004941	0.0003919	0.005469	0.0001363	SDFFQX1
B_reg_reg[8]	0.004986	0.0003392	0.005462	0.0001363	SDFFQX1
B_reg_reg[1]	0.004932	0.0003908	0.005459	0.0001363	SDFFQX1
B_reg_reg[6]	0.004971	0.0003374	0.005444	0.0001363	SDFFQX1
B_reg_reg[5]	0.004949	0.0003486	0.005434	0.0001363	SDFFQX1
C_reg_reg[2]	0.004977	0.0003101	0.005424	0.0001363	SDFFQX1
B_reg_reg[4]	0.004975	0.0003053	0.005416	0.0001363	SDFFQX1
B_reg_reg[3]	0.004983	0.0002894	0.005409	0.0001363	SDFFQX1
A_reg_reg[7]	0.004978	0.0002869	0.005401	0.0001363	SDFFQX1
A_reg_reg[9]	0.004978	0.0002783	0.005393	0.0001363	SDFFQX1
A_reg_reg[2]	0.004891	0.0003476	0.005374	0.0001363	SDFFQX1
C_reg_reg[0]	0.004975	0.000172	0.005283	0.0001363	SDFFQX1
C_reg_reg[5]	0.00489	0.0002524	0.005279	0.0001363	SDFFQX1
A_reg_reg[5]	0.004776	0.000308	0.005221	0.0001363	SDFFQX1
out_reg[10]	0.00499	7.373e-05	0.005193	0.0001296	SDFFQXL
C_reg_reg[7]	0.004776	0.0002176	0.00513	0.0001363	SDFFQX1
B_reg_reg[9]	0.004528	0.0002298	0.004895	0.0001363	SDFFQX1
B_reg_reg[7]	0.004528	0.0002255	0.00489	0.0001363	SDFFQX1
CTS_cdb_buf_00009	0.003594	0.000488	0.004124	4.129e-05	CLKBUFX2
g2617	0.0004062	0.001394	0.001816	1.612e-05	NAND4X1
g538	0.0001788	0.001604	0.001796	1.301e-05	CLKINVX1
FE_PHC43_scan_en	0.0001431	0.001549	0.001733	4.129e-05	CLKBUFX2
g2645	0.001034	0.0002099	0.001264	2.034e-05	NOR3X1
FE_PHC22_out_0	0.0008734	0.0002895	0.001217	5.435e-05	DLY1X1
g2632	0.0006948	0.000346	0.001059	1.815e-05	AOI21X1
g2638	0.0005738	0.0004106	0.001003	1.815e-05	AOI21X1
in1/FE_PHC42_n_277	0.0005486	0.0003737	0.0009766	5.435e-05	DLY1X1
g2633	0.0007749	0.0001594	0.0009544	2.004e-05	NOR2BX1
g2629	0.0005125	0.0003902	0.0009157	1.299e-05	OAI21X1
g2664	0.0006383	0.0002374	0.0008937	1.791e-05	OAI22X1
g2679	0.000491	0.0003794	0.0008904	2.004e-05	NOR2BX1
FE_PHC19_C_reg_1	0.0006429	0.0001817	0.0008789	5.435e-05	DLY1X1
g2603	0.0005577	0.0002961	0.0008667	1.299e-05	OAI21X1
FE_PHC14_out_1	0.0007164	8.535e-05	0.0008561	5.435e-05	DLY1X1
in1/FE_PHC37_SPCASCAN_N0	0.0005738	0.0002218	0.0008499	5.435e-05	DLY1X1
in1/FE_PHC47_n_9	0.000716	9.114e-05	0.0008484	4.129e-05	CLKBUFX2
g2623	0.00051	0.0003151	0.0008392	1.41e-05	OAI211X1
g2644	0.000642	0.000177	0.0008389	1.995e-05	AOI211X1
FE_PHC17_out_2	0.0006697	0.0001031	0.0008271	5.435e-05	DLY1X1
g2675	0.0005032	0.0002795	0.0008177	3.499e-05	NAND2BX1
g2676	0.000582	0.0002019	0.0008039	2.004e-05	NOR2BX1

FE_PHC7_out_5	0.0006502	7.769e-05	0.0007823	5.435e-05	DLY1X1
g2624	0.0004211	0.0003435	0.0007787	1.41e-05	OAI21X1
g2665	0.0006151	0.0001367	0.00077	1.815e-05	AOI21X1
FE_PHC6_out_9	0.000628	8.55e-05	0.0007678	5.435e-05	DLY1X1
FE_PHC16_out_7	0.0006252	8.6e-05	0.0007656	5.435e-05	DLY1X1
g2687	0.0004899	0.0002051	0.0007656	7.055e-05	XNOR2X1
g2685	0.0004899	0.000203	0.0007635	7.055e-05	XNOR2X1
FE_PHC13_out_4	0.0006132	8.649e-05	0.000754	5.435e-05	DLY1X1
g2688	0.0004787	0.0002029	0.0007522	7.055e-05	XNOR2X1
FE_PHC8_out_8	0.0006092	8.379e-05	0.0007473	5.435e-05	DLY1X1
FE_PHC9_out_6	0.0006038	8.305e-05	0.0007412	5.435e-05	DLY1X1
g2682	0.000484	0.0002388	0.000741	1.815e-05	AOI21X1
FE_PHC5_out_3	0.000596	8.41e-05	0.0007344	5.435e-05	DLY1X1
g2651	0.0005051	0.0002102	0.0007335	1.815e-05	AOI21X1
g2699	0.0004924	0.0002195	0.0007319	2.004e-05	NOR2BX1
g2704	0.0002755	0.0004349	0.0007227	1.236e-05	NOR2XL
g2600	0.0004814	0.0002227	0.0007183	1.41e-05	OAI21X1
g2666	0.0004446	0.0002559	0.0007135	1.299e-05	AOI21X1
g2649	0.0005259	9.967e-05	0.0006887	6.308e-05	XNOR2XL
g2713	0.0004088	0.00026	0.0006812	1.236e-05	NOR2XL
g2681	0.0003414	0.0003008	0.0006773	3.499e-05	NAND2BX1
in1/FE_PHC39_out1	0.000529	9.359e-05	0.000677	5.435e-05	DLY1X1
g2619	0.0003121	0.0003503	0.0006747	1.236e-05	NOR2XL
g2650	0.0003965	0.0002635	0.000673	1.299e-05	OAI21X1
g2674	0.0005339	0.0001183	0.0006723	2.004e-05	NOR2BX1
FE_PHC23_C_reg_8	0.0005385	7.374e-05	0.0006665	5.435e-05	DLY1X1
FE_PHC33_B_reg_4	0.0004306	0.0001714	0.0006564	5.435e-05	DLY1X1
FE_PHC41_C_reg_4	0.0004255	0.0001788	0.0006557	5.435e-05	DLY1X1
g2711	0.0003442	0.000294	0.0006506	1.236e-05	NOR2XL
FE_PHC34_C_reg_3	0.000435	0.0001581	0.0006475	5.435e-05	DLY1X1
in1/g2	0.0004737	9.874e-05	0.0006407	6.826e-05	XOR2XL
g2	0.0004832	9.302e-05	0.0006393	6.308e-05	XNOR2XL
g2806	0.0004823	8.806e-05	0.0006334	6.308e-05	XNOR2XL
FE_PHC26_A_reg_3	0.0004334	0.00014	0.0006277	5.435e-05	DLY1X1
g2777	0.0004825	0.0001177	0.0006249	2.466e-05	AND2XL
g2695	0.0004914	0.0001118	0.0006232	2.004e-05	NOR2BX1
g2772	0.0004832	0.0001125	0.0006203	2.466e-05	AND2XL
g2768	0.0004836	0.0001095	0.0006177	2.466e-05	AND2XL
FE_PHC36_A_reg_9	0.0004324	0.0001304	0.0006171	5.435e-05	DLY1X1
FE_PHC25_B_reg_3	0.0004321	0.0001294	0.0006158	5.435e-05	DLY1X1
g2680	0.0002547	0.0003256	0.0006153	3.499e-05	NAND2BX1
g2612	0.0003618	0.0002351	0.0006152	1.833e-05	AOI22X1
g2621	0.0003703	0.0002253	0.0006135	1.791e-05	AOI22X1
g2775	0.0004842	0.0001046	0.0006134	2.466e-05	AND2XL
g2693	0.0004908	9.889e-05	0.0006098	2.004e-05	NOR2BX1
FE_PHC35_C_reg_5	0.0004073	0.0001451	0.0006068	5.435e-05	DLY1X1
g2774	0.0004871	9.372e-05	0.0006055	2.466e-05	AND2XL
FE_PHC29_B_reg_5	0.0004238	0.0001238	0.000602	5.435e-05	DLY1X1
g2760	0.0004928	7.48e-05	0.0005923	2.466e-05	AND2XL
g2660	0.0003984	0.0001753	0.000592	1.833e-05	AOI22X1
g2757	0.0004949	6.768e-05	0.0005873	2.466e-05	AND2XL
g2626	0.0003499	0.0002173	0.0005855	1.833e-05	AOI22X1
g2671	0.0004281	0.0001409	0.000582	1.299e-05	OAI21X1
g2602	0.0003772	0.0001865	0.0005816	1.791e-05	OAI22X1
g2773	0.0004982	5.684e-05	0.0005797	2.466e-05	AND2XL
FE_PHC28_B_reg_6	0.0004293	9.265e-05	0.0005763	5.435e-05	DLY1X1
FE_PHC12_A_reg_0	0.0004734	5.905e-05	0.0005737	4.129e-05	CLKBUFX2
g2610	0.000385	0.0001755	0.0005727	1.224e-05	OAI222XL
FE_PHC1_n_5	0.0004286	8.975e-05	0.0005726	5.435e-05	DLY1X1
FE_PHC2_n_0	0.0004228	9.469e-05	0.0005718	5.435e-05	DLY1X1
FE_PHC11_n_4	0.0004293	8.619e-05	0.0005698	5.435e-05	DLY1X1
FE_PHC0_C_reg_6	0.000474	5.444e-05	0.0005697	4.129e-05	CLKBUFX2
FE_PHC32_A_reg_7	0.000432	7.387e-05	0.0005602	5.435e-05	DLY1X1
FE_PHC15_B_reg_1	0.0004591	5.961e-05	0.00056	4.129e-05	CLKBUFX2
FE_PHC18_C_reg_0	0.0004291	7.626e-05	0.0005597	5.435e-05	DLY1X1
FE_PHC27_A_reg_2	0.0004092	9.175e-05	0.0005553	5.435e-05	DLY1X1
g2630	0.0003354	0.0002069	0.0005553	1.301e-05	INVX1
FE_PHC40_C_reg_2	0.0004322	6.633e-05	0.0005529	5.435e-05	DLY1X1
g2641	0.0003716	0.0001666	0.0005505	1.236e-05	NOR2XL
FE_PHC4_n_3	0.0004288	6.565e-05	0.0005488	5.435e-05	DLY1X1
FE_PHC10_n_2	0.0004292	6.023e-05	0.0005437	5.435e-05	DLY1X1
FE_PHC24_C_reg_7	0.0003734	0.0001005	0.0005283	5.435e-05	DLY1X1
FE_PHC3_n_1	0.000394	6.995e-05	0.0005183	5.435e-05	DLY1X1
g2608	0.0002994	0.0002033	0.0005147	1.205e-05	AOI22XL
g2683	0.000287	0.0002141	0.0005141	1.299e-05	OAI21X1
g2614	0.0003971	9.284e-05	0.0005085	1.851e-05	AOI32X1
g2657	0.0003026	0.0001866	0.0005073	1.815e-05	AOI21X1
FE_PHC30_A_reg_5	0.0003754	7.642e-05	0.0005062	5.435e-05	DLY1X1
g2663	0.0003586	0.0001339	0.0005048	1.236e-05	NOR2XL
g2656	0.0003059	0.0001803	0.0005043	1.815e-05	AOI21X1
g2700	0.0002621	0.0002019	0.000499	3.499e-05	NAND2BX1

g2677	0.0003006	0.0001858	0.0004988	1.236e-05	NOR2XL
g2670	0.0003045	0.0001802	0.0004971	1.236e-05	NOR2XL
FE_PHC21_DFT_sdi_1	0.0003341	4.346e-05	0.0004967	0.0001191	DLY4X1
g2689	0.000258	0.0002108	0.0004958	2.704e-05	MXI2XL
g2587	0.0003702	0.0001131	0.0004954	1.22e-05	AOI21XL
g2684	0.0002628	0.0001946	0.0004924	3.499e-05	NAND2BX1
in1/g62	0.0003707	0.0001079	0.000491	1.236e-05	NOR2XL
g2627	0.0003642	0.0001138	0.0004902	1.22e-05	AOI21XL
FE_PHC44_DFT_sdi_1	0.0003593	2.638e-05	0.0004869	0.0001012	DLY1X4
FE_PHC20_DFT_sdi_2	0.0003339	3.134e-05	0.0004844	0.0001191	DLY4X1
g2613	0.0003682	0.0001025	0.0004829	1.22e-05	AOI21XL
g2635	0.0002454	0.0002215	0.0004798	1.299e-05	OAI21X1
g2637	0.0003615	0.0001048	0.0004785	1.22e-05	AOI21XL
g2696	0.0002747	0.0001845	0.0004715	1.236e-05	NOR2XL
in1/g67	0.0002596	0.0001956	0.0004675	1.236e-05	NOR2XL
g2662	0.0003569	9.781e-05	0.0004671	1.236e-05	NOR2XL
g2689	0.0003475	0.0001022	0.000462	1.22e-05	AOI21XL
FE_PHC38_B_reg_9	0.0003234	9.473e-05	0.0004594	4.129e-05	CLKBUFX2
g2710	0.0002752	0.000171	0.0004586	1.236e-05	NOR2XL
g2591	0.0003486	8.724e-05	0.0004482	1.236e-05	NOR2XL
g2686	0.0002584	0.0001611	0.0004466	2.704e-05	MXI2XL
g2584	0.0003102	0.0001233	0.0004445	1.205e-05	OAI22XL
g2690	0.0002579	0.0001578	0.0004427	2.704e-05	MXI2XL
g2616	0.0003494	8.092e-05	0.0004427	1.236e-05	NOR2XL
g2648	0.0002337	0.0001909	0.0004376	1.299e-05	OAI21X1
g2609	0.000297	0.0001276	0.0004367	1.205e-05	OAI22XL
FE_PHC51_scan_en	0.0002696	6.849e-05	0.0004358	9.768e-05	DLY3X1
g2628	0.0003399	8.196e-05	0.0004342	1.236e-05	NOR2XL
g2639	0.0003422	7.823e-05	0.0004328	1.236e-05	NOR2XL
g2705	0.0003341	8.496e-05	0.0004314	1.236e-05	NOR2XL
g2604	0.0003066	0.0001029	0.0004308	2.127e-05	OAI2BB1X1
g2606	0.0002828	0.0001298	0.0004247	1.205e-05	OAI22XL
FE_PHC31_B_reg_7	0.0002999	7.009e-05	0.0004243	5.435e-05	DLY1X1
g2712	0.000274	0.0001379	0.0004242	1.236e-05	NOR2XL
g2706	0.0002749	0.0001348	0.0004221	1.236e-05	NOR2XL
g2601	0.0003109	9.66e-05	0.0004196	1.205e-05	OAI22XL
g2607	0.0002835	0.0001221	0.0004176	1.205e-05	OAI22XL
g2588	0.0002836	0.0001217	0.0004174	1.205e-05	OAI22XL
FE_PHC48_B_reg_9	0.0003216	3.797e-05	0.0004009	4.129e-05	CLKBUFX2
g2661	0.0002074	0.0001624	0.000385	1.511e-05	NAND3X1
FE_PHC49_scan_en	0.0002684	1.664e-05	0.0003827	9.768e-05	DLY3X1
in1/g72	0.0002577	8.857e-05	0.000371	2.466e-05	AND2XL
g2764	0.0002393	0.0001034	0.0003673	2.466e-05	AND2XL
g2692	0.0002235	0.0001035	0.0003653	3.828e-05	OR2XL
g2708	0.0001251	0.0002247	0.000359	9.289e-06	NAND2XL
g2738	0.0001455	0.0002	0.0003585	1.301e-05	INVX1
g2654	0.0002335	0.0001116	0.0003575	1.236e-05	NOR2XL
in1/g69	0.0001968	0.0001464	0.0003562	1.301e-05	CLKINVX1
g2737	0.0001545	0.0001875	0.000355	1.301e-05	INVX1
g2673	0.0001755	0.000164	0.0003525	1.299e-05	OAI21X1
FE_PHC46_scan_en	0.0002069	6.949e-05	0.0003523	7.598e-05	DLY2X1
g2636	0.0002197	0.000117	0.0003497	1.299e-05	OAI21X1
g2765	0.0002411	7.998e-05	0.0003457	2.466e-05	AND2XL
g2758	0.0002411	7.982e-05	0.0003456	2.466e-05	AND2XL
g2755	0.0002412	7.751e-05	0.0003434	2.466e-05	AND2XL
g2763	0.0002416	7.325e-05	0.0003395	2.466e-05	AND2XL
g2754	0.0002416	7.262e-05	0.0003389	2.466e-05	AND2XL
g2691	0.0002095	9.089e-05	0.0003387	3.828e-05	OR2XL
g2756	0.0002417	7.223e-05	0.0003386	2.466e-05	AND2XL
g2766	0.0002419	6.938e-05	0.0003359	2.466e-05	AND2XL
g2762	0.0002424	6.26e-05	0.0003297	2.466e-05	AND2XL
g2634	0.0002245	9.223e-05	0.0003291	1.236e-05	NOR2XL
g2759	0.0002425	6.114e-05	0.0003283	2.466e-05	AND2XL
g2771	0.0002425	6.103e-05	0.0003282	2.466e-05	AND2XL
g2646	0.0002061	8.622e-05	0.0003274	3.499e-05	NAND2BX1
g2769	0.0002426	5.973e-05	0.000327	2.466e-05	AND2XL
g2767	0.0002432	5.321e-05	0.000321	2.466e-05	AND2XL
g2776	0.0002432	5.29e-05	0.0003208	2.466e-05	AND2XL
g2719	0.0001567	0.0001464	0.0003161	1.301e-05	INVX1
g2770	0.0002438	4.608e-05	0.0003146	2.466e-05	AND2XL
FE_PHC45_DFT_sdi_2	0.0002073	2.52e-05	0.0003085	7.598e-05	DLY2X1
g2653	0.0001612	0.0001371	0.0003077	9.289e-06	NAND2XL
g2615	0.0001912	7.616e-05	0.0003024	3.499e-05	NAND2BX1
g2720	0.0001552	0.0001322	0.0003005	1.301e-05	INVX1
g2701	0.0002025	7.42e-05	0.0002967	2.004e-05	NOR2BX1
g2707	0.0001753	8.21e-05	0.0002957	3.828e-05	OR2XL
g2721	0.0001597	0.0001203	0.0002931	1.301e-05	CLKINVX1
g2715	0.0001178	0.0001641	0.0002913	9.289e-06	NAND2XL
g2618	0.0002062	7.257e-05	0.0002875	8.757e-06	INVXL
g2717	0.000138	0.000114	0.0002792	2.717e-05	AND2XL
g2672	0.00019	7.424e-05	0.0002772	1.299e-05	OAI21X1

g2647	0.000158	9.762e-05	0.000268	1.236e-05	NOR2XL
g2716	9.296e-05	0.0001609	0.0002632	9.289e-06	NAND2XL
g2703	0.000108	0.000109	0.0002521	3.499e-05	NAND2BX1
g2678	8.017e-05	0.0001597	0.0002492	9.289e-06	NAND2XL
g2718	6.263e-05	0.000175	0.000247	9.289e-06	NAND2XL
g2736	0.0001329	9.662e-05	0.0002426	1.301e-05	CLKINVX1
g2709	0.0001184	9.339e-05	0.0002242	1.236e-05	NOR2XL
FE_PHC50_scan_en	0.0001429	3.867e-05	0.0002229	4.129e-05	CLKBUFX2
g2652	0.0001249	8.263e-05	0.0002199	1.236e-05	NOR2XL
g2697	0.0001097	7.217e-05	0.0002168	3.499e-05	NAND2BX1
g2714	0.0001137	7.531e-05	0.0002014	1.236e-05	NOR2XL
g2586	0.0001377	4.953e-05	0.0001995	1.22e-05	AOI21XL
g2761	0.0001028	8.244e-05	0.0001945	9.289e-06	NAND2XL
g2643	0.0001147	4.888e-05	0.0001849	2.127e-05	OAI2BB1X1
g2640	0.0001185	4.322e-05	0.0001741	1.236e-05	NOR2XL
g2658	4.242e-05	9.6e-05	0.0001734	3.499e-05	NAND2BX1
g2702	5.185e-05	0.0001007	0.0001618	9.289e-06	NAND2XL
g2592	9.64e-05	4.174e-05	0.0001469	8.728e-06	AOI21XL
g2698	5.101e-05	8.266e-05	0.000143	9.289e-06	NAND2XL
g2631	7.647e-05	5.595e-05	0.0001429	1.046e-05	NAND4XL
g2669	8.942e-05	3.218e-05	0.000134	1.236e-05	NOR2XL
g2668	6.1e-05	4.796e-05	0.0001183	9.289e-06	NAND2XL
g2667	3.337e-05	5.159e-05	9.542e-05	1.046e-05	NAND4XL
g2694	5.364e-05	2.658e-05	8.951e-05	9.289e-06	NAND2XL
g2642	3.225e-05	2.879e-05	7.149e-05	1.046e-05	NAND4XL
g2655	3.529e-05	1.355e-05	6.186e-05	1.301e-05	INVX1

---

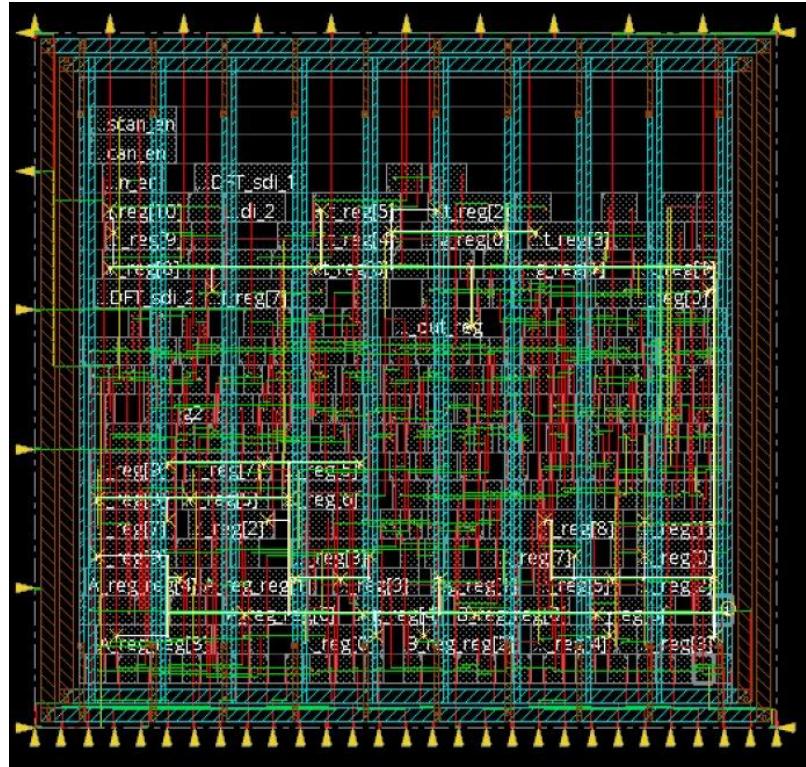
Total ( 255 of 255 )	0.3086	0.06708	0.3879	0.01229
Total Capacitance	1.815e-12 F			
Power Density	*** No Die Area ***			

### Power Analysis:

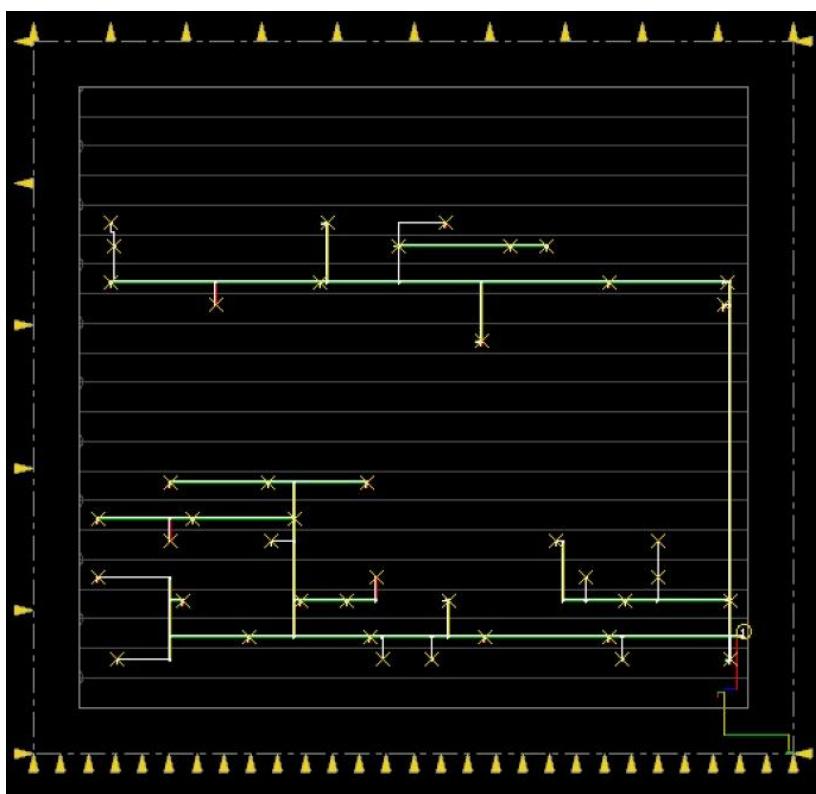
- The total power, 0.3870 mW has now increased post CTS. This is possibly due to the addition of clock buffers.
- Total Internal Power: 0.3086 mW
- Total switching power: 0.06708 mW
- Total leakage Power: 0.01229 mW

- Layout (Clock Tree)

Below screenshot shows the snapshot of the synthesized clock tree network:



After removing all standard cells we can see the clock tree:



# Post Routing

- Timing (Effect of different metal layers on timing of the path)

## SETUP

```

2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:13:31 2022
5 # Design: rtl_module
6 # Command: optDesign -postRoute -hold
7 #####
8
9 -----
10    optDesign Final SI Timing Summary
11 -----
12
13 +-----+-----+-----+
14 | Setup mode | all | req2req | default |
15 |           +-----+-----+
16 |       WNS (ns):| 0.052 | 0.306 | 0.052 |
17 |       TNS (ns):| 0.000 | 0.000 | 0.000 |
18 | Violating Paths:| 0 | 0 | 0 |
19 | All Paths:| 146 | 55 | 102 |
20 +-----+-----+-----+
21
22 +-----+-----+
23 |           Real |           Total |
24 | DRVs | Nr nets(terms) | Worst Vio | Nr nets(terms) |
25 |           +-----+-----+
26 | max_cap | 0 (0) | 0.000 | 0 (0) |
27 | max_tran | 0 (0) | 0.000 | 0 (0) |
28 | max_fanout | 0 (0) | 0 | 0 (0) |
29 | max_length | 0 (0) | 0 | 0 (0) |
30 +-----+-----+
31
32
33 Density: 65.476%
34 Total number of glitch violations: 0

```

```

1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:13:33 2022
5 # Design: rtl module
6 # Command: optDesign -postRoute -hold
7 #####
8 Path 1: MET Setup Check with Pin out_reg[2]/CK
9 Endpoint: out_reg[2]/D (^) checked with leading edge of 'clk'
10 Beginpoint: rst (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time      0.490
14 - Setup                      0.265
15 + Phase Shift                4.000
16 - Uncertainty                 0.500
17 = Required Time              3.724
18 - Arrival Time               3.672
19 = Slack Time                 0.052
20   Clock Rise Edge            0.000
21     + Input Delay             1.200
22     + Network Insertion Delay 0.500
23   = Beginpoint Arrival Time  1.700

```

```

24 Timing Path:
25 +-----+-----+-----+-----+-----+
26 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
27 |     |     |     |     | Time |     | Time |
28 |-----+-----+-----+-----+-----+
29 | rst | v   | rst |       |       | 1.700 | 1.752 |
30 | g538/A | v   | rst | CLKINVX1 | 0.000 | 1.700 | 1.752 |
31 | g538/Y | ^   | n_7  | CLKINVX1 | 0.879 | 2.579 | 2.631 |
32 | g2617/D | ^   | n_7  | NAND4X1 | 0.000 | 2.579 | 2.631 |
33 | g2617/Y | v   | n_159 | NAND4X1 | 0.732 | 3.311 | 3.363 |
34 | g2610/B1 | v   | n_159 | OA1222XL | 0.000 | 3.311 | 3.363 |
35 | g2610/Y | ^   | n_165 | OA1222XL | 0.361 | 3.672 | 3.724 |
36 | out_reg[2]/D | ^   | n_165 | SDFQX1  | 0.000 | 3.672 | 3.724 |
37 +-----+-----+-----+-----+-----+
38 Clock Rise Edge          0.000
39 = Beginpoint Arrival Time 0.000
40 Other End Path:
41 +
42 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
43 |     |     |     |     | Time |     | Time |
44 |-----+-----+-----+-----+-----+
45 | clk | ^   | clk |       |       | 0.000 | -0.052 |
46 | CTS_cdb_buf_00009/A | ^   | clk | CLKBUF2 | 0.000 | 0.000 | -0.052 |
47 | CTS_cdb_buf_00009/Y | ^   | CTS_2 | CLKBUF2 | 0.090 | 0.090 | 0.038 |
48 | CTS_cdb_buf_00008/A | ^   | CTS_2 | CLKBUF2 | 0.000 | 0.090 | 0.038 |
49 | CTS_cdb_buf_00008/Y | ^   | CTS_1 | CLKBUF2 | 0.399 | 0.488 | 0.436 |
50 | out_reg[2]/CK | ^   | CTS_1 | SDFQX1  | 0.001 | 0.490 | 0.438 |
51 +-----+-----+-----+-----+

```

## HOLD

```

2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:13:31 2022
5 # Design: rtl_module
6 # Command: optDesign -postRoute -hold
7 #####
8
9 -----
10 optDesign Final SI Timing Summary
11 -----
12
13+-----+-----+-----+
14 | Hold mode | all | reg2reg | default |
15+-----+-----+-----+
16 | WNS (ns): | 0.011 | 0.011 | 0.018 |
17 | TNS (ns): | 0.000 | 0.000 | 0.000 |
18 | Violating Paths: | 0 | 0 | 0 |
19 | All Paths: | 146 | 55 | 102 |
20+-----+-----+-----+
21
22+-----+-----+-----+
23 | | Real | Total |
24 | DRVs | Nr nets(terms) | Worst Vio | Nr nets(terms) |
25 | | | | |
26+-----+-----+-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31+-----+-----+-----+
32
33 Density: 65.476%
34 Total number of glitch violations: 0

```

```

1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:13:32 2022
5 # Design: rtl_module
6 # Command: optDesign -postRoute -hold
7 #####
8 Path 1: MET Hold Check with Pin out_reg[2]/CK
9 Endpoint: out_reg[2]/SI (v) checked with leading edge of 'clk'
10 Beginpoint: out_reg[3]/Q (v) triggered by leading edge of 'clk'
11 Path Groups: {reg2reg}
12 Analysis View: view1
13 Other End Arrival Time 0.512
14 + Hold 0.083
15 + Phase Shift 0.000
16 + Uncertainty 0.500
17 = Required Time 1.095
18 Arrival Time 1.106
19 Slack Time 0.011
20 Clock Rise Edge 0.000
21 = Beginpoint Arrival Time 0.000

```

```

22 Timing Path:
23+-----+-----+-----+-----+-----+-----+
24 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
25 | | | | | Time | | Time |
26+-----+-----+-----+-----+-----+-----+
27 | clk | ^ | clk | CLKBUFX2 | 0.000 | 0.000 | -0.011
28 | CTS_cdb_buf_00009/A | ^ | clk | CLKBUFX2 | 0.000 | 0.000 | -0.011
29 | CTS_cdb_buf_00009/Y | ^ | CTS 2 | CLKBUFX2 | 0.090 | 0.090 | 0.079
30 | CTS_cdb_buf_00008/A | ^ | CTS 2 | CLKBUFX2 | 0.000 | 0.090 | 0.079
31 | CTS_cdb_buf_00008/Y | ^ | CTS 1 | CLKBUFX2 | 0.399 | 0.489 | 0.478
32 | out_reg[3]/CK | ^ | CTS 1 | SDFFOX1 | 0.002 | 0.490 | 0.479
33 | out_reg[3]/Q | v | out[3] | SDFFOX1 | 0.394 | 0.884 | 0.873
34 | FE_PHN5.out_3/A | v | out[3] | DLY1X1 | 0.000 | 0.884 | 0.873
35 | FE_PHN5.out_3/Y | v | FE_PHN5.out 3 | DLY1X1 | 0.222 | 1.106 | 1.095
36 | out_reg[2]/SI | v | FE_PHN5.out_3 | SDFFOX1 | 0.000 | 1.106 | 1.095
37+-----+-----+-----+-----+-----+-----+
38 Clock Rise Edge 0.000
39 + Source Insertion Delay 0.003
40 = Beginpoint Arrival Time 0.003
41 Other End Path:
42+-----+-----+-----+-----+-----+-----+
43 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
44 | | | | | Time | | Time |
45+-----+-----+-----+-----+-----+-----+
46 | clk | ^ | clk | CLKBUFX2 | 0.003 | 0.003 | 0.014
47 | CTS_cdb_buf_00009/A | ^ | clk | CLKBUFX2 | 0.000 | 0.003 | 0.014
48 | CTS_cdb_buf_00009/Y | ^ | CTS 2 | CLKBUFX2 | 0.090 | 0.093 | 0.104
49 | CTS_cdb_buf_00008/A | ^ | CTS 2 | CLKBUFX2 | 0.000 | 0.093 | 0.104
50 | CTS_cdb_buf_00008/Y | ^ | CTS 1 | CLKBUFX2 | 0.418 | 0.511 | 0.522
51 | out_reg[2]/CK | ^ | CTS 1 | SDFFOX1 | 0.001 | 0.512 | 0.523
52+-----+-----+-----+-----+-----+-----+

```

**Analysis on STA:** Post routing we add metal layers to connect different cells together.

As the number of metal layers increase, the slack should reduce. Since, we need vias for a signal to go from one metal to another and this causes delay in the system. As we go towards higher metal levels, we increase their thickness and hence reduce their resistance, but then we need more vias as well. Vias have a significant resistance and hence overall the delay increases.

**Setup Slack : 0.052ns**

**Hold Slack : 0.011ns**

- Area

```

10 =====
11 General Design Information
12 =====
13 Design Status: Routed
14 Design Name: rtl_module
15 # Instances: 259
16 # Hard Macros: 0
17 # Std Cells: 259
18 -----
19 Standard Cells in Netlist
20 -----
21 | Cell Type | Instance Count | Area (um^2)
22 | OAI2BB1X1 | 2 | 10.5966
23 | | DLY4X1 | 2 | 52.9830
24 | | CLKBUFX2 | 14 | 63.5796
25 | | OR2XL | 3 | 13.6242
26 | | OAI222XL | 1 | 8.3259
27 | | AND2X1 | 1 | 4.5414
28 | | OAI211X1 | 3 | 15.8949
29 | | SDFFQX1 | 36 | 735.7068
30 | | XNOR2X1 | 3 | 24.9777
31 | | DLY1X4 | 1 | 10.5966
32 | | AND2XL | 24 | 108.9936
33 | | XOR2XL | 1 | 8.3259
34 | | OAI21X1 | 11 | 49.9554
35 | | CLKINVX1 | 4 | 9.0828
36 | | AOI211X1 | 1 | 5.2983
37 | | NAND2BX1 | 10 | 45.4140
38 | | SDFFQXL | 1 | 20.4363
39 | | XNOR2XL | 3 | 24.9777
40 | | NAND3X1 | 1 | 4.5414
41 | | NAND2XL | 11 | 33.3036
42 | | NOR2BX1 | 8 | 36.3312
43 | | OAI22X1 | 3 | 18.1656
44 | | OAI21XL | 1 | 4.5414
45 | | AOI21X1 | 7 | 31.7898
46 | | | INVXL | 1 | 2.2707
47 | | | NOR3X1 | 1 | 4.5414
48 | | | NAND4X1 | 1 | 6.0552
49 | | | INVX1 | 6 | 13.6242
50 | | | SDFFTRX1 | 6 | 163.4904
51 | | | OAI22XL | 7 | 42.3864
52 | | | NOR2XL | 28 | 84.7728
53 | | | AOI22X1 | 3 | 18.1656
54 | | | AOI21XL | 6 | 27.2484
55 | | | AOI32X1 | 1 | 6.8121
56 | | | DLY1X1 | 37 | 308.0583
57 | | | DLY2X1 | 2 | 28.7622
58 | | | NAND4XL | 3 | 15.8949
59 | | | DLY3X1 | 2 | 40.8726
60 | | | MXI2XL | 3 | 18.1656
61 # Pads: 0
62 # Net: 306
63 # Special Net: 2

```

```

3500 =====
3501 Floorplan/Placement Information
3502 =====
3503 Total area of Standard cells: 2123.105 um^2
3504 Total area of Standard cells(Subtracting Physical Cells): 2123.105 um^2
3505 Total area of Macros: 0.000 um^2
3506 Total area of Blockages: 0.000 um^2
3507 Total area of Pad cells: 0.000 um^2
3508 Total area of Core: 3242.560 um^2
3509 Total area of Chip: 4233.930 um^2
3510 Effective Utilization: 6.5476e-01
3511 Number of Cell Rows: 21
3512 % Pure Gate Density #1 (Subtracting BLOCKAGES): 65.476%
3513 % Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 65.476%
3514 % Pure Gate Density #3 (Subtracting MACROS): 65.476%
3515 % Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 65.476%
3516 % Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 65.476%
3517 % Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 65.476%
3518 % Core Density (Counting Std Cells and MACROS): 65.476%
3519 % Core Density #2(Subtracting Physical Cells): 65.476%
3520 % Chip Density (Counting Std Cells and MACROS and IOs): 50.145%
3521 % Chip Density #2(Subtracting Physical Cells): 50.145%
3522 # Macros within 5 sites of IO pads: No
3523 Macro halo defined?: No
3524 =====
3525 =====
3526 Wire Length Distribution
3527 =====
3528 Total Metal1 wire length: 198.1450 um
3529 Total Metal2 wire length: 2598.8850 um
3530 Total Metal3 wire length: 1539.6650 um
3531 Total Metal4 wire length: 517.0700 um
3532 Total Metal5 wire length: 0.0000 um
3533 Total Metal6 wire length: 0.0000 um
3534 Total Metal7 wire length: 0.0000 um
3535 Total Metal8 wire length: 0.0000 um
3536 Total Metal9 wire length: 0.0000 um
3537 Total wire length: 4853.7650 um
3538 Average wire length/net: 15.8620 um
3539 Area of Power Net Distribution:
3540 | -----
3541 | Area of Power Net Distribution
3542 | -----
3543 | Layer Name Area of Power Net Routable Area Percentage
3544 | Metal1 0.0000 3242.5596 0.0000%
3545 | Metal2 0.0000 3242.5596 0.0000%
3546 | Metal3 0.0000 3242.5596 0.0000%
3547 | Metal4 0.0000 3242.5596 0.0000%
3548 | Metal5 0.0000 3242.5596 0.0000%
3549 | Metal6 0.0000 3242.5596 0.0000%
3550 | Metal7 0.0000 3242.5596 0.0000%
3551 | Metal8 378.5680 3242.5596 11.6750%
3552 | Metal9 216.8170 3242.5596 6.6866% For more information click here
3553

```

**Area Analysis:** The total number of instances have increased from 251 to 255 post the Routing stage as compared to post CTS stage and no macros have been added. The total area has increased from 2104.939 um square to 2123.105 um square. Also the effective utilization has increased from 0.64 to 0.6547 . We observe that the increase in area is mainly due to addition of some more Buffers such as CLKBUFX2 which have been added by the tool in order to handle or fix the timing violations further. Total metal wire length increases by approximately 200 um since some extra metal has been used, mainly metal-1 has been added.

## ● Power

```

*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile ./PostRoutingPowerRpt/rtl_module.rpt -rail_analysis_format VS
*
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
CTS_cdb_buf_00008	0.00358	0.02283	0.02645	4.129e-05	CLKBUFX2
B_reg_reg[2]	0.006341	0.0004375	0.006944	0.0001662	SDFFTRX1
B_reg_reg[0]	0.0064	0.0003119	0.006878	0.0001662	SDFFTRX1
out_reg[0]	0.006442	0.0002682	0.006847	0.0001363	SDFFQX1
A_reg_reg[8]	0.00593	0.0004416	0.006538	0.0001662	SDFFTRX1
A_reg_reg[1]	0.005927	0.0003974	0.006491	0.0001662	SDFFTRX1
A_reg_reg[6]	0.005929	0.0003896	0.006485	0.0001662	SDFFTRX1
A_reg_reg[4]	0.005877	0.0004085	0.006452	0.0001662	SDFFTRX1
out_reg[1]	0.005953	0.0002478	0.006337	0.0001363	SDFFQX1
out_reg[2]	0.005848	0.0002652	0.006249	0.0001363	SDFFQX1
C_reg_reg[1]	0.005703	0.0003215	0.006161	0.0001363	SDFFQX1
out_reg[5]	0.005763	0.0001995	0.006099	0.0001363	SDFFQX1
out_reg[7]	0.005687	0.0002039	0.006027	0.0001363	SDFFQX1
out_reg[9]	0.005699	0.0001905	0.006025	0.0001363	SDFFQX1
out_reg[4]	0.00567	0.0001813	0.005988	0.0001363	SDFFQX1
out_reg[8]	0.005637	0.0002013	0.005975	0.0001363	SDFFQX1
out_reg[6]	0.005618	0.0001755	0.00593	0.0001363	SDFFQX1
in1/count_reg_reg[0]	0.00564	0.0001503	0.005927	0.0001363	SDFFQX1
C_reg_reg[8]	0.005341	0.0004036	0.005881	0.0001363	SDFFQX1
out_reg[3]	0.005575	0.0001484	0.005859	0.0001363	SDFFQX1
in1/clk_out_reg	0.005439	0.000247	0.005822	0.0001363	SDFFQX1
in1/count_reg_reg[1]	0.005546	8.71e-05	0.00577	0.0001363	SDFFQX1
C_reg_reg[3]	0.004994	0.0004419	0.005572	0.0001363	SDFFQX1
C_reg_reg[6]	0.004984	0.0004457	0.005566	0.0001363	SDFFQX1
A_reg_reg[3]	0.004994	0.0003961	0.005520	0.0001363	SDFFQX1
C_reg_reg[4]	0.004962	0.0004025	0.005501	0.0001363	SDFFQX1
B_reg_reg[8]	0.005007	0.0003398	0.005483	0.0001363	SDFFQX1
B_reg_reg[1]	0.004953	0.0003915	0.00548	0.0001363	SDFFQX1
A_reg_reg[0]	0.004993	0.0003432	0.005473	0.0001363	SDFFQX1
B_reg_reg[6]	0.004991	0.0003342	0.005462	0.0001363	SDFFQX1
B_reg_reg[5]	0.00497	0.0003383	0.005445	0.0001363	SDFFQX1
A_reg_reg[7]	0.004999	0.0003039	0.00544	0.0001363	SDFFQX1
B_reg_reg[3]	0.005004	0.0002954	0.005436	0.0001363	SDFFQX1
C_reg_reg[2]	0.004998	0.0003007	0.005435	0.0001363	SDFFQX1
A_reg_reg[9]	0.004999	0.0002874	0.005423	0.0001363	SDFFQX1
B_reg_reg[4]	0.004996	0.0002895	0.005422	0.0001363	SDFFQX1
A_reg_reg[2]	0.004912	0.0003207	0.005369	0.0001363	SDFFQX1
C_reg_reg[0]	0.004996	0.0001822	0.005315	0.0001363	SDFFQX1
C_reg_reg[5]	0.004911	0.0002565	0.005304	0.0001363	SDFFQX1
A_reg_reg[5]	0.004797	0.0003191	0.005253	0.0001363	SDFFQX1
out_reg[10]	0.005011	6.115e-05	0.005202	0.0001296	SDFFQXL
C_reg_reg[7]	0.004797	0.0002174	0.00515	0.0001363	SDFFQX1
B_reg_reg[9]	0.004549	0.0002427	0.004928	0.0001363	SDFFQX1
B_reg_reg[7]	0.004549	0.0002354	0.00492	0.0001363	SDFFQX1
CTS_cdb_buf_00009	0.003592	0.0005324	0.004165	4.129e-05	CLKBUFX2
g2617	0.000406	0.001422	0.001844	1.612e-05	NAND4X1
g538	0.0001794	0.001588	0.001781	1.301e-05	CLKINVX1
FE_PHC43_scan_en	0.0001431	0.001567	0.001751	4.129e-05	CLKBUFX2
g2645	0.001034	0.0002232	0.001278	2.034e-05	NOR3X1
FE_PHC22_out_0	0.0008732	0.000288	0.001216	5.435e-05	DLY1X1
g2632	0.0006951	0.0003461	0.001059	1.815e-05	AOI21X1
g2638	0.000574	0.0004077	0.0009999	1.815e-05	AOI21X1
g2633	0.000776	0.0001607	0.0009568	2.004e-05	NOR2BX1
in1/FE_PHC42_n_277	0.0005485	0.000351	0.0009538	5.435e-05	DLY1X1
g2629	0.0005128	0.0004195	0.0009453	1.299e-05	OAI21X1
g2664	0.0006414	0.0002479	0.0009072	1.791e-05	OAI22X1
g2679	0.0004909	0.0003941	0.0009051	2.004e-05	NOR2BX1
FE_PHC19_C_reg_1	0.0006434	0.000189	0.0008867	5.435e-05	DLY1X1
FE_PHC14_out_1	0.0007162	9.363e-05	0.0008642	5.435e-05	DLY1X1
g2603	0.0005591	0.0002904	0.0008625	1.299e-05	OAI21X1
in1/FE_PHC37_SPCASCAN_N0	0.0005738	0.0002272	0.0008554	5.435e-05	DLY1X1
in1/FE_PHC47_n_9	0.0007158	9.473e-05	0.0008518	4.129e-05	CLKBUFX2
g2644	0.0006421	0.0001806	0.0008427	1.995e-05	AOI21X1
g2623	0.00051	0.0003147	0.0008388	1.41e-05	OAI21X1
FE_PHC17_out_2	0.0006698	0.0001005	0.0008246	5.435e-05	DLY1X1
g2676	0.0005821	0.0002206	0.0008228	2.004e-05	NOR2BX1
g2675	0.0005041	0.0002826	0.0008217	3.499e-05	NAND2BX1

g2624	0.0004214	0.0003686	0.0008041	1.41e-05	OAI211X1
FE_PHC7_out_5	0.00065	8.368e-05	0.000788	5.435e-05	DLY1X1
g2687	0.0004903	0.0002167	0.0007776	7.055e-05	XNOR2X1
FE_PHC6_out_9	0.000628	9.353e-05	0.0007759	5.435e-05	DLY1X1
g2665	0.0006158	0.0001403	0.0007743	1.815e-05	AOI21X1
FE_PHC16_out_7	0.0006253	9.135e-05	0.0007711	5.435e-05	DLY1X1
g2685	0.0004905	0.0002041	0.0007651	7.055e-05	XNOR2X1
FE_PHC13_out_4	0.0006131	9.484e-05	0.0007623	5.435e-05	DLY1X1
g2688	0.0004785	0.0002113	0.0007604	7.055e-05	XNOR2X1
FE_PHC8_out_8	0.0006093	9.371e-05	0.0007573	5.435e-05	DLY1X1
g2704	0.0002754	0.000463	0.0007508	1.236e-05	NOR2XL
FE_PHC9_out_6	0.0006037	9.253e-05	0.0007506	5.435e-05	DLY1X1
FE_PHC5_out_3	0.0005959	8.839e-05	0.0007386	5.435e-05	DLY1X1
g2682	0.0004851	0.0002349	0.0007382	1.815e-05	AOI21X1
g2651	0.0005047	0.00021	0.0007329	1.815e-05	AOI21X1
g2600	0.0004816	0.000236	0.0007316	1.41e-05	OAI21X1
g2699	0.0004924	0.000216	0.0007284	2.004e-05	NOR2BX1
g2666	0.0004449	0.0002543	0.0007122	1.299e-05	AOI21X1
g2649	0.0005266	0.0001083	0.000698	6.308e-05	XNOR2XL
g2713	0.000409	0.0002661	0.0006875	1.236e-05	NOR2XL
g2619	0.0003117	0.0003631	0.0006872	1.236e-05	NOR2XL
g2650	0.0003971	0.0002764	0.0006864	1.299e-05	OAI21X1
FE_PHC33_B_reg_4	0.0004305	0.0001957	0.0006806	5.435e-05	DLY1X1
g2674	0.0005386	0.00012	0.0006787	2.004e-05	NOR2BX1
g2681	0.0003423	0.0003013	0.0006786	3.499e-05	NAND2BX1
in1/FE_PHC39_out1	0.0005288	9.067e-05	0.0006738	5.435e-05	DLY1X1
FE_PHC23_C_reg_8	0.0005381	7.851e-05	0.000671	5.435e-05	DLY1X1
g2711	0.0003442	0.0003026	0.0006592	1.236e-05	NOR2XL
FE_PHC41_C_reg_4	0.0004257	0.0001657	0.0006458	5.435e-05	DLY1X1
in1/g2	0.000473	0.0001017	0.000643	6.826e-05	XOR2XL
g2806	0.0004831	9.62e-05	0.0006424	6.308e-05	XNOR2XL
FE_PHC34_C_reg_3	0.0004352	0.0001519	0.0006415	5.435e-05	DLY1X1
g2	0.0004845	9.147e-05	0.000639	6.308e-05	XNOR2XL
g2695	0.0004914	0.0001183	0.0006297	2.004e-05	NOR2BX1
FE_PHC26_A_reg_3	0.0004339	0.0001402	0.0006285	5.435e-05	DLY1X1
FE_PHC36_A_reg_9	0.0004327	0.0001343	0.0006213	5.435e-05	DLY1X1
g2612	0.0003618	0.0002372	0.0006174	1.833e-05	AOI22X1
g2775	0.0004834	0.000108	0.0006161	2.466e-05	AND2XL
g2777	0.0004837	0.0001057	0.0006141	2.466e-05	AND2XL
g2680	0.0002547	0.0003238	0.0006134	3.499e-05	NAND2BX1
g2621	0.0003703	0.000224	0.0006122	1.791e-05	OAI22X1
FE_PHC25_B_reg_3	0.0004322	0.0001256	0.0006121	5.435e-05	DLY1X1
g2772	0.000484	0.0001033	0.000612	2.466e-05	AND2XL
g2693	0.000491	0.0001009	0.0006119	2.004e-05	NOR2BX1
g2768	0.0004843	0.0001019	0.0006109	2.466e-05	AND2XL
g2660	0.0003984	0.0001883	0.000605	1.833e-05	AOI22X1
FE_PHC52_A_reg_0	0.0004677	9.319e-05	0.0006021	4.129e-05	CLKBUFX2
FE_PHC35_C_reg_5	0.0004074	0.0001397	0.0006014	5.435e-05	DLY1X1
g2671	0.0004317	0.0001534	0.0005981	1.299e-05	AOI21X1
g2774	0.00049	8.3e-05	0.0005977	2.466e-05	AND2XL
g2760	0.0004921	7.587e-05	0.0005927	2.466e-05	AND2XL
FE_PHC0_C_reg_6	0.0004719	7.698e-05	0.0005902	4.129e-05	CLKBUFX2
g2626	0.0003501	0.0002195	0.0005879	1.833e-05	AOI22X1
FE_PHC55_C_reg_6	0.000458	8.662e-05	0.0005859	4.129e-05	CLKBUFX2
FE_PHC29_B_reg_5	0.0004234	0.0001057	0.0005834	5.435e-05	DLY1X1
g2757	0.0004971	5.937e-05	0.0005811	2.466e-05	AND2XL
g2602	0.0003772	0.0001852	0.0005804	1.791e-05	OAI22X1
FE_PHC28_B_reg_6	0.0004292	9.427e-05	0.0005779	5.435e-05	DLY1X1
g2773	0.000499	5.299e-05	0.0005767	2.466e-05	AND2XL
FE_PHC1_n_5	0.0004287	9.119e-05	0.0005742	5.435e-05	DLY1X1
FE_PHC11_n_4	0.0004293	8.9e-05	0.0005727	5.435e-05	DLY1X1
FE_PHC15_B_reg_1	0.0004577	7.204e-05	0.000571	4.129e-05	CLKBUFX2
FE_PHC2_n_0	0.0004227	9.314e-05	0.0005702	5.435e-05	DLY1X1
FE_PHC12_A_reg_0	0.0004618	6.252e-05	0.0005656	4.129e-05	CLKBUFX2
FE_PHC18_C_reg_0	0.0004299	8.109e-05	0.0005647	5.435e-05	DLY1X1
FE_PHC27_A_reg_2	0.0004086	0.0001014	0.0005644	5.435e-05	DLY1X1
FE_PHC54_B_reg_1	0.0004464	7.543e-05	0.0005631	4.129e-05	CLKBUFX2
FE_PHC32_A_reg_7	0.0004323	7.33e-05	0.00056	5.435e-05	DLY1X1
g2630	0.0003353	0.0002103	0.0005586	1.301e-05	INVX1
g2610	0.000386	0.0001556	0.0005538	1.224e-05	OAI222XL
FE_PHC40_C_reg_2	0.000432	6.723e-05	0.0005536	5.435e-05	DLY1X1
FE_PHC4_n_3	0.0004288	6.842e-05	0.0005516	5.435e-05	DLY1X1
g2641	0.0003716	0.0001639	0.0005478	1.236e-05	NOR2XL
FE_PHC10_n_2	0.0004293	6.339e-05	0.000547	5.435e-05	DLY1X1
FE_PHC24_C_reg_7	0.0003734	9.973e-05	0.0005274	5.435e-05	DLY1X1
g2657	0.0003028	0.0001974	0.0005184	1.815e-05	AOI21X1
FE_PHC3_n_1	0.000394	6.556e-05	0.0005139	5.435e-05	DLY1X1
g2627	0.0003648	0.0001363	0.0005132	1.22e-05	AOI21XL
g2614	0.0003977	9.49e-05	0.0005111	1.851e-05	AOI32X1
g2656	0.0003061	0.000184	0.0005082	1.815e-05	AOI21X1
g2663	0.0003587	0.0001353	0.0005064	1.236e-05	NOR2XL

g2670	0.0003045	0.0001879	0.0005048	1.236e-05	NOR2XL
g2683	0.0002868	0.0002049	0.0005047	1.299e-05	OAI21X1
g2613	0.0003684	0.0001235	0.0005042	1.22e-05	AOI21XL
FE_PHC30_A_reg_5	0.0003756	7.341e-05	0.0005033	5.435e-05	DLY1X1
g2677	0.0003012	0.0001888	0.0005024	1.236e-05	NOR2XL
g2684	0.0002634	0.0002002	0.0004986	3.499e-05	NAND2BX1
g2689	0.0002578	0.0002133	0.0004982	2.704e-05	MXI2XL
g2700	0.0002617	0.0002002	0.0004969	3.499e-05	NAND2BX1
g2635	0.0002456	0.0002342	0.0004928	1.299e-05	OAI21X1
FE_PHC21_DFT_sdi_1	0.000334	3.903e-05	0.0004922	0.0001191	DLY4X1
g2587	0.0003703	0.0001083	0.0004907	1.22e-05	AOI21XL
g2608	0.0003006	0.0001775	0.0004901	1.205e-05	OAI22XL
FE_PHC44_DFT_sdi_1	0.0003583	2.727e-05	0.0004867	0.0001012	DLY1X4
in1/g62	0.0003706	0.0001026	0.0004855	1.236e-05	NOR2XL
FE_PHC20_DFT_sdi_2	0.0003339	3.216e-05	0.0004852	0.0001191	DLY4X1
g2637	0.0003618	0.0001083	0.0004823	1.22e-05	AOI21XL
g2696	0.0002747	0.0001827	0.0004697	1.236e-05	NOR2XL
g2662	0.0003571	9.929e-05	0.0004688	1.236e-05	NOR2XL
g2710	0.0002753	0.0001793	0.0004669	1.236e-05	NOR2XL
FE_PHC38_B_reg_9	0.0003237	9.979e-05	0.0004648	4.129e-05	CLKBUFX2
in1/g67	0.0002596	0.0001913	0.0004632	1.236e-05	NOR2XL
g2659	0.0003478	0.0001018	0.0004618	1.22e-05	AOI21XL
g2686	0.0002583	0.000176	0.0004614	2.704e-05	MXI2XL
g2690	0.000258	0.0001689	0.0004539	2.704e-05	MXI2XL
g2591	0.0003486	9.173e-05	0.0004527	1.236e-05	NOR2XL
g2616	0.0003493	8.836e-05	0.00045	1.236e-05	NOR2XL
g2584	0.0003104	0.0001251	0.0004476	1.205e-05	OAI22XL
g2705	0.0003339	9.962e-05	0.0004459	1.236e-05	NOR2XL
g2628	0.0003402	9.152e-05	0.000444	1.236e-05	NOR2XL
g2604	0.0003068	0.0001129	0.000441	2.127e-05	OAI2BB1X1
g2712	0.000274	0.0001535	0.0004399	1.236e-05	NOR2XL
g2648	0.000234	0.000192	0.000439	1.299e-05	OAI21X1
g2639	0.0003422	8.439e-05	0.0004389	1.236e-05	NOR2XL
FE_PHC31_B_reg_7	0.0003002	7.537e-05	0.0004299	5.435e-05	DLY1X1
g2606	0.0002829	0.0001342	0.0004292	1.205e-05	OAI22XL
g2609	0.000298	0.0001174	0.0004275	1.205e-05	OAI22XL
FE_PHC51_scan_en	0.0002695	5.79e-05	0.0004251	9.768e-05	DLY3X1
g2607	0.0002835	0.0001293	0.0004249	1.205e-05	OAI22XL
g2706	0.000275	0.000137	0.0004243	1.236e-05	NOR2XL
g2601	0.0003114	9.704e-05	0.0004205	1.205e-05	OAI22XL
g2588	0.000284	0.0001236	0.0004196	1.205e-05	OAI22XL
FE_PHC48_B_reg_9	0.0003214	4.22e-05	0.0004049	4.129e-05	CLKBUFX2
g2661	0.0002075	0.000166	0.0003868	1.511e-05	NAND3X1
FE_PHC49_scan_en	0.0002684	1.619e-05	0.0003823	9.768e-05	DLY3X1
in1/g72	0.0002577	8.859e-05	0.000371	2.466e-05	AND2XL
g2673	0.0001756	0.000178	0.0003666	1.299e-05	OAI21X1
g2708	0.0001251	0.0002306	0.000365	9.289e-06	NAND2XL
g2692	0.0002235	0.0001023	0.0003641	3.828e-05	OR2XL
g2764	0.0002392	9.943e-05	0.0003633	2.466e-05	AND2XL
g2654	0.0002335	0.0001127	0.0003586	1.236e-05	NOR2XL
g2737	0.000154	0.0001914	0.0003585	1.301e-05	INVX1
g2738	0.0001456	0.0001983	0.000357	1.301e-05	INVX1
in1/g69	0.0001959	0.0001457	0.0003546	1.301e-05	CLKINVX1
FE_PHC46_scan_en	0.0002069	7.012e-05	0.000353	7.598e-05	DLY2X1
g2636	0.0002198	0.0001161	0.0003489	1.299e-05	OAI21X1
g2755	0.0002405	8.23e-05	0.0003475	2.466e-05	AND2XL
g2765	0.0002406	8.222e-05	0.0003474	2.466e-05	AND2XL
g2758	0.0002412	7.431e-05	0.0003401	2.466e-05	AND2XL
g2754	0.0002412	7.397e-05	0.0003398	2.466e-05	AND2XL
g2762	0.0002413	7.219e-05	0.0003382	2.466e-05	AND2XL
g2766	0.0002414	7.204e-05	0.0003381	2.466e-05	AND2XL
g2634	0.0002245	9.827e-05	0.0003352	1.236e-05	NOR2XL
g2691	0.0002098	8.601e-05	0.0003341	3.828e-05	OR2XL
g2756	0.0002417	6.766e-05	0.000334	2.466e-05	AND2XL
g2763	0.0002419	6.526e-05	0.0003318	2.466e-05	AND2XL
g2646	0.0002067	8.822e-05	0.0003299	3.499e-05	NAND2BX1
g2771	0.0002423	5.989e-05	0.0003269	2.466e-05	AND2XL
g2759	0.0002423	5.979e-05	0.0003268	2.466e-05	AND2XL
g2769	0.0002425	5.779e-05	0.0003249	2.466e-05	AND2XL
g2719	0.0001567	0.0001534	0.0003231	1.301e-05	INVX1
g2776	0.0002428	5.362e-05	0.0003211	2.466e-05	AND2XL
g2767	0.0002431	5.015e-05	0.0003179	2.466e-05	AND2XL
g2770	0.0002434	4.711e-05	0.0003151	2.466e-05	AND2XL
g2653	0.0001615	0.0001442	0.000315	9.289e-06	NAND2XL
FE_PHC45_DFT_sdi_2	0.0002073	2.476e-05	0.0003081	7.598e-05	DLY2X1
g2720	0.0001551	0.0001381	0.0003062	1.301e-05	INVX1
g2721	0.0001599	0.0001271	0.0003	1.301e-05	CLKINVX1
g2615	0.0001928	7.205e-05	0.0002998	3.499e-05	NAND2BX1
g2707	0.0001754	8.419e-05	0.0002978	3.828e-05	OR2XL
g2701	0.0002023	7.512e-05	0.0002975	2.004e-05	NOR2BX1
g2715	0.0001178	0.0001639	0.0002911	9.289e-06	NAND2XL

g2618	0.0002077	7.172e-05	0.0002882	8.757e-06	INVXL
g2717	0.0001381	0.0001176	0.0002829	2.717e-05	AND2X1
g2672	0.0001908	7.109e-05	0.0002749	1.299e-05	OAI21X1
g2647	0.0001581	0.0001025	0.0002729	1.236e-05	NOR2XL
g2716	9.279e-05	0.0001606	0.0002627	9.289e-06	NAND2XL
g2678	8.033e-05	0.0001655	0.0002551	9.289e-06	NAND2XL
g2718	6.265e-05	0.0001808	0.0002528	9.289e-06	NAND2XL
g2703	0.0001079	0.0001086	0.0002514	3.499e-05	NAND2BX1
g2736	0.0001329	9.566e-05	0.0002416	1.301e-05	CLKINVX1
FE_PHC50_scan_en	0.0001429	4.134e-05	0.0002255	4.129e-05	CLKBUFX2
g2709	0.0001184	9.473e-05	0.0002255	1.236e-05	NOR2XL
g2652	0.000125	8.403e-05	0.0002214	1.236e-05	NOR2XL
g2697	0.0001097	7.115e-05	0.0002158	3.499e-05	NAND2BX1
g2714	0.0001137	7.786e-05	0.000204	1.236e-05	NOR2XL
FE_PHC53_DFT_sdi_1	0.0001439	1.834e-05	0.0002035	4.129e-05	CLKBUFX2
g2586	0.000138	4.936e-05	0.0001995	1.22e-05	AOI21XL
g2761	0.0001026	8.227e-05	0.0001942	9.289e-06	NAND2XL
g2643	0.0001148	5.495e-05	0.000191	2.127e-05	OAI2BB1X1
g2658	4.244e-05	9.956e-05	0.000177	3.499e-05	NAND2BX1
g2640	0.0001187	4.521e-05	0.0001763	1.236e-05	NOR2XL
g2702	5.186e-05	0.0001037	0.0001648	9.289e-06	NAND2XL
g2631	7.654e-05	5.891e-05	0.0001459	1.046e-05	NAND4XL
g2698	5.106e-05	8.486e-05	0.0001452	9.289e-06	NAND2XL
g2592	9.646e-05	3.841e-05	0.0001436	8.728e-06	AOI21XL
g2669	8.943e-05	3.366e-05	0.0001354	1.236e-05	NOR2XL
g2668	6.119e-05	5.194e-05	0.0001224	9.289e-06	NAND2XL
g2667	3.338e-05	5.203e-05	9.587e-05	1.046e-05	NAND4XL
g2694	5.373e-05	2.852e-05	9.155e-05	9.289e-06	NAND2XL
g2642	3.228e-05	2.98e-05	7.254e-05	1.046e-05	NAND4XL
g2655	3.535e-05	1.45e-05	6.287e-05	1.301e-05	INVX1

---

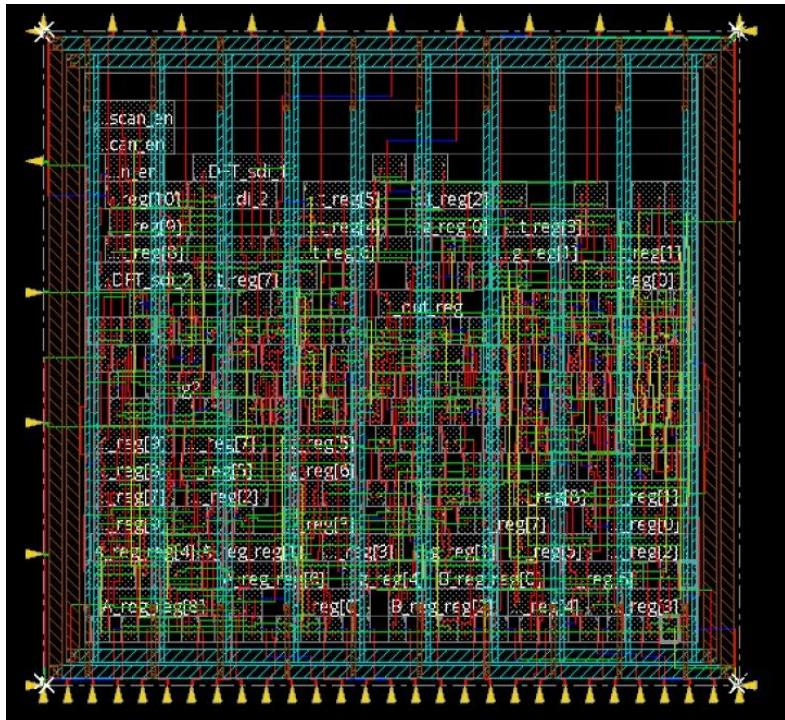
Total ( 259 of 259 )	0.311	0.06867	0.3921	0.01245
Total Capacitance	1.848e-12 F			
Power Density	*** No Die Area ***			

### Power Analysis:

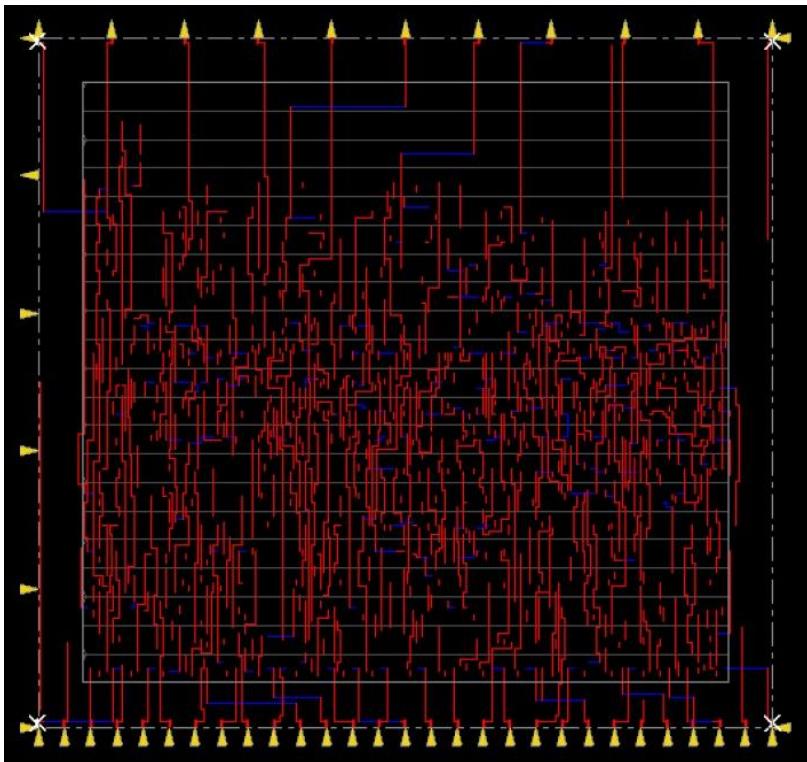
- Total Internal Power: 0.3086 mW
- Total switching power: 0.06708 mW
- Total leakage Power: 0.01229 mW
- Total Power Dissipated: 0.3921 mW
- The additional power consumed could be because we are routing via various metals layers, resulting in extra power being consumed.

- Layout (Metal Layer)

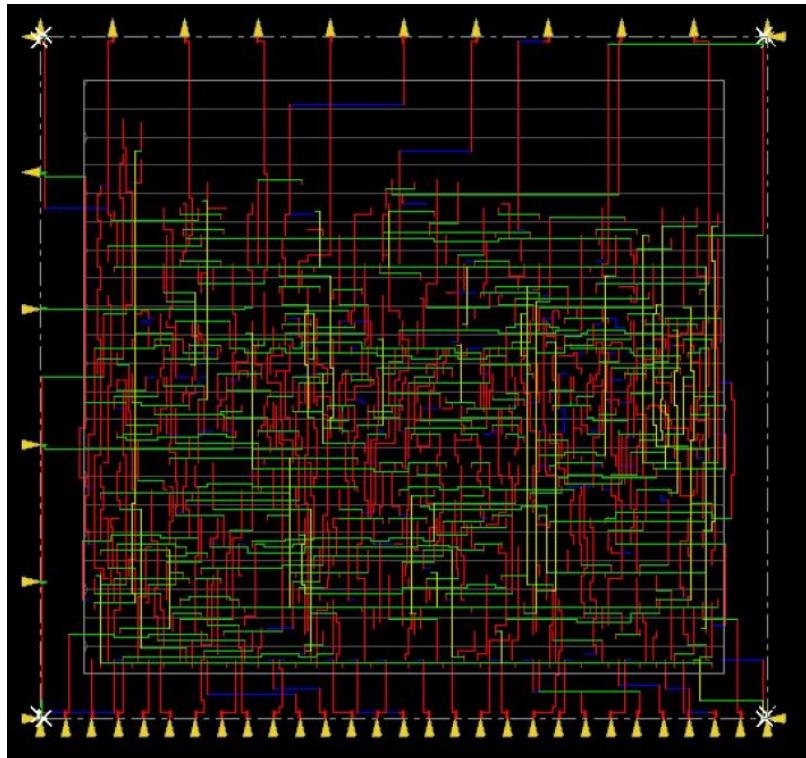
Below is the screenshots of the layout and metal layers.



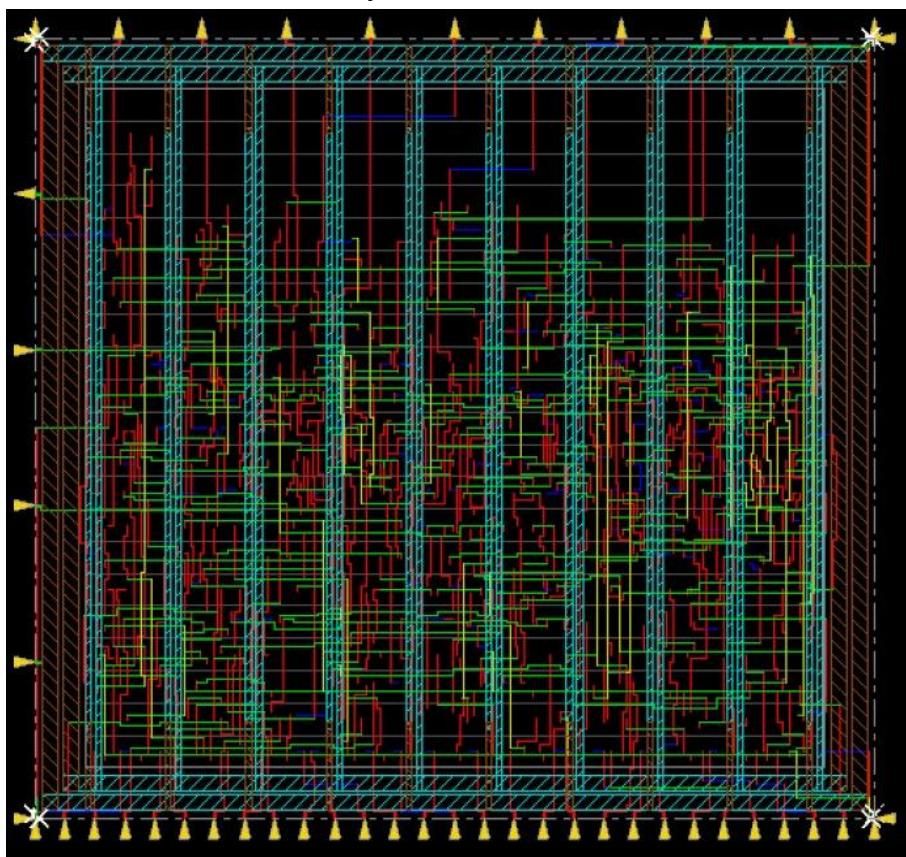
Connection between M1 & M2 Layers:



Connection between M1-M6 Metal Layers:



Connection between M1-M9 Metal Layers:





# Core Utilization = 0.8

## Post Placement

### ● Setup

```
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:07:01 2022
5 # Design: rtl_module
6 # Command: optDesign -preCTS
7 #####
8
9 -----
10    optDesign Final Summary
11 -----
12
13 +-----+-----+-----+
14 | Setup mode | all | reg/reg | default |
15 +-----+-----+-----+
16 | WNS (ns): | 0.234 | 0.494 | 0.234 |
17 | TNS (ns): | 0.000 | 0.000 | 0.000 |
18 | Violating Paths: | 0 | 0 | 0 |
19 | All Paths: | 146 | 55 | 102 |
20 +-----+-----+-----+
21
22 +-----+-----+-----+
23 | | Real | Total |
24 | DRVs | +-----+-----+
25 | | Nr nets(terms) | Worst Vio | Nr nets(terms) |
26 +-----+-----+-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 +-----+-----+-----+
32
33 Density: 79.82%
34 Routing Overflow: 0.00% H and 0.00% V
```

```
1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:07:01 2022
5 # Design: rtl_module
6 # Command: optDesign -preCTS
7 #####
8 Path 1: MET Setup Check with Pin B_reg_reg[2]/CK
9 Endpoint: B reg_reg[2]/D (v) checked with leading edge of 'clk'
10 Beginpoint: B[2] (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time 0.500
14 - Setup 2.066
15 + Phase Shift 4.000
16 - Uncertainty 0.500
17 = Required Time 1.934
18 - Arrival Time 1.700
19 = Slack Time 0.234
20 Clock Rise Edge 0.000
21 + Input Delay 1.200
22 + Network Insertion Delay 0.500
23 = Beginpoint Arrival Time 1.700
```

```
24 Timing Path:
25 +-----+-----+-----+-----+-----+
26 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
27 | | | | | | Time | Time |
28 +-----+-----+-----+-----+-----+
29 | B[2] | v | B[2] | | | 1.700 | 1.934 |
30 | B_reg_reg[2]/D | v | B[2] | SDFFTRX1 | 0.000 | 1.700 | 1.934 |
31 +-----+-----+-----+-----+-----+
32 Clock Rise Edge 0.000
33 + Network Insertion Delay 0.500
34 = Beginpoint Arrival Time 0.500
35 Other End Path:
36 +-----+-----+-----+-----+-----+
37 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
38 | | | | | | Time | Time |
39 +-----+-----+-----+-----+-----+
40 | clk | ^ | clk | | 0.500 | 0.266 |
41 | B_reg_reg[2]/CK | ^ | clk | SDFFTRX1 | 0.000 | 0.500 | 0.266 |
42 +-----+-----+-----+-----+-----+
```

Setup Slack: 1.934 - 1.700 = 0.234ns (Effect mentioned before)

## Area

```
10 =====
11 General Design Information
12 =====
13 Design Status: Routed
14 Design Name: rtl_module
15 # Instances: 202
16 # Hard Macros: 0
17 # Std Cells: 202
18 -----
19 Standard Cells in Netlist
20 -----
21 | Cell Type | Instance Count | Area (um^2)
22 | OAI2BB1X1 | 2 | 10.5966
23 | OR2XL | 3 | 13.6242
24 | BUFX2 | 1 | 4.5414
25 | OAI222XL | 1 | 8.3259
26 | AND2X1 | 1 | 4.5414
27 | OAI211X1 | 3 | 15.8949
28 | SDFFQX1 | 36 | 735.7068
29 | XNOR2X1 | 3 | 24.9777
30 | AND2XL | 24 | 108.9936
31 | XOR2XL | 1 | 8.3259
32 | OAI21X1 | 11 | 49.9554
33 | CLKINVX1 | 3 | 6.8121
34 | AOI211X1 | 1 | 5.2983
35 | NAND2BX1 | 10 | 45.4140
36 | SDFFQXL | 1 | 20.4363
37 | XNOR2XL | 3 | 24.9777
38 | NAND3X1 | 1 | 4.5414
39 | NAND2XL | 11 | 33.3036
40 | NOR2BX1 | 8 | 36.3312
41 | OAI22X1 | 3 | 18.1656
42 | OAI21XL | 1 | 4.5414
43 | AOI21X1 | 7 | 31.7898
44 | INVXL | 1 | 2.2707
45 | NOR3X1 | 1 | 4.5414
46 | NAND4X1 | 1 | 6.0552
47 | INVX1 | 7 | 15.8949
48 | SDFFTRX1 | 6 | 163.4904
49 | OAI22XL | 7 | 42.3864
50 | NOR2XL | 28 | 84.7728
51 | AOI22X1 | 3 | 18.1656
52 | AOI21XL | 6 | 27.2484
53 | AOI32X1 | 1 | 6.8121
54 | NAND4XL | 3 | 15.8949
55 | MXI2XL | 3 | 18.1656
56 # Pads: 0
57 # Net: 248
58 # Special Net: 2
```

```

3437 =====
3438 Floorplan/Placement Information
3439 =====
3440 Total area of Standard cells: 1622.794 um^2
3441 Total area of Standard cells(Subtracting Physical Cells): 1622.794 um^2
3442 Total area of Macros: 0.000 um^2
3443 Total area of Blockages: 0.000 um^2
3444 Total area of Pad cells: 0.000 um^2
3445 Total area of Core: 2033.033 um^2
3446 Total area of Chip: 2831.311 um^2
3447 Effective Utilization: 7.982e-01
3448 Number of Cell Rows: 17
3449 % Pure Gate Density #1 (Subtracting BLOCKAGES): 79.821%
3450 % Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 79.821%
3451 % Pure Gate Density #3 (Subtracting MACROS): 79.821%
3452 % Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 79.821%
3453 % Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 79.821%
3454 % Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 79.821%
3455 % Core Density (Counting Std Cells and MACROS): 79.821%
3456 % Core Density #(Subtracting Physical Cells): 79.821%
3457 % Chip Density (Counting Std Cells and MACROS and IOs): 57.316%
3458 % Chip Density #(Subtracting Physical Cells): 57.316%
3459 # Macro within 5 sites of IO pad: No
3460 Macro halo defined?: No
3461
3462 =====
3463 Wire Length Distribution
3464 =====
3465 Total Metal1 wire length: 0.0000 um
3466 Total Metal2 wire length: 2033.0500 um
3467 Total Metal3 wire length: 1247.0000 um
3468 Total Metal4 wire length: 95.9900 um
3469 Total Metal5 wire length: 0.0000 um
3470 Total Metal6 wire length: 0.0000 um
3471 Total Metal7 wire length: 0.0000 um
3472 Total Metal8 wire length: 0.0000 um
3473 Total Metal9 wire length: 0.0000 um
3474 Total wire length: 3376.0400 um
3475 Average wire length/net: 13.6131 um
3476 Area of Power Net Distribution:
3477 -----
3478 Area of Power Net Distribution
3479 -----
3480 Layer Name Area of Power Net Routable Area Percentage
3481 Metal1 0.0000 2033.0334 0.0000%
3482 Metal2 0.0000 2033.0334 0.0000%
3483 Metal3 0.0000 2033.0334 0.0000%
3484 Metal4 0.0000 2033.0334 0.0000%
3485 Metal5 0.0000 2033.0334 0.0000%
3486 Metal6 0.0000 2033.0334 0.0000%
3487 Metal7 0.0000 2033.0334 0.0000%
3488 Metal8 299.2820 2033.0334 14.7210%
3489 Metal9 190.7170 2033.0334 9.3809% For more information click here
3490

```

**Area Analysis:** The total number of instances have increased by 1 after placement as they were after the scan insertion stage. The total area has increased by 5 um square. In the above screenshot, total effective utilization is mentioned as 0.7982 which is in accordance with the core utilization we have given as 0.8 . The distribution of different metal layers is also visible which shows that after placement only metal 2 - metal 4 layers have been used. The above screenshot also shows that no macro or pad cells have been used.

## Power

```

* Power Units = 1mW
*
* Time Units = 1e-09 secs
*
* Temperature = 125
*
* report_power -outfile ./PostPlacementPowerRpt/rtl_module_post_placement.rpt -rail_analysis_format VS
*
-----
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
B_reg_reg[2]	0.006371	0.0004141	0.006952	0.0001662	SDFFTRX1
B_reg_reg[0]	0.006369	0.0003491	0.006884	0.0001662	SDFFTRX1
out_reg[1]	0.006334	0.0001972	0.006667	0.0001363	SDFFQX1
out_reg[2]	0.006228	0.0002637	0.006628	0.0001363	SDFFQX1
A_reg_reg[1]	0.005926	0.0004258	0.006518	0.0001662	SDFFTRX1
A_reg_reg[4]	0.005914	0.0004152	0.006495	0.0001662	SDFFTRX1
A_reg_reg[6]	0.005951	0.0003623	0.00648	0.0001662	SDFFTRX1
A_reg_reg[8]	0.005933	0.0003727	0.006472	0.0001662	SDFFTRX1
out_reg[4]	0.005914	0.0001437	0.006194	0.0001363	SDFFQX1
out_reg[3]	0.005793	0.0002551	0.006184	0.0001363	SDFFQX1
in1/count_reg_reg[0]	0.005696	0.0003302	0.006163	0.0001363	SDFFQX1
in1/count_reg_reg[1]	0.005601	0.000339	0.006076	0.0001363	SDFFQX1
out_reg[0]	0.005716	0.0001876	0.00604	0.0001363	SDFFQX1
out_reg[5]	0.005709	0.0001756	0.006021	0.0001363	SDFFQX1
out_reg[6]	0.005644	0.0001324	0.005913	0.0001363	SDFFQX1
B_reg_reg[1]	0.005259	0.0004868	0.005882	0.0001363	SDFFQX1
in1/clk_out_reg	0.005493	0.0002506	0.005879	0.0001363	SDFFQX1
out_reg[9]	0.005577	0.0001366	0.00585	0.0001363	SDFFQX1
out_reg[8]	0.005552	0.0001287	0.005817	0.0001363	SDFFQX1
out_reg[7]	0.005531	0.0001431	0.00581	0.0001363	SDFFQX1
B_reg_reg[9]	0.00532	0.0003485	0.005805	0.0001363	SDFFQX1
B_reg_reg[7]	0.00517	0.0004033	0.00571	0.0001363	SDFFQX1
A_reg_reg[3]	0.00505	0.0004019	0.005588	0.0001363	SDFFQX1
C_reg_reg[6]	0.005015	0.0004211	0.005572	0.0001363	SDFFQX1
C_reg_reg[4]	0.005038	0.000376	0.00555	0.0001363	SDFFQX1
A_reg_reg[5]	0.005043	0.0003423	0.005521	0.0001363	SDFFQX1
B_reg_reg[3]	0.005059	0.0003256	0.005521	0.0001363	SDFFQX1
C_reg_reg[3]	0.005049	0.0003277	0.005513	0.0001363	SDFFQX1
A_reg_reg[2]	0.005037	0.0003302	0.005503	0.0001363	SDFFQX1
C_reg_reg[2]	0.005051	0.0002848	0.005472	0.0001363	SDFFQX1
B_reg_reg[8]	0.00506	0.0002748	0.005471	0.0001363	SDFFQX1
A_reg_reg[9]	0.005052	0.0002726	0.00546	0.0001363	SDFFQX1
A_reg_reg[0]	0.005015	0.000308	0.005459	0.0001363	SDFFQX1
B_reg_reg[4]	0.005058	0.0002583	0.005452	0.0001363	SDFFQX1
B_reg_reg[5]	0.004972	0.0003266	0.005434	0.0001363	SDFFQX1
C_reg_reg[0]	0.005051	0.000221	0.005408	0.0001363	SDFFQX1
C_reg_reg[1]	0.005046	0.000194	0.005376	0.0001363	SDFFQX1
C_reg_reg[7]	0.004963	0.0002566	0.005356	0.0001363	SDFFQX1
B_reg_reg[6]	0.004856	0.0002605	0.005253	0.0001363	SDFFQX1
C_reg_reg[5]	0.004848	0.0002123	0.005197	0.0001363	SDFFQX1
out_reg[10]	0.004894	3.419e-05	0.005058	0.0001296	SDFFQXL
A_reg_reg[7]	0.004592	0.0001922	0.00492	0.0001363	SDFFQX1
C_reg_reg[8]	0.004592	0.0001881	0.004916	0.0001363	SDFFQX1
FE_OFC1_rst	0.0003849	0.001337	0.001763	4.129e-05	BUFX2
g2617	0.0003473	0.001103	0.001466	1.612e-05	NAND4X1
g2645	0.001003	0.0002399	0.001263	2.034e-05	NOR3X1
g2679	0.0005671	0.0004612	0.001048	2.004e-05	NOR2BX1
g2638	0.0005735	0.0004316	0.001023	1.815e-05	AOI21X1
g2629	0.0005458	0.0004481	0.001007	1.299e-05	OAI21X1
g2633	0.0007343	0.0001572	0.0009116	2.004e-05	NOR2BX1
g2687	0.0005728	0.000262	0.0009054	7.055e-05	XNOR2X1
g2651	0.0005844	0.0002728	0.0008753	1.815e-05	AOI21X1
g2644	0.0006462	0.000204	0.0008701	1.995e-05	AOI211X1
g2665	0.000666	0.0001519	0.0008561	1.815e-05	AOI21X1
g2603	0.0005427	0.0002948	0.0008505	1.299e-05	OAI21X1
g2664	0.0006024	0.0002254	0.0008457	1.791e-05	OAI22X1
g2632	0.0005519	0.0002641	0.0008341	1.815e-05	AOI21X1
g2623	0.0004941	0.0003226	0.0008308	1.41e-05	AOI211X1
g2685	0.0005294	0.0002249	0.0008248	7.055e-05	XNOR2X1
g2699	0.000558	0.0002346	0.0008126	2.004e-05	NOR2BX1
g2676	0.0005827	0.0001714	0.0007742	2.004e-05	NOR2BX1
g2650	0.0003973	0.0003577	0.000768	1.299e-05	OAI21X1
g2688	0.0004882	0.0002014	0.0007602	7.055e-05	XNOR2X1

g2704	0.0002755	0.0004158	0.0007036	1.236e-05	NOR2XL
g2649	0.0005261	0.0001033	0.0006925	6.308e-05	XNOR2XL
g2660	0.0004555	0.0002183	0.0006921	1.833e-05	AOI22X1
g2666	0.0004432	0.0002244	0.0006806	1.299e-05	AOI21X1
g2681	0.0003435	0.0002987	0.0006772	3.499e-05	NAND2BX1
g2674	0.00053	0.000111	0.000661	2.004e-05	NOR2BX1
in1/g2	0.0004759	0.0001158	0.00066	6.826e-05	XOR2XL
g2680	0.0002554	0.0003658	0.0006562	3.499e-05	NAND2BX1
g2619	0.0003027	0.0003294	0.0006445	1.236e-05	NOR2XL
g2612	0.0003856	0.0002309	0.0006348	1.833e-05	AOI22X1
g2768	0.0004524	0.0001545	0.0006316	2.466e-05	AND2XL
g2621	0.0003784	0.0002341	0.0006304	1.791e-05	AOI22X1
g2	0.0004801	8.481e-05	0.000628	6.308e-05	XNOR2XL
g2806	0.0004731	9.055e-05	0.0006268	6.308e-05	XNOR2XL
g2602	0.0003902	0.000209	0.0006171	1.791e-05	AOI22X1
g2693	0.0004842	0.0001036	0.0006078	2.004e-05	NOR2BX1
g2695	0.0004896	9.771e-05	0.0006074	2.004e-05	NOR2BX1
g2772	0.0004561	0.0001231	0.0006038	2.466e-05	AND2XL
g2682	0.0003904	0.0001826	0.0005911	1.815e-05	AOI21X1
g2641	0.0004148	0.0001629	0.0005901	1.236e-05	NOR2XL
g2775	0.0004592	0.0001003	0.0005841	2.466e-05	AND2XL
g2774	0.00046	9.74e-05	0.000582	2.466e-05	AND2XL
g2675	0.0003438	0.0001957	0.0005745	3.499e-05	NAND2BX1
g2587	0.0004066	0.0001552	0.000574	1.22e-05	AOI21XL
g2777	0.0004657	7.71e-05	0.0005675	2.466e-05	AND2XL
g2626	0.000334	0.0002108	0.0005631	1.833e-05	AOI22X1
g2760	0.0004687	6.647e-05	0.0005599	2.466e-05	AND2XL
g2757	0.0004696	6.335e-05	0.0005576	2.466e-05	AND2XL
g2663	0.0003877	0.0001575	0.0005575	1.236e-05	NOR2XL
g2600	0.0003678	0.0001746	0.0005565	1.41e-05	AOI21X1
g2773	0.0004716	5.62e-05	0.0005525	2.466e-05	AND2XL
g2624	0.0002711	0.0002639	0.0005491	1.41e-05	AOI21X1
g2610	0.0003642	0.0001704	0.0005468	1.224e-05	AOI22XL
FE_OFC0_rst	0.0002848	0.0002443	0.0005421	1.301e-05	INVX1
g2659	0.000358	0.0001701	0.0005403	1.22e-05	AOI21XL
g2683	0.0002854	0.0002315	0.0005299	1.299e-05	AOI21X1
g2700	0.0002662	0.0002278	0.0005291	3.499e-05	NAND2BX1
g2614	0.0004077	9.724e-05	0.0005235	1.851e-05	AOI32X1
g2684	0.0002647	0.0002205	0.0005202	3.499e-05	NAND2BX1
g2689	0.0002573	0.000232	0.0005163	2.704e-05	MXI2XL
g2656	0.0003054	0.0001886	0.0005122	1.815e-05	AOI21X1
g2657	0.0003104	0.0001826	0.0005111	1.815e-05	AOI21X1
g2627	0.0003635	0.0001346	0.0005103	1.22e-05	AOI21XL
in1/g62	0.0003719	0.0001254	0.0005097	1.236e-05	NOR2XL
g2677	0.0003003	0.0001907	0.0005034	1.236e-05	NOR2XL
g2671	0.0003752	0.0001066	0.0004949	1.299e-05	AOI21X1
g2613	0.0003587	0.0001163	0.0004872	1.22e-05	AOI21XL
in1/g67	0.0002598	0.0002092	0.0004814	1.236e-05	NOR2XL
g2616	0.0003729	9.545e-05	0.0004807	1.236e-05	NOR2XL
g2591	0.000375	9.246e-05	0.0004798	1.236e-05	NOR2XL
g2637	0.0003599	0.0001044	0.0004765	1.22e-05	AOI21XL
g2710	0.0002759	0.0001881	0.0004763	1.236e-05	NOR2XL
g2711	0.0002462	0.0002152	0.0004737	1.236e-05	NOR2XL
g2662	0.0003622	8.774e-05	0.0004623	1.236e-05	NOR2XL
g2696	0.0002747	0.0001739	0.0004609	1.236e-05	NOR2XL
g2639	0.000346	0.0001018	0.0004602	1.236e-05	NOR2XL
g2635	0.0002396	0.0002053	0.0004578	1.299e-05	AOI21X1
g2713	0.0002745	0.0001692	0.0004561	1.236e-05	NOR2XL
g2648	0.0002336	0.0002037	0.0004503	1.299e-05	AOI21X1
g2628	0.0003393	8.104e-05	0.0004327	1.236e-05	NOR2XL
g2686	0.000258	0.0001424	0.0004275	2.704e-05	MXI2XL
g2690	0.0002558	0.000139	0.0004218	2.704e-05	MXI2XL
g2630	0.0002631	0.000145	0.0004211	1.301e-05	INVX1
g2712	0.000274	0.0001285	0.0004149	1.236e-05	NOR2XL
g2670	0.0002489	0.0001534	0.0004147	1.236e-05	NOR2XL
g2661	0.0002201	0.0001753	0.0004104	1.511e-05	NAND3X1
g2608	0.0002774	0.0001139	0.0004033	1.205e-05	AOI22XL
g2601	0.0002837	9.535e-05	0.0003911	1.205e-05	AOI22XL
g2706	0.0002746	0.0001027	0.0003896	1.236e-05	NOR2XL
g2609	0.0002702	0.0001067	0.000389	1.205e-05	AOI22XL
g2673	0.0001918	0.0001778	0.0003826	1.299e-05	AOI21X1
g2588	0.0002615	0.0001069	0.0003804	1.205e-05	AOI22XL
g2584	0.0002644	0.0001039	0.0003804	1.205e-05	AOI22XL
g2606	0.0002667	0.0001003	0.0003791	1.205e-05	AOI22XL
g2692	0.0002281	0.0001118	0.0003781	3.828e-05	OR2XL
g2607	0.0002654	9.705e-05	0.0003745	1.205e-05	AOI22XL
in1/g72	0.0002582	8.975e-05	0.0003726	2.466e-05	AND2XL
g2654	0.0002439	0.000116	0.0003722	1.236e-05	NOR2XL
g2604	0.0002637	8.639e-05	0.0003714	2.127e-05	AOI2BB1X1
g2691	0.0002149	0.0001005	0.0003536	3.828e-05	OR2XL
g2738	0.0001331	0.0002031	0.0003492	1.301e-05	INVX1

g2737	0.000154	0.0001817	0.0003488	1.301e-05	INVX1
g2708	0.0001256	0.0002129	0.0003477	9.289e-06	NAND2XL
in1/g69	0.0001963	0.0001348	0.0003442	1.301e-05	CLKINVX1
g2765	0.0002136	9.903e-05	0.0003373	2.466e-05	AND2XL
g2646	0.0002113	8.457e-05	0.0003308	3.499e-05	NAND2BX1
g2756	0.0002141	8.994e-05	0.0003287	2.466e-05	AND2XL
g2758	0.0002141	8.947e-05	0.0003283	2.466e-05	AND2XL
g2636	0.0002236	9.101e-05	0.0003276	1.299e-05	OAI21X1
g2762	0.0002145	8.382e-05	0.000323	2.466e-05	AND2XL
g2755	0.0002146	8.223e-05	0.0003215	2.466e-05	AND2XL
g2767	0.0002147	8.043e-05	0.0003198	2.466e-05	AND2XL
g2759	0.0002149	7.648e-05	0.0003161	2.466e-05	AND2XL
g2705	0.0002381	6.375e-05	0.0003142	1.236e-05	NOR2XL
g2754	0.0002152	7.277e-05	0.0003126	2.466e-05	AND2XL
g2769	0.0002153	6.973e-05	0.0003097	2.466e-05	AND2XL
g2715	0.0001183	0.0001805	0.0003081	9.289e-06	NAND2XL
g2707	0.0001795	9.021e-05	0.0003038	3.828e-05	OR2XL
g2766	0.0002156	6.538e-05	0.0003056	2.466e-05	AND2XL
g2719	0.0001545	0.0001378	0.0003053	1.301e-05	INVX1
g2770	0.0002156	6.491e-05	0.0003052	2.466e-05	AND2XL
g2653	0.0001604	0.0001332	0.0003029	9.289e-06	NAND2XL
g2776	0.0002159	6.128e-05	0.0003018	2.466e-05	AND2XL
g2615	0.0001995	6.668e-05	0.0003012	3.499e-05	NAND2BX1
g2763	0.0002161	5.647e-05	0.0002973	2.466e-05	AND2XL
g2701	0.0001985	7.605e-05	0.0002946	2.004e-05	NOR2BX1
g2764	0.0002163	5.328e-05	0.0002943	2.466e-05	AND2XL
g2771	0.0002165	5.114e-05	0.0002923	2.466e-05	AND2XL
g2721	0.0001564	0.0001109	0.0002804	1.301e-05	CLKINVX1
g2720	0.0001344	0.0001325	0.0002799	1.301e-05	INVX1
g2647	0.0001612	0.0001054	0.000279	1.236e-05	NOR2XL
g2716	9.719e-05	0.0001718	0.0002782	9.289e-06	NAND2XL
g2634	0.0001919	7.139e-05	0.0002756	1.236e-05	NOR2XL
g2618	0.0001993	6.286e-05	0.0002709	8.757e-06	INVXL
g2717	0.000138	0.0001027	0.0002678	2.717e-05	AND2BX1
g2703	0.0001094	0.0001155	0.0002599	3.499e-05	NAND2BX1
g2736	0.0001455	9.852e-05	0.0002571	1.301e-05	CLKINVX1
g2672	0.000178	6.305e-05	0.000254	1.299e-05	OAI21X1
g2697	0.0001251	8.628e-05	0.0002464	3.499e-05	NAND2BX1
g2652	0.0001276	8.377e-05	0.0002237	1.236e-05	NOR2XL
g2718	5.102e-05	0.0001591	0.0002194	9.289e-06	NAND2XL
g2709	0.0001178	8.927e-05	0.0002194	1.236e-05	NOR2XL
g2678	6.652e-05	0.0001418	0.0002177	9.289e-06	NAND2XL
g2714	0.0001157	7.361e-05	0.0002017	1.236e-05	NOR2XL
g2643	0.0001145	4.819e-05	0.0001839	2.127e-05	OAI2BB1X1
g2640	0.0001215	4.467e-05	0.0001785	1.236e-05	NOR2XL
g2761	9.175e-05	7.226e-05	0.0001733	9.289e-06	NAND2XL
g2702	5.125e-05	0.0001037	0.0001643	9.289e-06	NAND2XL
g2586	0.0001043	4.336e-05	0.0001598	1.22e-05	AOI21XL
g2658	3.632e-05	8.271e-05	0.000154	3.499e-05	NAND2BX1
g2698	5.106e-05	8.683e-05	0.0001472	9.289e-06	NAND2XL
g2669	8.828e-05	3.8e-05	0.0001386	1.236e-05	NOR2XL
g2592	9.438e-05	3.459e-05	0.0001377	8.728e-06	OAI21XL
g2631	6.946e-05	4.833e-05	0.0001283	1.046e-05	NAND4XL
g2668	5.367e-05	4.831e-05	0.0001113	9.289e-06	NAND2XL
g2667	2.884e-05	4.315e-05	8.245e-05	1.046e-05	NAND4XL
g2694	4.871e-05	2.369e-05	8.169e-05	9.289e-06	NAND2XL
g2642	3.043e-05	2.405e-05	6.494e-05	1.046e-05	NAND4XL
g2655	2.729e-05	1.198e-05	5.229e-05	1.301e-05	INVX1

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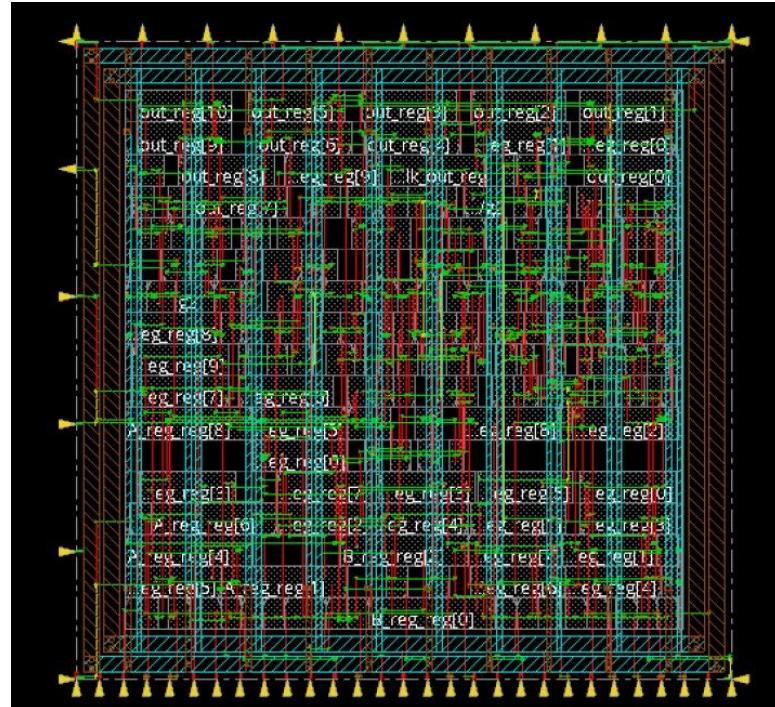
Total ( 202 of 202 )	0.2786	0.03704	0.3249	0.009218
Total Capacitance	1.305e-12 F			
Power Density	*** No Die Area ***			

### Power Analysis:

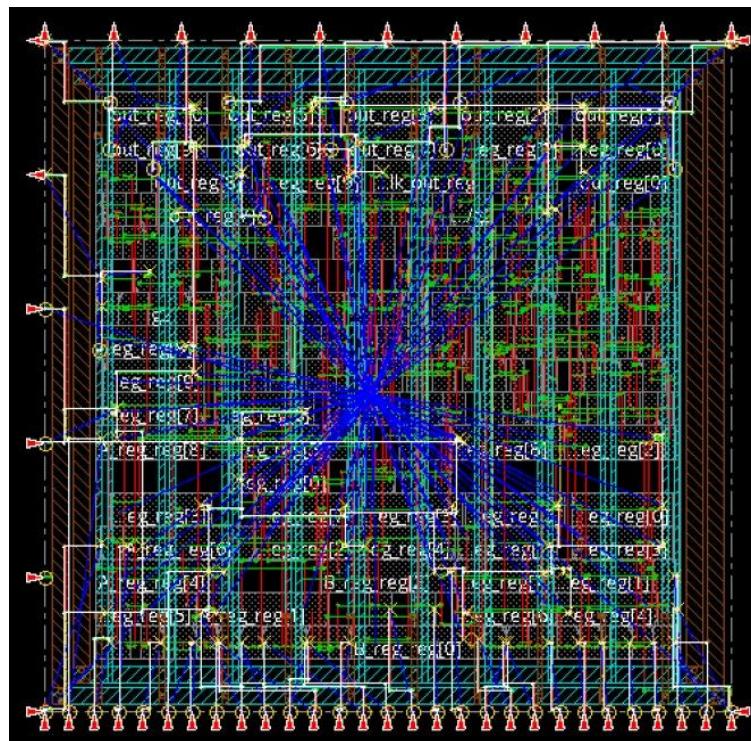
- Total Internal Power: 0.2786 mW
- Total switching power: 0.03704 mW
- Total leakage Power: 0.009218 mW
- Total Power Dissipated: 0.3249 mW

- Layout (Showing Fly Lines)

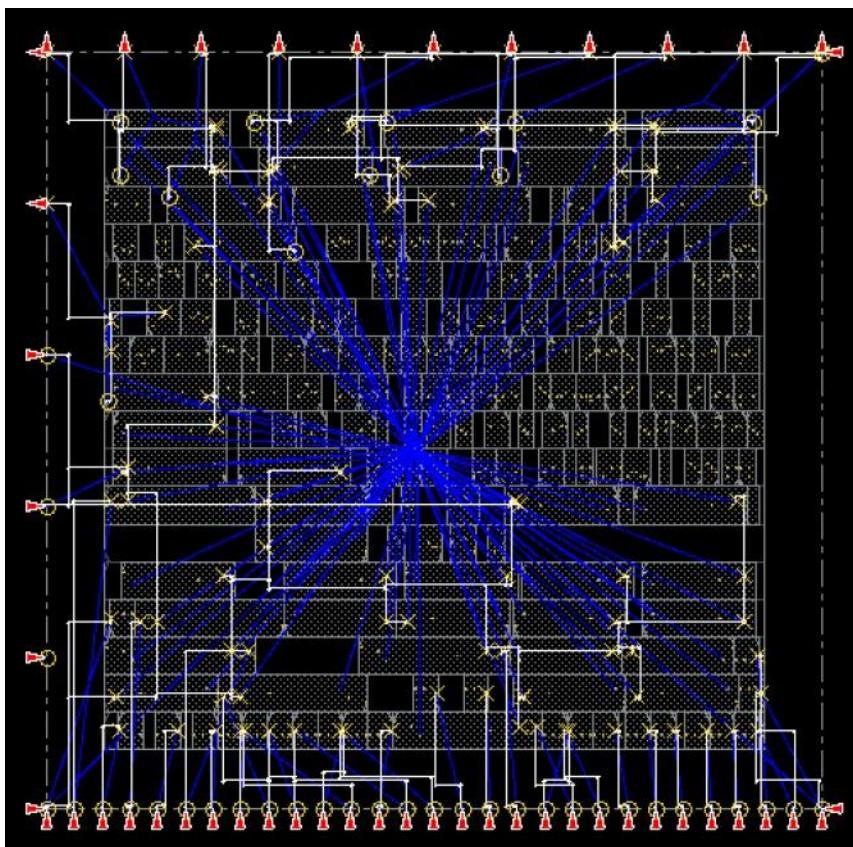
Without any fly-lines, after design is Placed:



With Fly Lines after Design is Placed:



Flylines with only instances showing:



# Post CTS

- Timing Effect

```

2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:08:55 2022
5 # Design: rtl module
6 # Command: optDesign -postCTS -hold
7 #####
8
9 -----
10    optDesign Final Summary
11 -----
12
13 +-----+-----+-----+
14 |   Setup mode | all | reg2reg | default |
15 +-----+-----+-----+
16 |       WNS (ns): 0.226 | 0.492 | 0.226 |
17 |       TNS (ns): 0.000 | 0.000 | 0.000 |
18 | Violating Paths: 0 | 0 | 0 |
19 | All Paths: 146 | 55 | 102 |
20 +-----+-----+-----+
21
22 +-----+-----+-----+
23 |           Real          |      Total      |
24 | DRVs      | Nr nets(terms) | Worst Vio | Nr nets(terms) |
25 |           |               |           |               |
26 +-----+-----+-----+
27 | max_cap   | 0 (0)     | 0.000  | 0 (0)     |
28 | max_tran  | 0 (0)     | 0.000  | 0 (0)     |
29 | max_fanout| 0 (0)     | 0      | 0 (0)     |
30 | max_length| 0 (0)     | 0      | 0 (0)     |
31 +-----+-----+-----+
32
33 Density: 95.048%
34 Routing Overflow: 0.00% H and 0.00% V

```

```

1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:08:55 2022
5 # Design: rtl_module
6 # Command: optDesign -postCTS -hold
7 #####
8 Path 1: MET Setup Check with Pin B_reg_reg[2]/CK
9 Endpoint: B_reg_reg[2]/D (v) checked with leading edge of 'clk'
10 Beginpoint: B[2] (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time      0.500
14 - Setup                      2.074
15 + Phase Shift                 4.000
16 - Uncertainty                0.500
17 = Required Time              1.926
18 - Arrival Time               1.700
19 = Slack Time                 0.226
20   Clock Rise Edge            0.000
21     + Input Delay             1.200
22     + Network Insertion Delay 0.500
23     = Beginpoint Arrival Time 1.700

```

```

24 Timing Path:
25 +-----+-----+-----+-----+
26 |   Pin    | Edge | Net | Cell | Delay | Arrival | Required |
27 |           |     |   |     |       | Time   | Time    |
28 |           +---+---+---+-----+
29 | B[2]     | v   | B[2] |      |       | 1.700 | 1.926 |
30 | B_reg_reg[2]/D | v   | B[2] | SDFFFTRX1 | 0.000 | 1.700 | 1.926 |
31 +-----+-----+-----+-----+
32 Clock Rise Edge              0.000
33 + Source Insertion Delay     0.022
34 = Beginpoint Arrival Time   0.022
35 Other End Path:
36 +-----+-----+-----+-----+
37 |   Pin    | Edge | Net | Cell | Delay | Arrival | Required |
38 |           |     |   |     |       | Time   | Time    |
39 |           +---+---+---+-----+
40 | clk      | ^   | clk  |      |       | 0.022 | -0.204 |
41 | CTS_cdb_buf_00009/A | ^   | clk  | CLKBUFX2 | 0.000 | 0.022 | -0.204 |
42 | CTS_cdb_buf_00009/Y | ^   | CTS_2 | CLKBUFX2 | 0.091 | 0.113 | -0.113 |
43 | CTS_cdb_buf_00008/A | ^   | CTS_2 | CLKBUFX2 | 0.000 | 0.113 | -0.113 |
44 | CTS_cdb_buf_00008/Y | ^   | CTS_1 | CLKBUFX2 | 0.387 | 0.499 | 0.273 |
45 | B_reg_reg[2]/CK | ^   | CTS_1 | SDFFFTRX1 | 0.000 | 0.500 | 0.274 |
46 +-----+-----+-----+

```

```

2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:08:55 2022
5 # Design: rtl module
6 # Command: optDesign -postCTS -hold
7 #####
8
9 -----
10      optDesign Final Summary
11 -----
12
13 +-----+
14 | Hold mode | all | reg2reg | default |
15 +-----+
16 | WNS (ns): | -1.026 | -0.104 | -1.026 |
17 | TNS (ns): | -26.579 | -0.667 | -25.911 |
18 | Violating Paths:| 56 | 11 | 45 |
19 | All Paths:| 146 | 55 | 102 |
20 +-----+
21
22 +-----+
23 | | Real | Total |
24 | DRVs | +-----+ | +-----+
25 | | Nr nets(terms) | Worst Vio | Nr nets(terms) |
26 +-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 +-----+
32
33 Density: 95.048%
34 Routing Overflow: 0.00% H and 0.00% V

```

```

1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:08:55 2022
5 # Design: rtl module
6 # Command: optDesign -postCTS -hold
7 #####
8 Path 1: VIOLATED Hold Check with Pin A_reg_reg[5]/CK
9 Endpoint: A_reg_reg[5]/SE (v) checked with leading edge of 'clk'
10 Beginpoint: scan_en (v) triggered by leading edge of '@'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time 0.481
14 + Hold 0.045
15 + Phase Shift 0.000
16 + Uncertainty 0.500
17 = Required Time 1.026
18 Arrival Time 0.000
19 Slack Time -1.026
20     Clock Rise Edge 0.000
21     + Input Delay 0.000
22     = Beginpoint Arrival Time 0.000

```

```

23 Timing Path:
24 +-----+
25 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
26 | | | | | | Time | Time |
27 +-----+
28 | scan_en | v | scan_en | | 0.000 | 1.026 |
29 | A_reg_reg[5]/SE | v | scan_en | SDFFQX1 | 0.000 | 0.000 | 1.026 |
30 +-----+
31 Clock Rise Edge 0.000
32 + Source Insertion Delay 0.022
33 = Beginpoint Arrival Time 0.022
34 Other End Path:
35 +-----+
36 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
37 | | | | | | Time | Time |
38 +-----+
39 | clk | ^ | clk | CLKBUFX2 | 0.000 | 0.022 | -1.004 |
40 | CTS_cdb_buf_00009/A | ^ | clk | CLKBUFX2 | 0.000 | 0.022 | -1.004 |
41 | CTS_cdb_buf_00009/Y | ^ | CTS_2 | CLKBUFX2 | 0.091 | 0.113 | -0.913 |
42 | CTS_cdb_buf_00008/A | ^ | CTS_2 | CLKBUFX2 | 0.000 | 0.113 | -0.913 |
43 | CTS_cdb_buf_00008/Y | ^ | CTS_1 | CLKBUFX2 | 0.368 | 0.480 | -0.545 |
44 | A_reg_reg[5]/CK | ^ | CTS_1 | SDFFQX1 | 0.001 | 0.481 | -0.545 |
45 +-----+

```

### Setup Slack: 0.226ns (Effect mentioned before)

**Hold Slack : -1.026ns** Although the slack has improved it is still negative. Thus our design cannot run for utilization of 0.8

- Area

```

10 =====
11 General Design Information
12 =====
13 Design Status: Routed
14 Design Name: rtl_module
15 # Instances: 242
16 # Hard Macros: 0
17 # Std Cells: 242
18 -----
19 Standard Cells in Netlist
20 -----
21 | | | Cell Type | Instance Count | Area (um^2)
22 | | | OAI2BB1X1 | 2 | 10.5966
23 | | | DLY4X1 | 2 | 52.9830
24 | | | CLKBUFX2 | 16 | 72.6624
25 | | | OR2XL | 3 | 13.6242
26 | | | BUFX2 | 1 | 4.5414
27 | | | OAI222XL | 1 | 8.3259
28 | | | AND2X1 | 1 | 4.5414
29 | | | OAI211X1 | 3 | 15.8949
30 | | | SDFFQX1 | 36 | 735.7068
31 | | | XNOR2X1 | 3 | 24.9777
32 | | | AND2XL | 23 | 104.4522
33 | | | XOR2XL | 1 | 8.3259
34 | | | OAI21X1 | 11 | 49.9554
35 | | | CLKINVX1 | 2 | 4.5414
36 | | | AOI211X1 | 1 | 5.2983
37 | | | NAND2BX1 | 10 | 45.4140
38 | | | SDFFQXL | 1 | 20.4363
39 | | | XNOR2XL | 3 | 24.9777
40 | | | NAND3X1 | 1 | 4.5414
41 | | | NAND2XL | 11 | 33.3036
42 | | | NOR2BX1 | 8 | 36.3312
43 | | | CLKAND2X2 | 1 | 5.2983
44 | | | OAI22X1 | 3 | 18.1656
45 | | | OAI21XL | 1 | 4.5414
46 | | | AOI21X1 | 7 | 31.7898
47 | | | INVXL | 2 | 4.5414
48 | | | NOR3X1 | 1 | 4.5414
49 | | | NAND4X1 | 1 | 6.0552
50 | | | INVX1 | 7 | 15.8949
51 | | | SDFFTTRX1 | 6 | 163.4904
52 | | | OAI22XL | 7 | 42.3864
53 | | | NOR2XL | 28 | 84.7728
54 | | | AOI22X1 | 3 | 18.1656
55 | | | AOI21XL | 6 | 27.2484
56 | | | AOI32X1 | 1 | 6.8121
57 | | | DLY1X1 | 22 | 183.1698
58 | | | NAND4XL | 3 | 15.8949
59 | | | MXI2XL | 3 | 18.1656
60 # Pads: 0
61 # Net: 288
62 # Special Net: 2

```

```

3481 =====
3482 Floorplan/Placement Information
3483 =====
3484 Total area of Standard cells: 1932.366 um^2
3485 Total area of Standard cells(Subtracting Physical Cells): 1932.366 um^2
3486 Total area of Macros: 0.000 um^2
3487 Total area of Blockages: 0.000 um^2
3488 Total area of Pad cells: 0.000 um^2
3489 Total area of Core: 2033.033 um^2
3490 Total area of Chip: 2831.311 um^2
3491 Effective Utilization: 9.5048e-01
3492 Number of Cell Rows: 17
3493 % Pure Gate Density #1 (Subtracting BLOCKAGES): 95.048%
3494 % Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 95.048%
3495 % Pure Gate Density #3 (Subtracting MACROS): 95.048%
3496 % Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 95.048%
3497 % Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 95.048%
3498 % Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 95.048%
3499 % Core Density (Counting Std Cells and MACROs): 95.048%
3500 % Core Density #2(Subtracting Physical Cells): 95.048%
3501 % Chip Density (Counting Std Cells and MACROs and IOs): 68.250%
3502 % Chip Density #2(Subtracting Physical Cells): 68.250%
3503 # Macros within 5 sites of IO pad: No
3504 Macro halo defined?: No
3505
3506 =====
3507 Wire Length Distribution
3508 =====
3509 Total Metal1 wire length: 0.0000 um |
3510 Total Metal2 wire length: 2456.6950 um
3511 Total Metal3 wire length: 1442.2050 um
3512 Total Metal4 wire length: 318.0150 um
3513 Total Metal5 wire length: 201.6950 um
3514 Total Metal6 wire length: 0.0000 um
3515 Total Metal7 wire length: 0.0000 um
3516 Total Metal8 wire length: 0.0000 um
3517 Total Metal9 wire length: 0.0000 um
3518 Total wire length: 4418.6100 um
3519 Average wire length/net: 15.3424 um
3520 Area of Power Net Distribution:
3521
3522 Area of Power Net Distribution
3523 =====
3524 Layer Name Area of Power Net Routable Area Percentage
3525 Metal1 0.0000 2033.0334 0.0000%
3526 Metal2 0.0000 2033.0334 0.0000%
3527 Metal3 0.0000 2033.0334 0.0000%
3528 Metal4 0.0000 2033.0334 0.0000%
3529 Metal5 0.0000 2033.0334 0.0000%
3530 Metal6 0.0000 2033.0334 0.0000%
3531 Metal7 0.0000 2033.0334 0.0000%
3532 Metal8 299.2820 2033.0334 14.7210%
3533 Metal9 190.7170 2033.0334 9.3809% For more information click here
3534

```

**Area Analysis:** The total number of instances have increased from 202 to 242 post the CTS stage as compared to post placement stage and no macros have been added. The total area has increased from 1622.794 um square to 1932.366 um square. Also the effective utilization has increased from 0.7982 to 0.9504 . We observe that the increase in area is mainly due to addition of Buffers and delay cells such as CLKBUFX2 and DLY1X1 which have been added by the tool in order to handle or fix the timing violations. Total metal wire length increases by approximately 1100 um since an extra metal-5 layer has been added.

## ● Power

```

*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile ./PostCTSPowerRPT/rtl_module_post_cts.rpt -rail_analysis_format VS
*
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
CTS_cdb_buf_00008	0.00358	0.02056	0.02418	4.129e-05	CLKBUFX2
B_reg_reg[2]	0.006211	0.0005352	0.006912	0.0001662	SDFFTRX1
B_reg_reg[0]	0.006242	0.0005035	0.006912	0.0001662	SDFFTRX1
out_reg[1]	0.006129	0.0004075	0.006672	0.0001363	SDFFQX1
out_reg[2]	0.006067	0.0004208	0.006624	0.0001363	SDFFQX1
A_reg_reg[4]	0.005817	0.0005627	0.006546	0.0001662	SDFFTRX1
A_reg_reg[1]	0.005776	0.0004654	0.006408	0.0001662	SDFFTRX1
A_reg_reg[6]	0.005821	0.0003498	0.006337	0.0001662	SDFFTRX1
out_reg[4]	0.005801	0.0001993	0.006136	0.0001363	SDFFQX1
out_reg[5]	0.005617	0.0003585	0.006112	0.0001363	SDFFQX1
out_reg[3]	0.005725	0.0001973	0.006059	0.0001363	SDFFQX1
out_reg[0]	0.005595	0.000306	0.006037	0.0001363	SDFFQX1
out_reg[9]	0.005438	0.0003826	0.005957	0.0001363	SDFFQX1
in1/count_reg_reg[0]	0.005574	0.0002093	0.00592	0.0001363	SDFFQX1
in1/count_reg_reg[1]	0.005481	0.0003001	0.005917	0.0001363	SDFFQX1
out_reg[8]	0.005487	0.0002279	0.005851	0.0001363	SDFFQX1
out_reg[6]	0.005514	0.0001599	0.00581	0.0001363	SDFFQX1
in1/clk_out_reg	0.005371	0.0002541	0.005762	0.0001363	SDFFQX1
out_reg[7]	0.005367	0.0002546	0.005758	0.0001363	SDFFQX1
B_reg_reg[9]	0.005209	0.0003617	0.005707	0.0001363	SDFFQX1
A_reg_reg[8]	0.00527	0.0002564	0.005692	0.0001662	SDFFTRX1
B_reg_reg[1]	0.004997	0.0003698	0.005503	0.0001363	SDFFQX1
C_reg_reg[4]	0.00492	0.0003927	0.005449	0.0001363	SDFFQX1
A_reg_reg[9]	0.004933	0.0003797	0.005449	0.0001363	SDFFQX1
C_reg_reg[6]	0.004899	0.0004034	0.005438	0.0001363	SDFFQX1
B_reg_reg[6]	0.004941	0.0003597	0.005437	0.0001363	SDFFQX1
B_reg_reg[7]	0.004934	0.0003635	0.005434	0.0001363	SDFFQX1
C_reg_reg[3]	0.004929	0.0003658	0.005431	0.0001363	SDFFQX1
A_reg_reg[2]	0.004933	0.000323	0.005392	0.0001363	SDFFQX1
B_reg_reg[5]	0.00492	0.0003329	0.005389	0.0001363	SDFFQX1
C_reg_reg[2]	0.004935	0.0002831	0.005354	0.0001363	SDFFQX1
B_reg_reg[8]	0.004943	0.0002737	0.005353	0.0001363	SDFFQX1
B_reg_reg[3]	0.004936	0.0002778	0.00535	0.0001363	SDFFQX1
A_reg_reg[0]	0.004897	0.0003151	0.005348	0.0001363	SDFFQX1
C_reg_reg[1]	0.004935	0.0002765	0.005348	0.0001363	SDFFQX1
A_reg_reg[7]	0.004935	0.0002617	0.005333	0.0001363	SDFFQX1
A_reg_reg[5]	0.004802	0.000356	0.005294	0.0001363	SDFFQX1
B_reg_reg[4]	0.004888	0.0002588	0.005283	0.0001363	SDFFQX1
C_reg_reg[0]	0.004933	0.0002091	0.005278	0.0001363	SDFFQX1
C_reg_reg[7]	0.004848	0.0002407	0.005225	0.0001363	SDFFQX1
A_reg_reg[3]	0.004734	0.0003445	0.005215	0.0001363	SDFFQX1
C_reg_reg[5]	0.004734	0.0002122	0.005082	0.0001363	SDFFQX1
out_reg[10]	0.004812	3.492e-05	0.004977	0.0001296	SDFFQXL
C_reg_reg[8]	0.00448	0.0001885	0.004804	0.0001363	SDFFQX1
CTS_cdb_buf_00009	0.003589	0.0005735	0.004204	4.129e-05	CLKBUFX2
FE_OFCl_rst	0.0003848	0.001335	0.001761	4.129e-05	BUFX2
FE_PHC19_scan_en	0.0001439	0.001511	0.001696	4.129e-05	CLKBUFX2
g2617	0.0003472	0.001107	0.00147	1.612e-05	NAND4X1
g2645	0.001001	0.0002386	0.00126	2.034e-05	NOR3X1
FE_PHC16_out_2	0.0007716	0.000426	0.001252	5.435e-05	DLY1X1
FE_PHC8_out_1	0.0007958	0.0003043	0.001154	5.435e-05	DLY1X1
g2638	0.0005734	0.0004303	0.001022	1.815e-05	AOI21X1
FE_PHC14_out_0	0.0006335	0.0002518	0.0009396	5.435e-05	DLY1X1
FE_PHC12_out_5	0.0006302	0.0002393	0.0009238	5.435e-05	DLY1X1
g2687	0.0005823	0.0002654	0.0009182	7.055e-05	XNOR2X1
FE_PHC13_out_9	0.0005768	0.0002846	0.0009157	5.435e-05	DLY1X1
g2633	0.0007331	0.0001565	0.0009096	2.004e-05	NOR2BX1
g2679	0.0004855	0.0003932	0.0008988	2.004e-05	NOR2BX1
in1/FE_PHC33_count_reg_0	0.0005747	0.0002619	0.000891	5.435e-05	DLY1X1
g2629	0.0004734	0.0003983	0.0008846	1.299e-05	OA121X1
FE_PHC5_out_4	0.000686	0.0001404	0.0008808	5.435e-05	DLY1X1
g2644	0.0006466	0.0001992	0.0008657	1.995e-05	AOI211X1
g2664	0.0006024	0.0002246	0.0008449	1.791e-05	OA122X1
in1/g72	0.0007018	9.25e-05	0.0008393	4.5e-05	CLKAND2X2
g2632	0.0005517	0.0002639	0.0008337	1.815e-05	AOI21X1
FE_PHC7_out_8	0.0005895	0.0001899	0.0008337	5.435e-05	DLY1X1
g2623	0.0004939	0.000324	0.000832	1.41e-05	OA1211X1

FE_PHC11_out_7	0.0005539	0.0001983	0.0008065	5.435e-05	DLY1X1
g2603	0.0005157	0.0002774	0.0008061	1.299e-05	OAI21X1
FE_PHC28_out_3	0.0006635	8.622e-05	0.0008041	5.435e-05	DLY1X1
g2676	0.0005824	0.0001712	0.0007736	2.004e-05	NOR2BX1
g2685	0.0004896	0.0002079	0.000768	7.055e-05	XNOR2X1
g2650	0.0003973	0.0003516	0.000762	1.299e-05	OAI21X1
g2665	0.0006026	0.0001341	0.0007549	1.815e-05	AOI21X1
g2688	0.0004835	0.0001983	0.0007523	7.055e-05	XNOR2X1
g2651	0.0004988	0.0002349	0.0007519	1.815e-05	AOI21X1
FE_PHC6_out_6	0.0005941	0.0001005	0.000749	5.435e-05	DLY1X1
FE_PHC26_A_reg_9	0.0004654	0.0002272	0.0007339	4.129e-05	CLKBUFX2
g2704	0.0002754	0.0004151	0.0007028	1.236e-05	NOR2XL
g2699	0.000482	0.0002001	0.0007021	2.004e-05	NOR2BX1
g2649	0.0005309	0.0001004	0.0006944	6.308e-05	XNOR2XL
g2681	0.0003434	0.0003018	0.0006802	3.499e-05	NAND2BX1
g2666	0.0004429	0.0002239	0.0006798	1.299e-05	OAI21X1
FE_PHC27_n_1	0.0004594	0.000172	0.0006727	4.129e-05	CLKBUFX2
FE_PHC22_A_reg_2	0.0004657	0.000157	0.0006639	4.129e-05	CLKBUFX2
g2674	0.0005299	0.0001109	0.0006608	2.004e-05	NOR2BX1
g2680	0.0002586	0.0003671	0.0006607	3.499e-05	NAND2BX1
in1/g2	0.0004756	0.0001153	0.0006591	6.826e-05	XOR2XL
in1/FE_PHC29_out1	0.0005288	6.9e-05	0.0006521	5.435e-05	DLY1X1
g2619	0.0003026	0.0003297	0.0006447	1.236e-05	NOR2XL
g2806	0.0004811	9.133e-05	0.0006355	6.308e-05	XNOR2XL
FE_PHC21_C_reg_4	0.0004652	0.000128	0.0006345	4.129e-05	CLKBUFX2
FE_PHC25_n_0	0.0004455	0.0001473	0.0006341	4.129e-05	CLKBUFX2
FE_PHC20_C_reg_3	0.0004671	0.0001245	0.0006328	4.129e-05	CLKBUFX2
FE_PHC23_A_reg_5	0.0004411	0.0001484	0.0006309	4.129e-05	CLKBUFX2
g2768	0.0004529	0.0001502	0.0006278	2.466e-05	AND2XL
g2	0.0004802	8.441e-05	0.0006277	6.308e-05	XNOR2XL
FE_PHC24_n_4	0.0004617	0.0001166	0.0006196	4.129e-05	CLKBUFX2
g2693	0.000491	0.000105	0.000616	2.004e-05	NOR2BX1
g2621	0.0003725	0.0002239	0.0006143	1.791e-05	OAI22X1
g2626	0.0003629	0.0002314	0.0006126	1.833e-05	AOI22X1
g2660	0.0003946	0.0001883	0.0006012	1.833e-05	AOI22X1
g2772	0.0004565	0.0001199	0.000601	2.466e-05	AND2XL
g2602	0.0003851	0.0001938	0.0005968	1.791e-05	OAI22X1
FE_PHC15_n_5	0.0004198	0.0001211	0.0005952	5.435e-05	DLY1X1
FE_PHC3_C_reg_6	0.0004621	8.616e-05	0.0005896	4.129e-05	CLKBUFX2
g2682	0.0003903	0.0001779	0.0005863	1.815e-05	AOI21X1
FE_PHC17_B_reg_7	0.0004709	7.139e-05	0.0005836	4.129e-05	CLKBUFX2
FE_PHC18_B_reg_5	0.0004643	7.756e-05	0.0005832	4.129e-05	CLKBUFX2
g2774	0.0004606	9.51e-05	0.0005804	2.466e-05	AND2XL
g2775	0.0004608	9.451e-05	0.0005799	2.466e-05	AND2XL
g2587	0.0004099	0.0001569	0.0005791	1.22e-05	AOI21XL
g2675	0.0003443	0.0001949	0.0005742	3.499e-05	NAND2BX1
g2777	0.0004671	7.227e-05	0.000564	2.466e-05	AND2XL
FE_PHC4_B_reg_1	0.0004339	8.51e-05	0.0005603	4.129e-05	CLKBUFX2
g2760	0.0004688	6.614e-05	0.0005596	2.466e-05	AND2XL
g2612	0.0003359	0.0002035	0.0005577	1.833e-05	AOI22X1
g2757	0.0004697	6.295e-05	0.0005573	2.466e-05	AND2XL
g2600	0.0003677	0.0001736	0.0005554	1.41e-05	OAI21X1
FE_PHC10_n_3	0.0004287	7.176e-05	0.0005549	5.435e-05	DLY1X1
g2773	0.0004717	5.601e-05	0.0005523	2.466e-05	AND2XL
g2695	0.0004412	8.956e-05	0.0005508	2.004e-05	NOR2BX1
g2610	0.0003653	0.0001698	0.0005474	1.224e-05	OAI22XL
in1/FE_PHC34_B_reg_6	0.0004433	5.602e-05	0.0005433	5.435e-05	DLY1X1
FE_PHC35_C_reg_1	0.0004314	5.609e-05	0.0005418	5.435e-05	DLY1X1
FE_OFC0_rst	0.0002851	0.0002427	0.0005408	1.301e-05	INVX1
FE_PHC36_B_reg_3	0.0004299	5.58e-05	0.00054	5.435e-05	DLY1X1
g2624	0.0002711	0.0002541	0.0005393	1.41e-05	OAI21X1
FE_PHC32_C_reg_0	0.0004293	5.256e-05	0.0005363	5.435e-05	DLY1X1
g2659	0.00035	0.0001661	0.0005283	1.22e-05	AOI21XL
g2700	0.0002658	0.000227	0.0005278	3.499e-05	NAND2BX1
FE_PHC2_A_reg_3	0.0004093	7.574e-05	0.0005263	4.129e-05	CLKBUFX2
g2683	0.0002828	0.0002289	0.0005247	1.299e-05	OAI21X1
FE_PHC37_A_reg_0	0.000416	5.385e-05	0.0005242	5.435e-05	DLY1X1
g2684	0.0002644	0.0002179	0.0005172	3.499e-05	NAND2BX1
g2641	0.0003599	0.0001439	0.0005162	1.236e-05	NOR2XL
g2627	0.0003693	0.0001341	0.0005156	1.22e-05	AOI21XL
g2689	0.0002572	0.0002289	0.0005132	2.704e-05	MXI2XL
FE_PHC38_C_reg_7	0.000406	5.252e-05	0.0005129	5.435e-05	DLY1X1
g2656	0.0003057	0.0001885	0.0005124	1.815e-05	AOI21X1
g2657	0.0003095	0.0001828	0.0005105	1.815e-05	AOI21X1
in1/g62	0.0003712	0.0001249	0.0005085	1.236e-05	NOR2XL
g2635	0.000264	0.0002301	0.0005071	1.299e-05	OAI21X1
g2663	0.0003513	0.0001422	0.0005058	1.236e-05	NOR2XL
g2677	0.0003003	0.0001903	0.000503	1.236e-05	NOR2XL
g2613	0.0003719	0.000118	0.0005021	1.22e-05	AOI21XL
g2671	0.000375	0.0001104	0.0004984	1.299e-05	OAI21X1
g2614	0.0003867	9.181e-05	0.000497	1.851e-05	AOI32X1

g2637	0.0003709	0.0001065	0.0004897	1.22e-05	AOI2XL
in1/g67	0.0002596	0.0002088	0.0004807	1.236e-05	NOR2XL
g2648	0.0002495	0.0002159	0.0004783	1.299e-05	OAI21X1
g2591	0.0003726	9.135e-05	0.0004763	1.236e-05	NOR2XL
g2711	0.0002461	0.0002146	0.000473	1.236e-05	NOR2XL
g2710	0.0002743	0.000186	0.0004727	1.236e-05	NOR2XL
FE_PHC31_DFT_sdi_1	0.0003346	1.583e-05	0.0004696	0.0001191	DLY4X1
FE_PHC30_DFT_sdi_2	0.0003346	1.524e-05	0.000469	0.0001191	DLY4X1
g2696	0.0002746	0.0001729	0.0004599	1.236e-05	NOR2XL
g2662	0.0003599	8.692e-05	0.0004592	1.236e-05	NOR2XL
g2713	0.0002754	0.0001691	0.0004569	1.236e-05	NOR2XL
g2639	0.0003438	0.0001002	0.0004564	1.236e-05	NOR2XL
g2616	0.0003408	8.678e-05	0.0004399	1.236e-05	NOR2XL
g2628	0.0003418	8.195e-05	0.0004361	1.236e-05	NOR2XL
g2690	0.000258	0.0001405	0.0004255	2.704e-05	MXI2XL
g2608	0.0002908	0.0001183	0.0004212	1.205e-05	OAI22XL
g2630	0.0002631	0.0001411	0.0004172	1.301e-05	INVX1
g2670	0.0002491	0.0001532	0.0004147	1.236e-05	NOR2XL
g2712	0.0002739	0.0001283	0.0004146	1.236e-05	NOR2XL
g2686	0.0002405	0.0001424	0.0004099	2.704e-05	MXI2XL
g2588	0.0002767	0.0001118	0.0004006	1.205e-05	OAI22XL
FE_PHC9_n_2	0.0002968	4.173e-05	0.0003929	5.435e-05	DLY1X1
FE_PHC39_C_reg_8	0.0002986	3.859e-05	0.0003915	5.435e-05	DLY1X1
g2706	0.0002745	0.0001024	0.0003893	1.236e-05	NOR2XL
g2607	0.0002743	9.756e-05	0.0003839	1.205e-05	OAI22XL
g2584	0.0002673	0.0001038	0.0003831	1.205e-05	OAI22XL
g2609	0.0002688	0.0001022	0.0003831	1.205e-05	OAI22XL
g2604	0.0002686	8.744e-05	0.0003773	2.127e-05	OAI2BB1X1
g2692	0.0002259	0.00011	0.0003741	3.828e-05	OR2XL
g2691	0.0002284	0.000106	0.0003727	3.828e-05	OR2XL
g2606	0.0002588	9.631e-05	0.0003671	1.205e-05	OAI22XL
g2661	0.0001953	0.0001555	0.000366	1.511e-05	NAND3X1
g2601	0.0002659	8.43e-05	0.0003623	1.205e-05	OAI22XL
g2654	0.0002343	0.0001099	0.0003566	1.236e-05	NOR2XL
g2673	0.0001796	0.0001619	0.0003545	1.299e-05	OAI21X1
g2738	0.0001331	0.0002035	0.0003496	1.301e-05	INVX1
g2708	0.0001252	0.0002119	0.0003464	9.289e-06	NAND2XL
g2737	0.0001487	0.0001751	0.0003369	1.301e-05	INVX1
g2765	0.0002137	9.674e-05	0.0003351	2.466e-05	AND2XL
g2758	0.0002142	8.869e-05	0.0003275	2.466e-05	AND2XL
g2756	0.0002142	8.845e-05	0.0003273	2.466e-05	AND2XL
g2720	0.0001572	0.0001526	0.0003228	1.301e-05	INVX1
g2762	0.0002145	8.349e-05	0.0003226	2.466e-05	AND2XL
g2755	0.0002146	8.137e-05	0.0003207	2.466e-05	AND2XL
g2636	0.0002179	8.927e-05	0.0003202	1.299e-05	OAI21X1
g2767	0.0002148	7.878e-05	0.0003182	2.466e-05	AND2XL
g2759	0.0002149	7.605e-05	0.0003157	2.466e-05	AND2XL
g2646	0.0002022	7.84e-05	0.0003156	3.499e-05	NAND2BX1
g2754	0.0002152	7.144e-05	0.0003113	2.466e-05	AND2XL
g2705	0.0002379	6.096e-05	0.0003112	1.236e-05	NOR2XL
g2769	0.0002153	6.98e-05	0.0003098	2.466e-05	AND2XL
g2701	0.0002087	7.98e-05	0.0003085	2.004e-05	NOR2BX1
g2766	0.0002156	6.509e-05	0.0003054	2.466e-05	AND2XL
g2719	0.0001544	0.0001376	0.0003051	1.301e-05	INVX1
g2770	0.0002156	6.454e-05	0.0003048	2.466e-05	AND2XL
g2715	0.0001183	0.0001762	0.0003038	9.289e-06	NAND2XL
g2653	0.0001603	0.0001329	0.0003026	9.289e-06	NAND2XL
g2776	0.0002158	6.148e-05	0.000302	2.466e-05	AND2XL
g2763	0.000216	5.808e-05	0.0002988	2.466e-05	AND2XL
g2615	0.0001975	6.598e-05	0.0002984	3.499e-05	NAND2BX1
g2707	0.0001699	8.549e-05	0.0002936	3.828e-05	OR2XL
g2771	0.0002164	5.111e-05	0.0002922	2.466e-05	AND2XL
g2764	0.0002165	5.108e-05	0.0002922	2.466e-05	AND2XL
in1/g69	0.0001242	0.0001509	0.0002838	8.757e-06	INVXL
g2721	0.0001576	0.0001104	0.0002809	1.301e-05	CLKINVX1
g2647	0.0001616	0.0001054	0.0002794	1.236e-05	NOR2XL
g2716	9.712e-05	0.000171	0.0002774	9.289e-06	NAND2XL
g2634	0.0001918	7.132e-05	0.0002755	1.236e-05	NOR2XL
g2618	0.0001993	6.276e-05	0.0002708	8.757e-06	INVXL
g2717	0.0001379	0.0001024	0.0002675	2.717e-05	AND2X1
g2703	0.0001132	0.000118	0.0002662	3.499e-05	NAND2BX1
g2736	0.0001449	9.841e-05	0.0002563	1.301e-05	CLKINVX1
g2672	0.0001778	6.293e-05	0.0002537	1.299e-05	OAI21X1
g2652	0.0001279	8.38e-05	0.0002241	1.236e-05	NOR2XL
g2718	5.107e-05	0.0001596	0.00022	9.289e-06	NAND2XL
g2697	0.000112	7.214e-05	0.0002191	3.499e-05	NAND2BX1
g2709	0.0001178	8.861e-05	0.0002188	1.236e-05	NOR2XL
g2678	6.658e-05	0.0001416	0.0002175	9.289e-06	NAND2XL
g2643	0.0001287	5.354e-05	0.0002036	2.127e-05	OAI2BB1X1
g2714	0.000116	7.373e-05	0.0002021	1.236e-05	NOR2XL
g2640	0.0001218	4.473e-05	0.0001789	1.236e-05	NOR2XL

g2761	9.18e-05	7.218e-05	0.0001733	9.289e-06	NAND2XL
g2586	0.0001093	4.373e-05	0.0001652	1.22e-05	AOI21XL
g2702	5.13e-05	0.0001036	0.0001641	9.289e-06	NAND2XL
g2698	5.43e-05	9.115e-05	0.0001547	9.289e-06	NAND2XL
g2658	3.629e-05	8.308e-05	0.0001544	3.499e-05	NAND2BX1
g2592	9.946e-05	3.622e-05	0.0001444	8.728e-06	OAI21XL
g2669	8.858e-05	3.799e-05	0.0001389	1.236e-05	NOR2XL
g2631	6.931e-05	4.818e-05	0.0001279	1.046e-05	NAND4XL
g2668	5.355e-05	4.809e-05	0.0001109	9.289e-06	NAND2XL
g2694	4.994e-05	2.402e-05	8.325e-05	9.289e-06	NAND2XL
g2667	2.887e-05	4.263e-05	8.196e-05	1.046e-05	NAND4XL
g2642	3.051e-05	2.406e-05	6.502e-05	1.046e-05	NAND4XL
g2655	2.734e-05	1.197e-05	5.232e-05	1.301e-05	INVX1

---

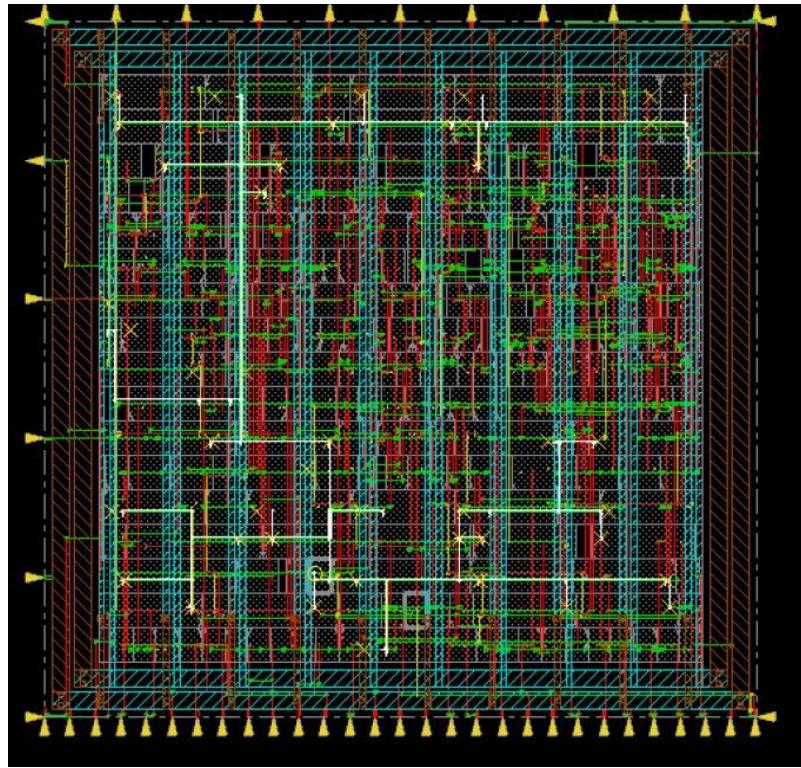
Total ( 242 of 242 )    0.2982    0.06552    0.375    0.01133  
 Total Capacitance        1.798e-12 F  
 Power Density            \*\*\* No Die Area \*\*\*

### Power Analysis:

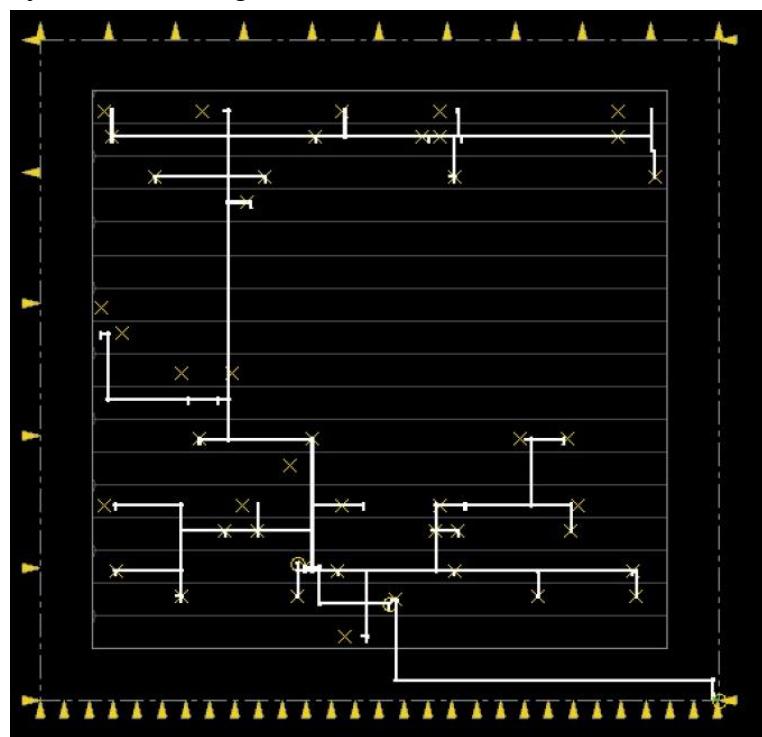
- Total Internal Power: 0.2982 mW
- Total switching power: 0.06552 mW
- Total leakage Power: 0.01133 mW
- Total Power Dissipated: 0.375 mW

- Layout (Clock Tree)

Clock Tree with all standard cells placed.



Clock tree with only clock showing:



# Post Routing

- Setup

```
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64 (Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:12:55 2022
5 # Design: rtl_module
6 # Command: optDesign -postRoute -hold
7 #####
8
9 -----
10 optDesign Final SI Timing Summary
11 -----
12 |
13 +-----+-----+-----+
14 | Setup mode | all | reg2reg | default |
15 +-----+-----+-----+
16 | WNS (ns):| 0.202 | 0.317 | 0.202 |
17 | TNS (ns):| 0.000 | 0.000 | 0.000 |
18 | Violating Paths:| 0 | 0 | 0 |
19 | All Paths:| 146 | 55 | 102 |
20 +-----+-----+-----+
21
22 +-----+-----+-----+
23 | | Real | Total |
24 | DRVs | Nr nets(terms) | Worst Vio | Nr nets(terms) |
25 | | | |
26 +-----+-----+-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 +-----+-----+-----+
32
33 Density: 95.048%
34 Total number of glitch violations: 0
```

```
1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64 (Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:13:00 2022
5 # Design: rtl_module
6 # Command: optDesign -postRoute -hold
7 #####
8 Path 1: MET Setup Check with Pin B_reg_reg[2]/CK
9 Endpoint: B_reg_reg[2]/D (v) checked with leading edge of 'clk'
10 Beginpoint: B[2] (v) triggered by leading edge of 'clk'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time 0.476
14 - Setup 2.074
15 + Phase Shift 4.000
16 - Uncertainty 0.500
17 = Required Time 1.902
18 - Arrival Time 1.700
19 = Slack Time 0.202
20 Clock Rise Edge 0.000
21 + Input Delay 1.200
22 + Network Insertion Delay 0.500
23 = Beginpoint Arrival Time 1.700
```

```
24 Timing Path:
25 +-----+-----+-----+-----+-----+-----+
26 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
27 | | | | | Time | | Time |
28 +-----+-----+-----+-----+-----+-----+
29 | B[2] | v | B[2] | | | 1.700 | 1.902 |
30 | B_reg_reg[2]/D | v | B[2] | SDFFFTRX1 | 0.000 | 1.700 | 1.902 |
31 +-----+-----+-----+-----+-----+-----+
32 Clock Rise Edge 0.000
33 = Beginpoint Arrival Time 0.000
34 Other End Path:
35 +-----+-----+-----+-----+-----+-----+
36 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
37 | | | | | Time | | Time |
38 +-----+-----+-----+-----+-----+-----+
39 | clk | ^ | clk | | | 0.000 | -0.202 |
40 | CTS_cdb_buf_00009/A | ^ | clk | CLKBUFX2 | 0.000 | 0.000 | -0.202 |
41 | CTS_cdb_buf_00009/Y | ^ | CTS_2 | CLKBUFX2 | 0.093 | 0.093 | -0.109 |
42 | CTS_cdb_buf_00008/A | ^ | CTS_2 | CLKBUFX2 | 0.000 | 0.093 | -0.109 |
43 | CTS_cdb_buf_00008/Y | ^ | CTS_1 | CLKBUFX2 | 0.383 | 0.476 | 0.274 |
44 | B_reg_reg[2]/CK | ^ | CTS_1 | SDFFFTRX1 | 0.000 | 0.476 | 0.274 |
45 +-----+-----+-----+-----+-----+-----+
```

- Hold

```

2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:12:55 2022
5 # Design: rtl_module
6 # Command: optDesign -postRoute -hold
7 #####
8
9 -----
10    optDesign Final SI Timing Summary
11 -----
12
13 +-----+-----+-----+
14 | Hold mode | all | reg2reg | default |
15 +-----+-----+-----+
16 | WNS (ns): | -1.067 | -0.149 | -1.067 |
17 | TNS (ns): | -28.838 | -1.476 | -27.363 |
18 | Violating Paths: | 78 | 25 | 45 |
19 | All Paths: | 146 | 55 | 102 |
20 +-----+-----+-----+
21
22 +-----+-----+-----+
23 | | Real | Total |
24 | DRVs | Nr nets(terms) | Worst Vio | Nr nets(terms) |
25 | | | |
26 +-----+-----+-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 +-----+-----+-----+
32
33 Density: 95.048%
34 Total number of glitch violations: 0

```

```

1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 20:12:55 2022
5 # Design: rtl_module
6 # Command: optDesign -postRoute -hold
7 #####
8 Path 1: VIOLATED Hold Check with Pin A_reg_reg[5]/CK
9 Endpoint: A_reg_reg[5]/SE (v) checked with leading edge of 'clk'
10 Beginpoint: scan_en (v) triggered by leading edge of '@'
11 Path Groups: {clk}
12 Analysis View: view1
13 Other End Arrival Time 0.518
14 + Hold 0.050
15 + Phase Shift 0.000
16 + Uncertainty 0.500
17 = Required Time 1.067
18 Arrival Time 0.000
19 Slack Time -1.067
20     Clock Rise Edge 0.000
21     + Input Delay 0.000
22     = Beginpoint Arrival Time 0.000

```

```

23 Timing Path:
24 +-----+-----+-----+-----+-----+-----+
25 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
26 | | | | | Time | | Time |
27 +-----+-----+-----+-----+-----+-----+
28 | scan_en | v | scan_en | SDFFQX1 | 0.000 | 0.000 | 1.067 |
29 | A_reg_reg[5]/SE | v | scan_en | SDFFQX1 | 0.000 | 0.000 | 1.067 |
30 +-----+-----+-----+-----+-----+-----+
31 Clock Rise Edge 0.000
32 + Source Insertion Delay 0.022
33 = Beginpoint Arrival Time 0.022
34 Other End Path:
35 +-----+-----+-----+-----+-----+-----+
36 | Pin | Edge | Net | Cell | Delay | Arrival | Required |
37 | | | | | Time | | Time |
38 +-----+-----+-----+-----+-----+-----+
39 | clk | ^ | clk | CLKBUFX2 | 0.000 | 0.022 | -1.045 |
40 | CTS_cdb_buf_00009/A | ^ | clk | CLKBUFX2 | 0.000 | 0.022 | -1.045 |
41 | CTS_cdb_buf_00009/Y | ^ | CTS_2 | CLKBUFX2 | 0.093 | 0.115 | -0.952 |
42 | CTS_cdb_buf_00008/A | ^ | CTS_2 | CLKBUFX2 | 0.000 | 0.115 | -0.952 |
43 | CTS_cdb_buf_00008/Y | ^ | CTS_1 | CLKBUFX2 | 0.402 | 0.517 | -0.550 |
44 | A_reg_reg[5]/CK | ^ | CTS_1 | SDFFQX1 | 0.001 | 0.518 | -0.550 |
45 +-----+-----+-----+-----+-----+-----+

```

Setup Slack: 0.202 ns (Effect described before)

Hold Slack : -1.067ns Since, our hold is negative our design won't work for this utilization.

## Hold analysis for utilization 0.65

```
4 # Generated on: Sat Apr 30 19:57:28 2022
5 # Design: rtl_module
6 # Command: optDesign -postCTS -hold
7 #####
8 -
9 -----
10    optDesign Final Summary
11 -----
12
13 +-----+-----+-----+
14 | Hold mode | all | reg2reg | default |
15 +-----+-----+-----+
16 |      WNS (ns):| 0.001 | 0.001 | 0.060 |
17 |      TNS (ns):| 0.000 | 0.000 | 0.000 |
18 | Violating Paths:| 0 | 0 | 0 |
19 | All Paths:| 146 | 55 | 102 |
20 +-----+-----+-----+
21
22 +-----+-----+-----+
23 | | Real | Total |
24 | DRVs +-----+-----+
25 | | Nr nets(terms) | Worst Vio | Nr nets(terms) |
26 +-----+-----+-----+
27 | max_cap | 0 (0) | 0.000 | 0 (0) |
28 | max_tran | 0 (0) | 0.000 | 0 (0) |
29 | max_fanout | 0 (0) | 0 | 0 (0) |
30 | max_length | 0 (0) | 0 | 0 (0) |
31 +-----+-----+-----+
32
33 Density: 84.362%
34 Routing Overflow: 0.00% H and 0.00% V
35
```

```
1 #####
2 # Generated by: Cadence Innovus 20.10-p004_1
3 # OS: Linux x86_64(Host ID edaserver4)
4 # Generated on: Sat Apr 30 19:59:36 2022
5 # Design: rtl_module
6 # Command: timeDesign -postRoute -hold -pathReports -slackReports -numPaths 50 -prefix rtl_module_postRoute -
7 # outDir timingReports
8
9 -----
10    timeDesign Summary
11 -----
12
13 +-----+-----+-----+
14 | Hold mode | all | reg2reg | default |
15 +-----+-----+-----+
16 |      WNS (ns):| 0.007 | 0.007 | 0.016 |
17 |      TNS (ns):| 0.000 | 0.000 | 0.000 |
18 | Violating Paths:| 0 | 0 | 0 |
19 | All Paths:| 146 | 55 | 102 |
20 +-----+-----+-----+
21
```

Post CTS and Post routing we have no hold violations for utilization of 0.65.

- Area

```

10 =====
11 General Design Information
12 =====
13 Design Status: Routed
14 Design Name: rtl_module
15 # Instances: 242
16 # Hard Macros: 0
17 # Std Cells: 242
18 -----
19 Standard Cells in Netlist
20 -----
21          Cell Type   Instance Count   Area (um^2)
22          OAI2BB1X1      2           10.5966
23          | DLY4X1       2           52.9830
24          CLKBUFX2      16          72.6624
25          | OR2XL        3           13.6242
26          BUFX2         1           4.5414
27          OAI222XL      1           8.3259
28          AND2X1        1           4.5414
29          OAI211X1      3           15.8949
30          SDFFQX1       36          735.7068
31          XNOR2X1       3           24.9777
32          AND2XL        23          104.4522
33          XOR2XL        1           8.3259
34          OAI21X1       11          49.9554
35          CLKINVX1      2           4.5414
36          AOI211X1      1           5.2983
37          NAND2BX1      10          45.4140
38          SDFFQXL       1           20.4363
39          XNOR2XL       3           24.9777
40          NAND3X1       1           4.5414
41          NAND2XL       11          33.3036
42          NOR2BX1       8            36.3312
43          CLKAND2X2     1           5.2983
44          OAI22X1       3           18.1656
45          OAI21XL        1           4.5414
46          AOI21X1       7            31.7898
47          | INVXL        2           4.5414
48          NOR3X1        1           4.5414
49          NAND4X1       1           6.0552
50          | INVX1        7            15.8949
51          SDFFTRX1      6            163.4904
52          OAI22XL        7           42.3864
53          NOR2XL        28          84.7728
54          AOI22X1       3           18.1656
55          AOI21XL        6           27.2484
56          AOI32X1       1           6.8121
57          DLY1X1        22          183.1698
58          NAND4XL       3           15.8949
59          MXI2XL        3           18.1656
60  # Pads: 0
61  # Net: 288
62  # Special Net: 2

```

```

3481 =====
3482 Floorplan/Placement Information
3483 =====
3484 Total area of Standard cells: 1932.366 um^2
3485 Total area of Standard cells(Subtracting Physical Cells): 1932.366 um^2
3486 Total area of Macros: 0.000 um^2
3487 Total area of Blockages: 0.000 um^2
3488 Total area of Pad cells: 0.000 um^2
3489 Total area of Core: 2033.033 um^2
3490 Total area of Chip: 2831.311 um^2
3491 Effective Utilization: 9.5048e-01
3492 Number of Cell Rows: 17
3493 % Pure Gate Density #1 (Subtracting BLOCKAGES): 95.048%
3494 % Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 95.048%
3495 % Pure Gate Density #3 (Subtracting MACROS): 95.048%
3496 % Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 95.048%
3497 % Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 95.048%
3498 % Pure Gate Density #6 ((Unreplaced Standard Inst + Unreplaced Block Inst + Unreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 95.048%
3499 % Core Density (Counting Std Cells and MACROS): 95.048%
3500 % Core Density #(Subtracting Physical Cells): 95.048%
3501 % Chip Density (Counting Std Cells and MACROS and IOs): 68.250%
3502 % Chip Density #2(Subtracting Physical Cells): 68.250%
3503 # Macros within 5 sites of IO pad: No
3504 Macro halo defined?: No
3505 =====
3506 =====
3507 Wire Length Distribution
3508 =====
3509 Total Metal1 wire length: 114.5500 um
3510 Total Metal2 wire length: 2160.2750 um
3511 Total Metal3 wire length: 1527.1400 um
3512 Total Metal4 wire length: 931.7700 um
3513 Total Metal5 wire length: 0.0000 um
3514 Total Metal6 wire length: 0.0000 um
3515 Total Metal7 wire length: 0.0000 um
3516 Total Metal8 wire length: 0.0000 um
3517 Total Metal9 wire length: 0.0000 um
3518 Total wire length: 4733.7350 um
3519 Average wire length/net: 16.4366 um
3520 Area of Power Net Distribution:
3521 =====
3522 Area of Power Net Distribution
3523 =====
3524 Layer Name Area of Power Net Routable Area Percentage
3525 Metal1 0.0000 2033.034 0.0000%
3526 Metal2 0.0000 2033.034 0.0000%
3527 Metal3 0.0000 2033.034 0.0000%
3528 Metal4 0.0000 2033.034 0.0000%
3529 Metal5 0.0000 2033.034 0.0000%
3530 Metal6 0.0000 2033.034 0.0000%
3531 Metal7 0.0000 2033.034 0.0000%
3532 Metal8 299.2820 2033.034 14.7210%
3533 Metal9 198.7170 2033.034 9.3809% For more information click here

```

**Area Analysis:** The total number of instances have remained same post the Routing stage as compared to post CTS stage and no macros have been added. The total area has remained the same since the area constraint is much tighter due to high core utilization and therefore additional components cannot be added to fix any kind of violations, which leads to hold violations while doing the timing analysis. Total metal wire length increases by approximately 300 um since some extra metal has been used in the existing layers and additional metal-1 layer has been added and metal-5 layer has been removed from the design as part of tool optimizations.

## ● Power

```

*      Power Units = 1mW
*
*      Time Units = 1e-09 secs
*
*      Temperature = 125
*
*      report_power -outfile ./PostRoutingPowerRpt/rtl_module.rpt -rail_analysis_format VS
*
```

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
CTS_cdb_buf_00008	0.003579	0.02164	0.02526	4.129e-05	CLKBUFX2
B_reg_reg[2]	0.006241	0.0005283	0.006936	0.0001662	SDFFTRX1
B_reg_reg[0]	0.006272	0.0004814	0.00692	0.0001662	SDFFTRX1
out_reg[1]	0.006161	0.0003793	0.006677	0.0001363	SDFFQX1
out_reg[2]	0.006099	0.0003664	0.006601	0.0001363	SDFFQX1
A_reg_reg[4]	0.005847	0.0005395	0.006553	0.0001662	SDFFTRX1
A_reg_reg[1]	0.005807	0.0004352	0.006408	0.0001662	SDFFTRX1
A_reg_reg[6]	0.005852	0.0003571	0.006375	0.0001662	SDFFTRX1
out_reg[4]	0.005834	0.0001647	0.006135	0.0001363	SDFFQX1
out_reg[5]	0.005649	0.0003134	0.006099	0.0001363	SDFFQX1
out_reg[3]	0.005758	0.0001889	0.006083	0.0001363	SDFFQX1
out_reg[0]	0.005626	0.0002664	0.006029	0.0001363	SDFFQX1
in1/count_reg_reg[1]	0.005512	0.0003067	0.005955	0.0001363	SDFFQX1
out_reg[9]	0.00547	0.0003483	0.005954	0.0001363	SDFFQX1
in1/count_reg_reg[0]	0.005605	0.00021	0.005951	0.0001363	SDFFQX1
out_reg[8]	0.005518	0.0002253	0.005879	0.0001363	SDFFQX1
out_reg[6]	0.005546	0.0001542	0.005836	0.0001363	SDFFQX1
in1/clk_out_reg	0.005402	0.0002644	0.005803	0.0001363	SDFFQX1
out_reg[7]	0.005398	0.0002307	0.005765	0.0001363	SDFFQX1
B_reg_reg[9]	0.00524	0.0003571	0.005733	0.0001363	SDFFQX1
A_reg_reg[8]	0.005299	0.0002491	0.005714	0.0001662	SDFFTRX1
B_reg_reg[1]	0.005026	0.0003817	0.005544	0.0001363	SDFFQX1
A_reg_reg[9]	0.004963	0.0004287	0.005528	0.0001363	SDFFQX1
C_reg_reg[4]	0.00495	0.0004174	0.005504	0.0001363	SDFFQX1
C_reg_reg[6]	0.004929	0.0004215	0.005487	0.0001363	SDFFQX1
B_reg_reg[6]	0.004971	0.00037	0.005478	0.0001363	SDFFQX1
B_reg_reg[7]	0.004964	0.0003643	0.005465	0.0001363	SDFFQX1
C_reg_reg[3]	0.004959	0.0003561	0.005452	0.0001363	SDFFQX1
A_reg_reg[2]	0.004963	0.0003261	0.005425	0.0001363	SDFFQX1
B_reg_reg[5]	0.004949	0.0003356	0.005421	0.0001363	SDFFQX1
B_reg_reg[3]	0.004966	0.0002871	0.00539	0.0001363	SDFFQX1
C_reg_reg[2]	0.004965	0.0002823	0.005383	0.0001363	SDFFQX1
B_reg_reg[8]	0.004973	0.0002608	0.00537	0.0001363	SDFFQX1
C_reg_reg[1]	0.004965	0.0002648	0.005366	0.0001363	SDFFQX1
A_reg_reg[7]	0.004965	0.0002622	0.005363	0.0001363	SDFFQX1
A_reg_reg[0]	0.004927	0.0002977	0.00536	0.0001363	SDFFQX1
A_reg_reg[5]	0.004831	0.0003504	0.005317	0.0001363	SDFFQX1
C_reg_reg[0]	0.004963	0.0002173	0.005316	0.0001363	SDFFQX1
C_reg_reg[7]	0.004878	0.0003	0.005314	0.0001363	SDFFQX1
B_reg_reg[4]	0.004918	0.0002544	0.005309	0.0001363	SDFFQX1
A_reg_reg[3]	0.004764	0.0003663	0.005266	0.0001363	SDFFQX1
C_reg_reg[5]	0.004764	0.0002562	0.005156	0.0001363	SDFFQX1
out_reg[10]	0.004842	2.442e-05	0.004996	0.0001296	SDFFQXL
C_reg_reg[8]	0.004508	0.0001931	0.004838	0.0001363	SDFFQX1
CTS_cdb_buf_00009	0.003583	0.0006655	0.00429	4.129e-05	CLKBUFX2
FE_OFCl_rst	0.0003857	0.001349	0.001776	4.129e-05	BUFX2
FE_PHC19_scan_en	0.0001439	0.001544	0.001729	4.129e-05	CLKBUFX2
g2617	0.0003473	0.001165	0.001529	1.612e-05	NAND4X1
g2645	0.001001	0.0002437	0.001265	2.034e-05	NOR3X1
FE_PHC16_out_2	0.0007703	0.0004012	0.001226	5.435e-05	DLY1X1
FE_PHC8_out_1	0.000795	0.0002584	0.001108	5.435e-05	DLY1X1
g2638	0.0005735	0.0004655	0.001057	1.815e-05	AOI21X1
FE_PHC12_out_5	0.0006297	0.0002819	0.000966	5.435e-05	DLY1X1
g2687	0.0005829	0.0002802	0.0009336	7.055e-05	XNOR2X1
in1/FE_PHC33_count_reg_0	0.0005751	0.0002999	0.0009294	5.435e-05	DLY1X1
FE_PHC14_out_0	0.0006328	0.0002385	0.0009256	5.435e-05	DLY1X1
g2633	0.0007337	0.0001614	0.0009151	2.004e-05	NOR2BX1
g2679	0.0004857	0.0004042	0.00091	2.004e-05	NOR2BX1
FE_PHC13_out_9	0.0005756	0.0002517	0.0008816	5.435e-05	DLY1X1
FE_PHC5_out_4	0.0006857	0.000138	0.000878	5.435e-05	DLY1X1
g2632	0.0005519	0.0003032	0.0008732	1.815e-05	AOI21X1
g2629	0.0004734	0.0003794	0.0008657	1.299e-05	AOI21X1
g2644	0.0006473	0.000198	0.0008653	1.995e-05	AOI211X1
g2664	0.0006051	0.0002266	0.0008497	1.791e-05	OAII2X1
in1/g72	0.0007025	8.823e-05	0.0008357	4.5e-05	CLKAND2X2
g2623	0.0004943	0.0003196	0.000828	1.41e-05	OAII21X1
FE_PHC7_out_8	0.0005893	0.000178	0.0008217	5.435e-05	DLY1X1

FE_PHC28_out_3	0.0006636	9.978e-05	0.0008177	5.435e-05	DLY1X1
g2685	0.0004894	0.0002355	0.0007954	7.055e-05	XNOR2X1
FE_PHC11_out_7	0.0005534	0.0001785	0.0007863	5.435e-05	DLY1X1
g2676	0.0005852	0.0001688	0.000774	2.004e-05	NOR2BX1
g2688	0.0004833	0.0002125	0.0007663	7.055e-05	XNOR2X1
g2603	0.000521	0.0002303	0.0007643	1.299e-05	OAI21X1
g2665	0.0006033	0.0001359	0.0007573	1.815e-05	AOI21X1
g2651	0.000499	0.0002337	0.0007509	1.815e-05	AOI21X1
FE_PHC6_out_6	0.0005941	0.0001022	0.0007507	5.435e-05	DLY1X1
g2650	0.000398	0.0003363	0.0007473	1.299e-05	OAI21X1
FE_PHC26_A_reg_9	0.0004672	0.0002208	0.0007294	4.129e-05	CLKBUFX2
g2704	0.0002754	0.0004399	0.0007277	1.236e-05	NOR2XL
g2699	0.0004819	0.0002105	0.0007125	2.004e-05	NOR2BX1
g2649	0.0005315	0.0001051	0.0006996	6.308e-05	XNOR2XL
g2666	0.0004431	0.0002373	0.0006934	1.299e-05	OAI21X1
in1/FE_PHC29_out1	0.0005293	0.0001058	0.0006895	5.435e-05	DLY1X1
g2681	0.0003455	0.0002981	0.0006786	3.499e-05	NAND2BX1
FE_PHC27_n_1	0.0004585	0.0001763	0.0006761	4.129e-05	CLKBUFX2
g2674	0.0005338	0.0001158	0.0006696	2.004e-05	NOR2BX1
g2619	0.0003018	0.0003552	0.0006694	1.236e-05	NOR2XL
g2680	0.0002586	0.0003754	0.000669	3.499e-05	NAND2BX1
in1/g2	0.0004754	0.000122	0.0006657	6.826e-05	XOR2XL
FE_PHC22_A_reg_2	0.0004661	0.0001446	0.0006521	4.129e-05	CLKBUFX2
g2806	0.0004809	9.738e-05	0.0006414	6.308e-05	XNOR2XL
FE_PHC24_n_4	0.0004606	0.000136	0.000638	4.129e-05	CLKBUFX2
g2	0.0004829	8.818e-05	0.0006342	6.308e-05	XNOR2XL
FE_PHC21_C_reg_4	0.0004664	0.0001233	0.0006309	4.129e-05	CLKBUFX2
FE_PHC25_n_0	0.0004449	0.0001393	0.0006255	4.129e-05	CLKBUFX2
g2587	0.0004103	0.000201	0.0006235	1.22e-05	AOI21XL
g2693	0.0004913	0.000112	0.0006233	2.004e-05	NOR2BX1
FE_PHC20_C_reg_3	0.000467	0.0001142	0.0006225	4.129e-05	CLKBUFX2
FE_PHC23_A_reg_5	0.0004411	0.0001386	0.0006211	4.129e-05	CLKBUFX2
g2621	0.0003725	0.0002299	0.0006203	1.791e-05	OAI22X1
g2626	0.000363	0.0002327	0.0006141	1.833e-05	AOI22X1
g2660	0.0003948	0.0002003	0.0006134	1.833e-05	AOI22X1
g2768	0.0004552	0.0001319	0.0006117	2.466e-05	AND2XL
FE_PHC3_C_reg_6	0.0004621	9.274e-05	0.0006225	4.129e-05	CLKBUFX2
g2602	0.0003853	0.0001893	0.0005925	1.791e-05	OAI22X1
g2675	0.0003451	0.0002119	0.000592	3.499e-05	NAND2BX1
FE_PHC18_B_reg_5	0.0004635	8.696e-05	0.0005918	4.129e-05	CLKBUFX2
g2772	0.000458	0.0001079	0.0005905	2.466e-05	AND2XL
g2682	0.0003909	0.0001791	0.0005881	1.815e-05	AOI21X1
FE_PHC17_B_reg_7	0.0004709	7.183e-05	0.000584	4.129e-05	CLKBUFX2
FE_PHC15_n_5	0.0004195	0.000108	0.0005819	5.435e-05	DLY1X1
g2774	0.0004611	9.379e-05	0.0005795	2.466e-05	AND2XL
g2695	0.0004411	0.0001141	0.0005752	2.004e-05	NOR2BX1
FE_PHC10_n_3	0.000429	8.926e-05	0.0005726	5.435e-05	DLY1X1
g2612	0.000336	0.0002153	0.0005696	1.833e-05	AOI22X1
g2775	0.0004657	7.748e-05	0.0005678	2.466e-05	AND2XL
FE_PHC4_B_reg_1	0.0004347	8.282e-05	0.0005588	4.129e-05	CLKBUFX2
g2777	0.0004696	6.354e-05	0.0005578	2.466e-05	AND2XL
g2760	0.0004708	5.954e-05	0.000555	2.466e-05	AND2XL
g2757	0.0004715	5.692e-05	0.0005531	2.466e-05	AND2XL
g2773	0.0004724	5.397e-05	0.000551	2.466e-05	AND2XL
FE_PHC35_C_reg_1	0.0004312	6.525e-05	0.0005508	5.435e-05	DLY1X1
FE_OFC0_rst	0.0002824	0.0002554	0.0005508	1.301e-05	INVX1
FE_PHC37_A_reg_0	0.0004159	7.931e-05	0.0005496	5.435e-05	DLY1X1
in1/FE_PHC34_B_reg_6	0.0004333	5.943e-05	0.0005471	5.435e-05	DLY1X1
g2600	0.000368	0.0001643	0.0005464	1.41e-05	OAI21X1
FE_PHC32_C_reg_0	0.0004295	6.086e-05	0.0005448	5.435e-05	DLY1X1
g2624	0.0002718	0.0002572	0.0005431	1.41e-05	OAI21X1
FE_PHC36_B_reg_3	0.0004301	5.396e-05	0.0005384	5.435e-05	DLY1X1
g2659	0.0003506	0.0001728	0.0005356	1.22e-05	AOI21XL
FE_PHC2_A_reg_3	0.0004096	8.119e-05	0.000532	4.129e-05	CLKBUFX2
g2683	0.0002832	0.0002347	0.0005309	1.299e-05	OAI21X1
g2656	0.0003065	0.0002005	0.0005251	1.815e-05	AOI21X1
g2700	0.000266	0.0002235	0.0005245	3.499e-05	NAND2BX1
g2684	0.0002654	0.0002231	0.0005235	3.499e-05	NAND2BX1
g2689	0.0002571	0.000239	0.0005232	2.704e-05	MX12XL
g2610	0.0003668	0.0001434	0.0005224	1.224e-05	OAI22XL
g2657	0.0003097	0.0001926	0.0005204	1.815e-05	AOI21X1
FE_PHC38_C_reg_7	0.0004075	5.745e-05	0.0005193	5.435e-05	DLY1X1
g2635	0.0002642	0.0002391	0.0005163	1.299e-05	OAI21X1
g2627	0.0003695	0.0001327	0.0005144	1.22e-05	AOI21XL
g2641	0.0003601	0.0001408	0.0005133	1.236e-05	NOR2XL
g2677	0.0003006	0.0001993	0.0005123	1.236e-05	NOR2XL
g2663	0.0003515	0.0001451	0.000509	1.236e-05	NOR2XL
g2637	0.0003711	0.0001212	0.0005044	1.22e-05	AOI21XL
g2614	0.0003876	9.545e-05	0.0005016	1.851e-05	AOI32XL
g2671	0.000379	0.000109	0.000501	1.299e-05	OAI21X1
g2613	0.0003721	0.0001125	0.0004967	1.22e-05	AOI21XL

g2710	0.0002745	0.0002086	0.0004955	1.236e-05	NOR2XL
in1/g62	0.0003714	0.0001054	0.0004892	1.236e-05	NOR2XL
g2648	0.00025	0.0002217	0.0004846	1.299e-05	OAI21X1
g2591	0.0003726	9.758e-05	0.0004826	1.236e-05	NOR2XL
in1/g67	0.0002596	0.0002069	0.0004788	1.236e-05	NOR2XL
g2711	0.0002462	0.00022	0.0004785	1.236e-05	NOR2XL
g2662	0.00036	0.0001056	0.0004779	1.236e-05	NOR2XL
FE_PHC30_DFT_sdi_2	0.0003347	1.989e-05	0.0004737	0.0001191	DLY4X1
FE_PHC31_DFT_sdi_1	0.0003346	1.758e-05	0.0004713	0.0001191	DLY4X1
g2696	0.0002746	0.0001788	0.0004658	1.236e-05	NOR2XL
g2713	0.0002753	0.0001779	0.0004655	1.236e-05	NOR2XL
g2639	0.0003447	9.988e-05	0.000457	1.236e-05	NOR2XL
g2628	0.0003421	8.814e-05	0.0004426	1.236e-05	NOR2XL
g2616	0.0003412	8.732e-05	0.0004409	1.236e-05	NOR2XL
g2686	0.0002403	0.000164	0.0004313	2.704e-05	MXI2XL
g2690	0.000258	0.0001431	0.0004282	2.704e-05	MXI2XL
g2712	0.0002741	0.0001369	0.0004234	1.236e-05	NOR2XL
g2608	0.0002919	0.0001179	0.0004218	1.205e-05	OAI22XL
g2630	0.0002664	0.0001423	0.0004217	1.301e-05	INVX1
g2670	0.0002493	0.0001577	0.0004194	1.236e-05	NOR2XL
FE_PHC9_n_2	0.0002969	4.641e-05	0.0003976	5.435e-05	DLY1X1
FE_PHC39_C_reg_8	0.0002987	4.21e-05	0.0003952	5.435e-05	DLY1X1
g2706	0.0002745	0.0001041	0.000391	1.236e-05	NOR2XL
g2604	0.0002702	9.846e-05	0.00039	2.127e-05	OAI2BB1X1
g2588	0.0002785	9.548e-05	0.000386	1.205e-05	OAI22XL
g2584	0.0002683	0.0001037	0.000384	1.205e-05	OAI22XL
g2607	0.0002753	9.653e-05	0.0003839	1.205e-05	OAI22XL
g2691	0.0002285	0.0001156	0.0003824	3.828e-05	OR2XL
g2661	0.0001955	0.0001707	0.0003813	1.511e-05	NAND3X1
g2609	0.0002699	9.925e-05	0.0003812	1.205e-05	OAI22XL
g2606	0.0002596	9.958e-05	0.0003713	1.205e-05	OAI22XL
g2673	0.0001798	0.0001755	0.0003683	1.299e-05	OAI21X1
g2692	0.0002258	0.0001041	0.0003682	3.828e-05	OR2XL
g2654	0.0002344	0.0001213	0.0003681	1.236e-05	NOR2XL
g2738	0.0001344	0.0002204	0.0003678	1.301e-05	INVX1
g2601	0.0002668	8.737e-05	0.0003662	1.205e-05	OAI22XL
g2708	0.0001254	0.0002198	0.0003544	9.289e-06	NAND2XL
g2737	0.0001486	0.000188	0.0003497	1.301e-05	INVX1
g2765	0.0002134	0.0001058	0.0003439	2.466e-05	AND2XL
g2756	0.0002135	0.0001017	0.0003398	2.466e-05	AND2XL
g2715	0.0001185	0.0002043	0.0003321	9.289e-06	NAND2XL
g2705	0.0002386	7.901e-05	0.0003299	1.236e-05	NOR2XL
g2758	0.0002144	8.618e-05	0.0003253	2.466e-05	AND2XL
g2636	0.0002182	9.409e-05	0.0003253	1.299e-05	OAI21X1
g2762	0.0002146	8.363e-05	0.0003229	2.466e-05	AND2XL
g2720	0.0001576	0.0001505	0.0003211	1.301e-05	INVX1
g2646	0.000203	8.232e-05	0.0003203	3.499e-05	NAND2BX1
g2755	0.0002148	8.032e-05	0.0003198	2.466e-05	AND2XL
g2759	0.0002148	8.03e-05	0.0003198	2.466e-05	AND2XL
g2769	0.0002151	7.568e-05	0.0003154	2.466e-05	AND2XL
g2776	0.0002151	7.548e-05	0.0003152	2.466e-05	AND2XL
g2719	0.000154	0.0001477	0.0003147	1.301e-05	INVX1
g2653	0.0001609	0.0001432	0.0003135	9.289e-06	NAND2XL
g2767	0.0002154	7.036e-05	0.0003104	2.466e-05	AND2XL
g2766	0.0002154	6.992e-05	0.00031	2.466e-05	AND2XL
g2701	0.0002088	7.807e-05	0.0003069	2.004e-05	NOR2BX1
g2754	0.0002158	6.405e-05	0.0003045	2.466e-05	AND2XL
g2615	0.0001985	6.891e-05	0.0003024	3.499e-05	NAND2BX1
g2763	0.0002116	6.088e-05	0.0003015	2.466e-05	AND2XL
g2770	0.0002162	5.777e-05	0.0002986	2.466e-05	AND2XL
g2707	0.0001696	8.826e-05	0.0002962	3.828e-05	OR2XL
g2771	0.0002164	5.321e-05	0.0002943	2.466e-05	AND2XL
g2736	0.000147	0.0001342	0.0002942	1.301e-05	CLKINVX1
g2764	0.0002167	4.853e-05	0.0002899	2.466e-05	AND2XL
g2721	0.000157	0.0001156	0.0002857	1.301e-05	CLKINVX1
g2716	9.708e-05	0.0001789	0.0002853	9.289e-06	NAND2XL
in1/g69	0.0001243	0.0001483	0.0002813	8.757e-06	INVXL
g2634	0.0001918	7.574e-05	0.0002799	1.236e-05	NOR2XL
g2647	0.0001617	0.0001035	0.0002775	1.236e-05	NOR2XL
g2618	0.0002007	6.67e-05	0.0002761	8.757e-06	INVXL
g2703	0.0001131	0.0001219	0.0002701	3.499e-05	NAND2BX1
g2717	0.0001381	0.0001043	0.0002696	2.717e-05	AND2X1
g2672	0.0001779	6.641e-05	0.0002573	1.299e-05	OAI21X1
g2709	0.0001178	9.76e-05	0.0002278	1.236e-05	NOR2XL
g2652	0.0001281	8.613e-05	0.0002266	1.236e-05	NOR2XL
g2697	0.0001119	7.582e-05	0.0002227	3.499e-05	NAND2BX1
g2718	5.105e-05	0.000162	0.0002224	9.289e-06	NAND2XL
g2678	6.66e-05	0.0001442	0.0002201	9.289e-06	NAND2XL
g2714	0.000116	8.12e-05	0.0002096	1.236e-05	NOR2XL
g2643	0.000129	5.904e-05	0.0002093	2.127e-05	OAI2BB1X1
g2640	0.0001217	4.822e-05	0.0001823	1.236e-05	NOR2XL

g2761	9.206e-05	7.231e-05	0.0001737	9.289e-06	NAND2XL
g2702	5.133e-05	0.0001027	0.0001633	9.289e-06	NAND2XL
g2586	0.0001099	4.065e-05	0.0001628	1.22e-05	AOI21XL
g2698	5.437e-05	9.573e-05	0.0001594	9.289e-06	NAND2XL
g2592	9.928e-05	4.77e-05	0.0001557	8.728e-06	OAI21XL
g2658	3.632e-05	8.412e-05	0.0001554	3.499e-05	NAND2BX1
g2669	8.861e-05	4.129e-05	0.0001423	1.236e-05	NOR2XL
g2631	6.942e-05	5.072e-05	0.0001306	1.046e-05	NAND4XL
g2668	5.372e-05	4.439e-05	0.0001074	9.289e-06	NAND2XL
g2694	5.004e-05	2.521e-05	8.454e-05	9.289e-06	NAND2XL
g2667	2.887e-05	4.277e-05	8.21e-05	1.046e-05	NAND4XL
g2642	3.052e-05	2.557e-05	6.655e-05	1.046e-05	NAND4XL
g2655	2.736e-05	1.274e-05	5.312e-05	1.301e-05	INVX1

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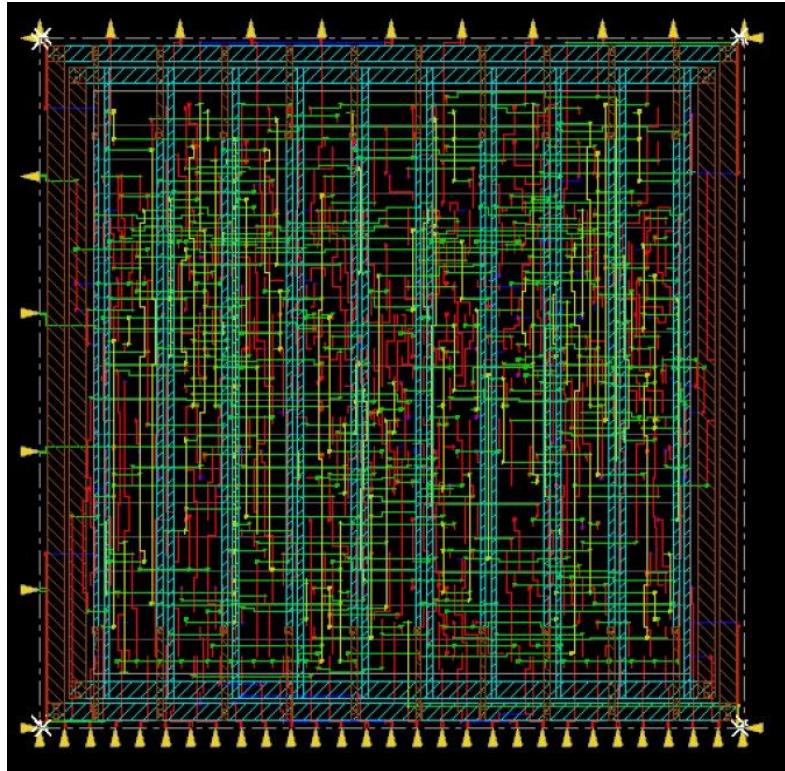
Total ( 242 of 242 )    0.2996    0.06735    0.3782    0.01133  
 Total Capacitance                1.835e-12 F  
 Power Density                   \*\*\* No Die Area \*\*\*

### Power Analysis:

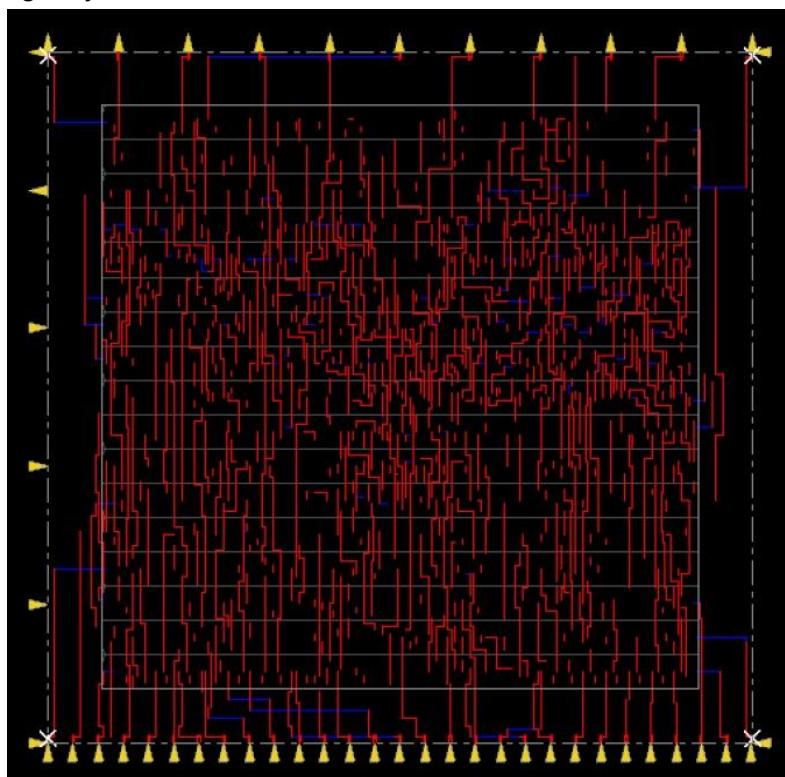
- Total Internal Power: 0.2996 mW
- Total switching power: 0.06735 mW
- Total leakage Power: 0.01133 mW
- Total Power Dissipated: 0.3782 mW

- Layout (Metal Layer)

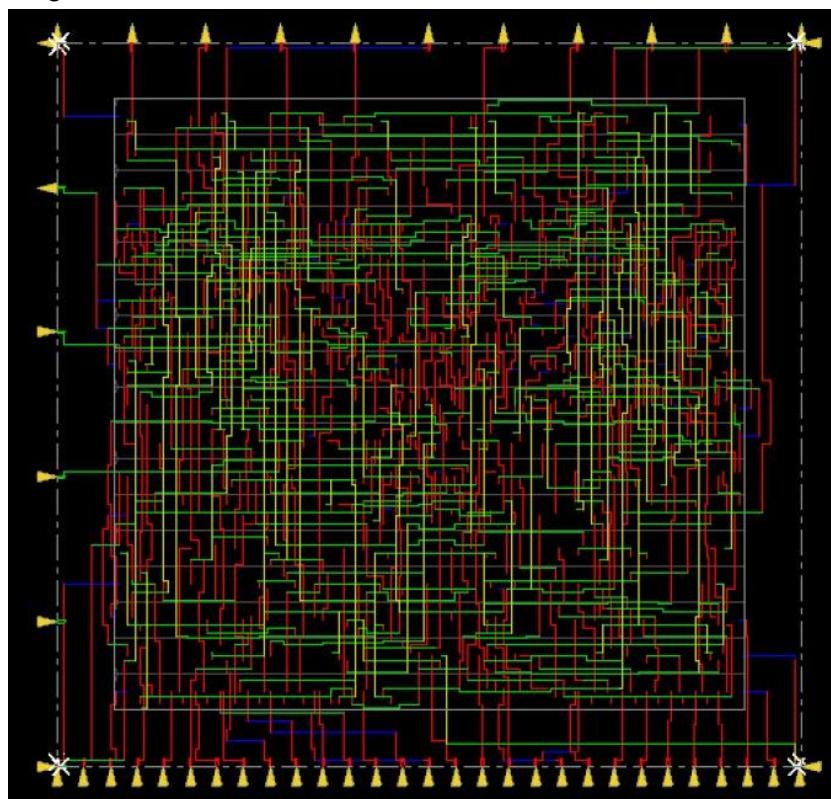
Screenshot showing all completed routed design:



Screenshot showing only M1 & M2:



Screenshot showing M1-M6 Metals:



Screenshot showing M1-M9 Metals:

