OAI-33 Complex Gate - Domino

Group Number: 7

Group Members :

- **Saksham Gupta – 2019199**
- **Samaksh Gupta – 2019200**
- **Shragvi Sidharth Jha – 2019207**
- **Mihir Chaturvedi– 2019175**

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INFORMATION TECHNOLOGY
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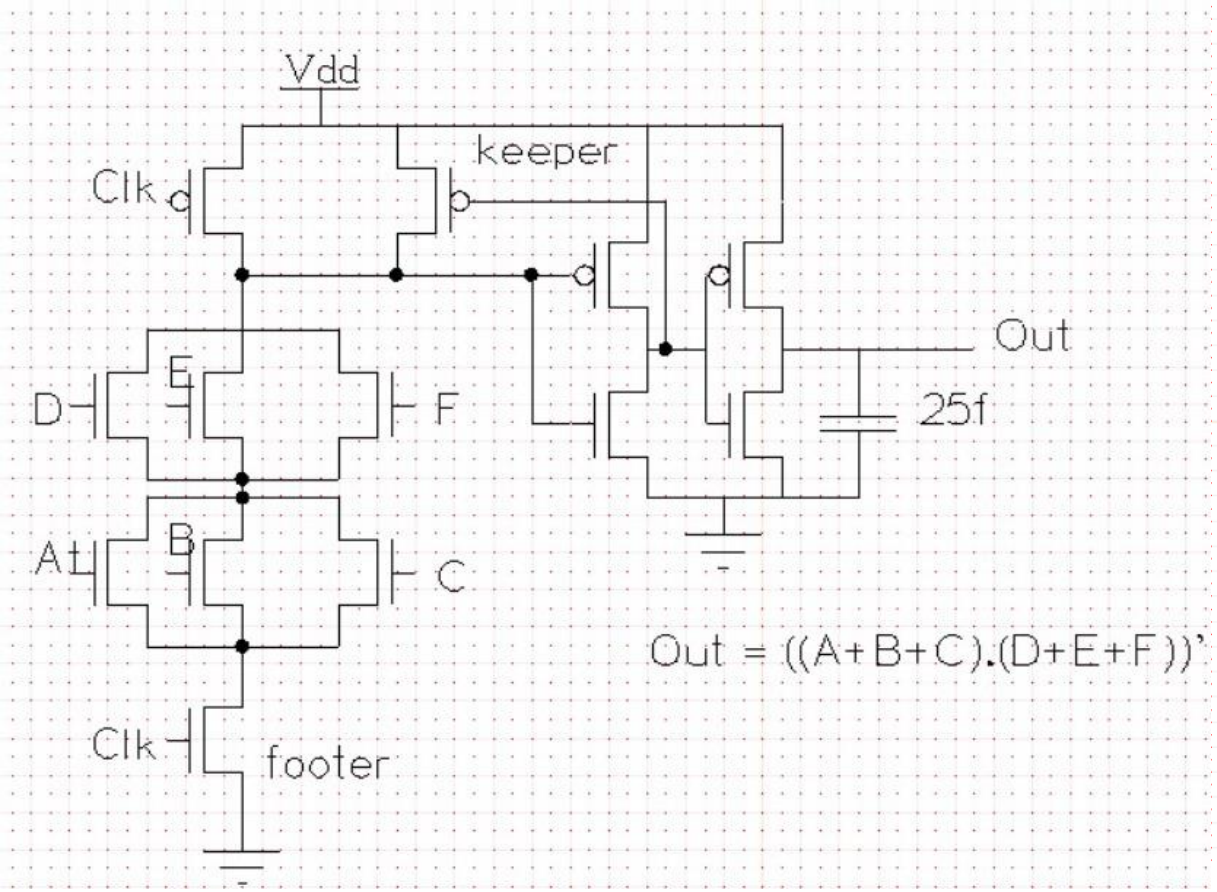
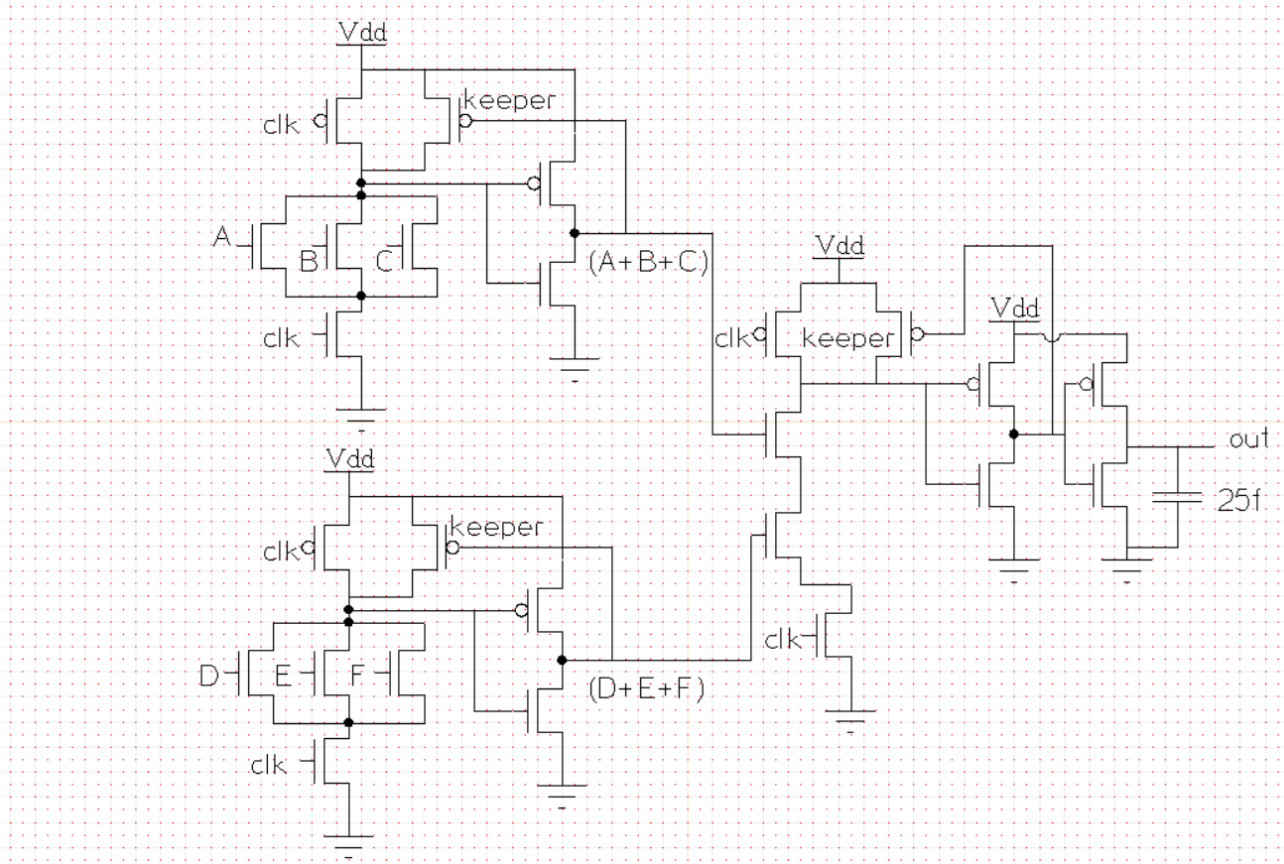
Schematic using XCircuit

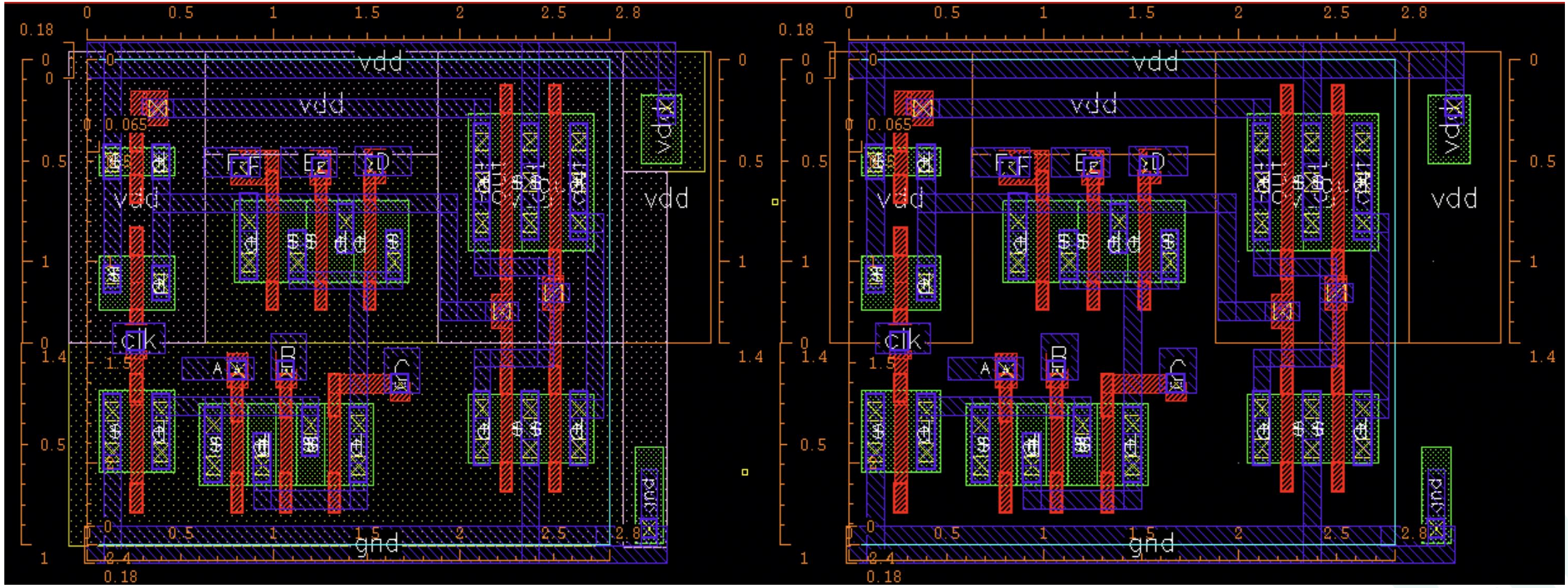
COMPLEX
Sizing- A, B, C, D, E, F ,clk (footer): 0.405u
clk(precharge): 0.27u, keeper: 0.135u
Inverters- nmos: 0.34u, pmos: 0.68u



NON COMPLEX
Sizing- keeper: 0.135u
A, B, C, D, E, F ,clk (footer), clk(precharge), A+B+C(nmos),
D+E+C(nmos) : 0.405u
Inverters- nmos: 0.34u, pmos: 0.68u

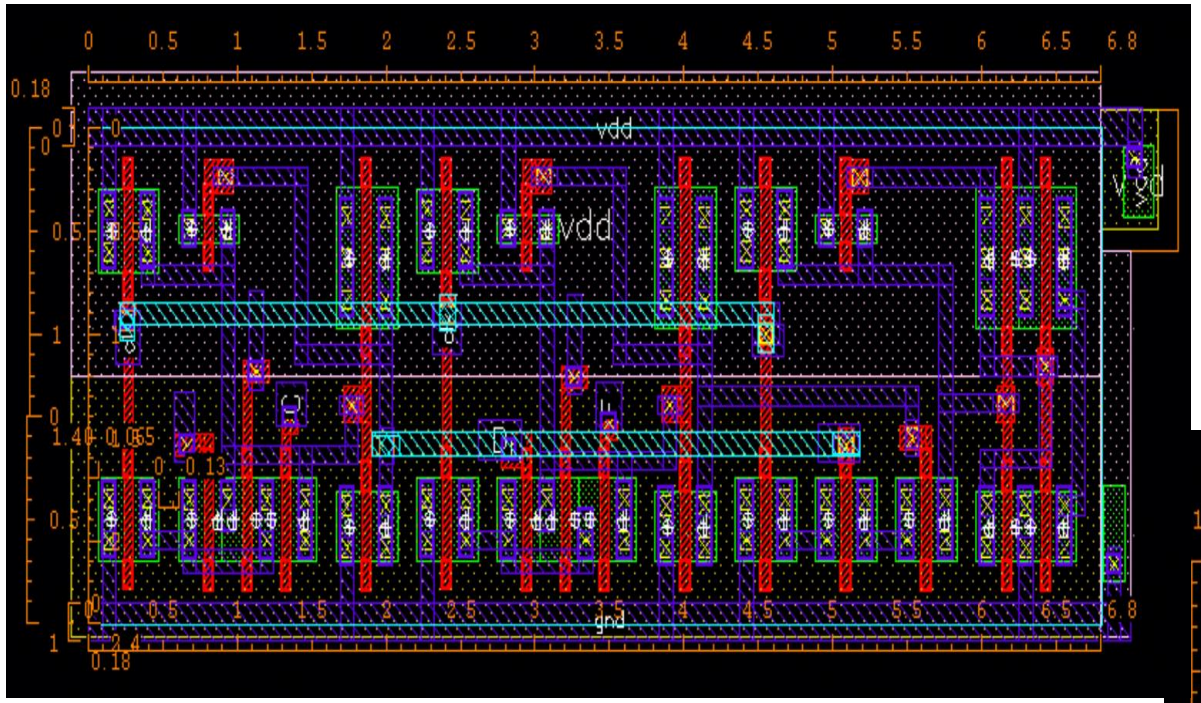


Layout Screenshots (Complex)

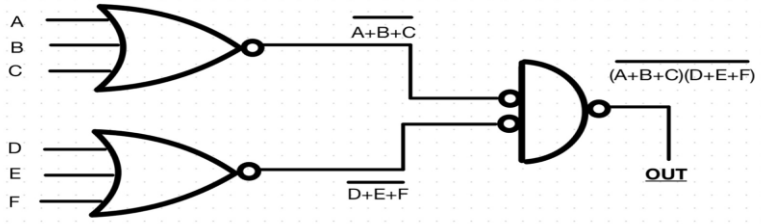


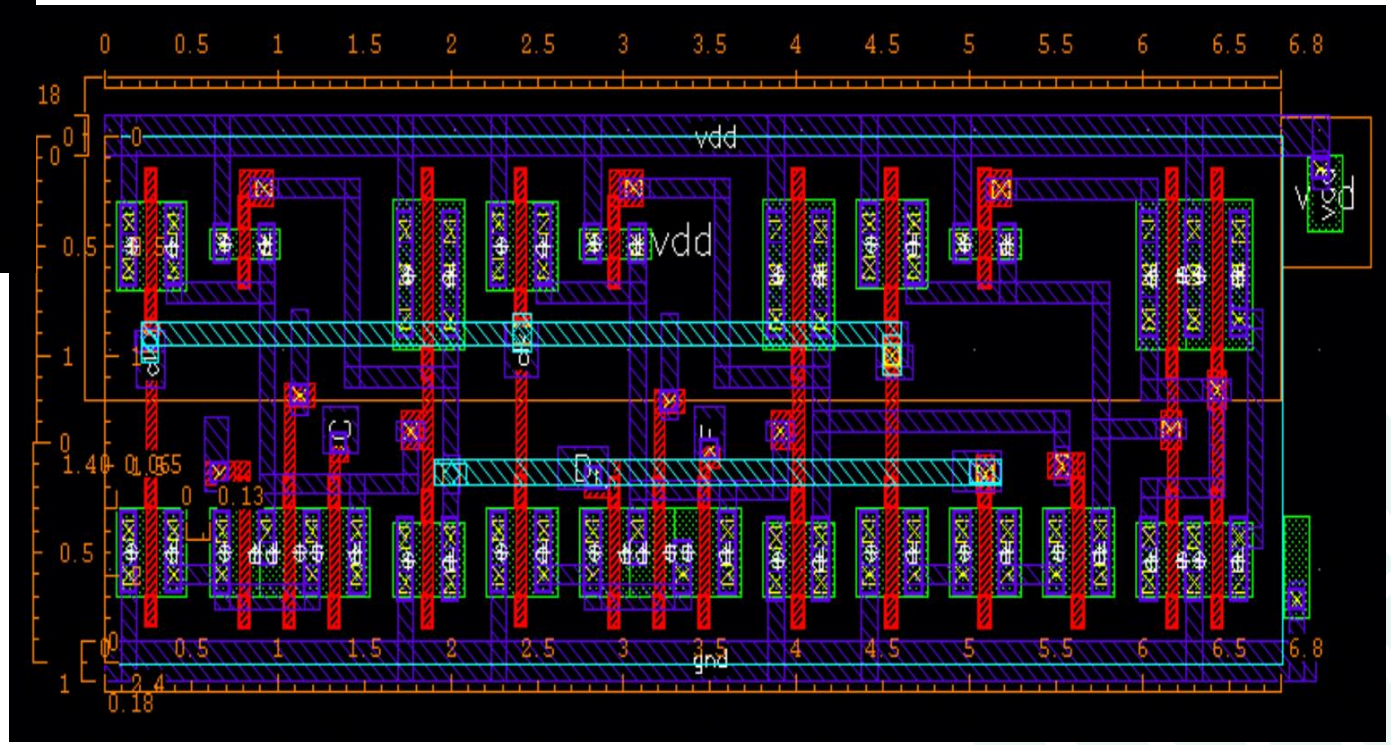
Area = 2.4*2.8 = 6.72 um^2

Layout Screenshots (Non-Complex)



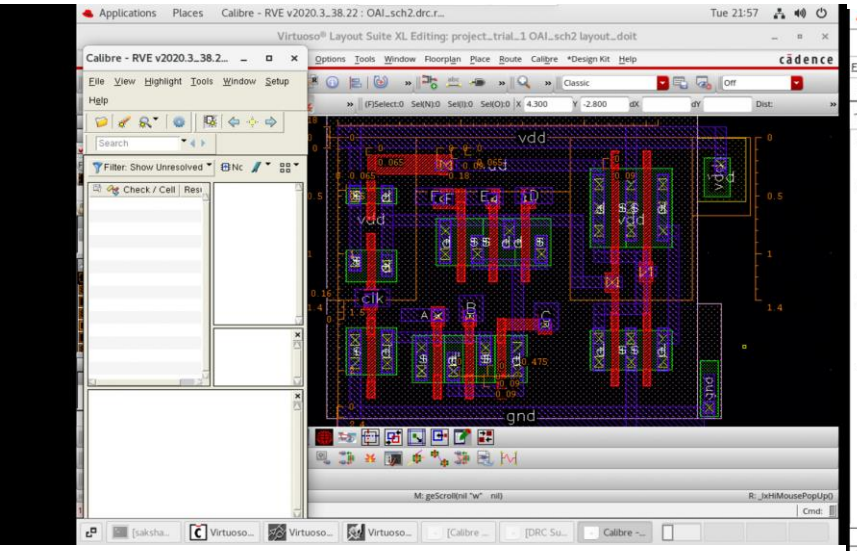
Area = 2.4*6.8 = 16.32 um^2

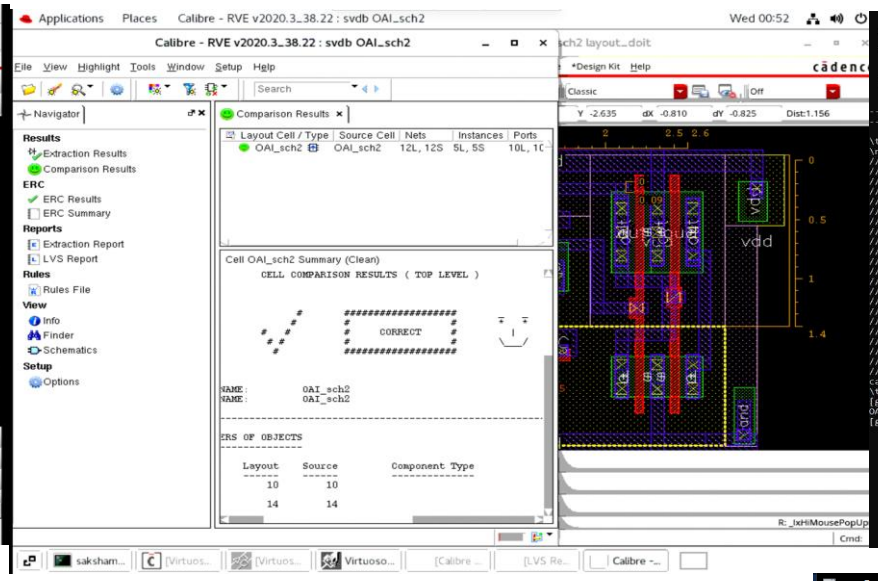


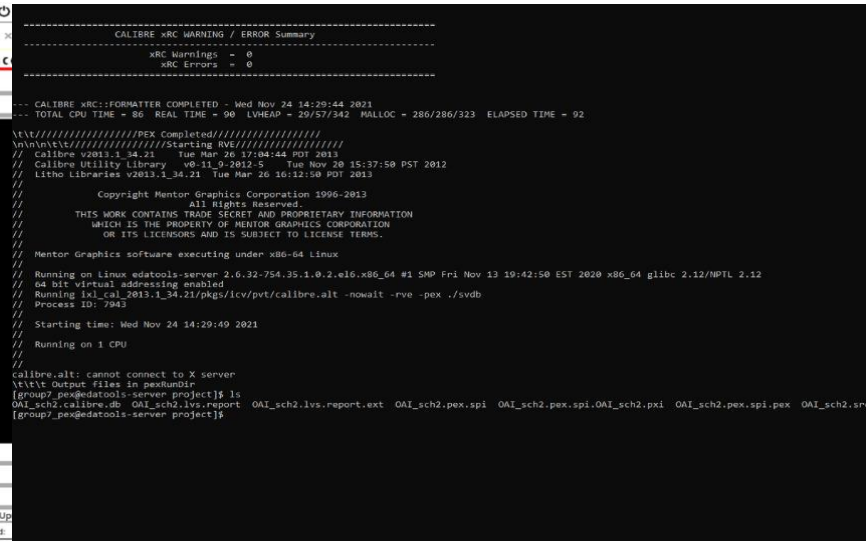


DRC, LVS, PEX Results

Complex







```
------------------------------------------------------------------------
                CALIBRE xRC WARNING / ERROR Summary
------------------------------------------------------------------------
                      xRC Warnings  =  0
                      xRC Errors    =  0
------------------------------------------------------------------------

--- CALIBRE xRC::FORMATTER COMPLETED - Wed Nov 24 14:29:44 2021
--- TOTAL CPU TIME = 86  REAL TIME = 90  LVHEAP = 29/57/342  MALLOC = 286/286/323  ELAPSED TIME = 92

\t\t//////////////////PEX Completed//////////////////
\n\n\n\t\t//////////////////Starting RVE//////////////////
//  Calibre v2013.1_34.21     Tue Mar 26 17:04:44 PDT 2013
//  Calibre Utility Library   v0-11_9-2012-5     Tue Nov 20 15:37:50 PST 2012
//  Litho Libraries v2013.1_34.21  Tue Mar 26 16:12:50 PDT 2013
//
//            Copyright Mentor Graphics Corporation 1996-2013
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//        THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//          WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//            OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under x86-64 Linux
//
//  Running on Linux edatools-server 2.6.32-754.35.1.0.2.el6.x86_64 #1 SMP Fri Nov 13 19:42:50 EST 2020 x86_64 glibc 2.12/NPTL 2.12
//  64 bit virtual addressing enabled
//  Running ixl_cal_2013.1_34.21/pkgs/icv/pvt/calibre.alt -nowait -rve -pex ./svdb
//  Process ID: 7943
//
//  Starting time: Wed Nov 24 14:29:49 2021
//
//  Running on 1 CPU
//
//
calibre.alt: cannot connect to X server
\t\t\t Output Files in pexRunDir
[group7_pex@edatools-server project]$ ls
OAI_sch2.calibre.db  OAI_sch2.lvs.report  OAI_sch2.lvs.report.ext  OAI_sch2.pex.spi  OAI_sch2.pex.spi.OAI_sch2.pxi  OAI_sch2.pex.spi.pex  OAI_sch2.sr
[group7_pex@edatools-server project]$
```
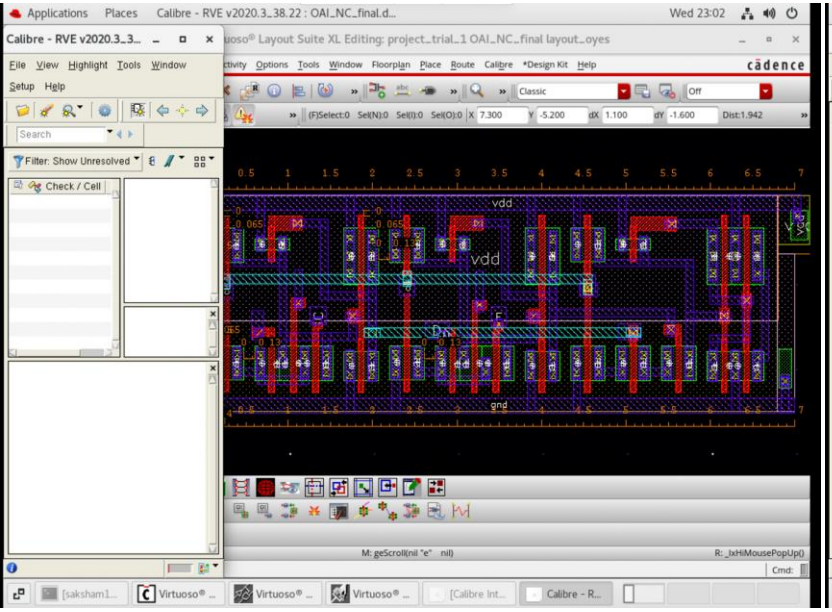
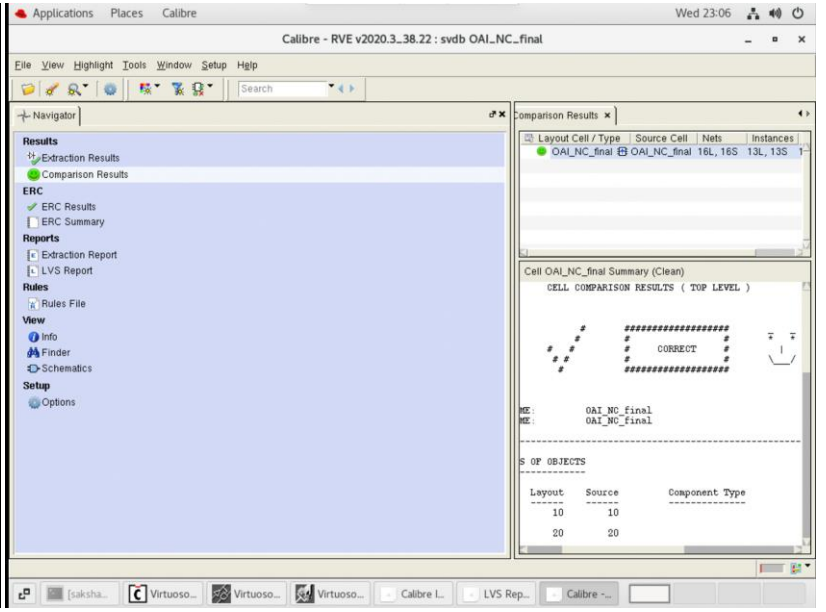
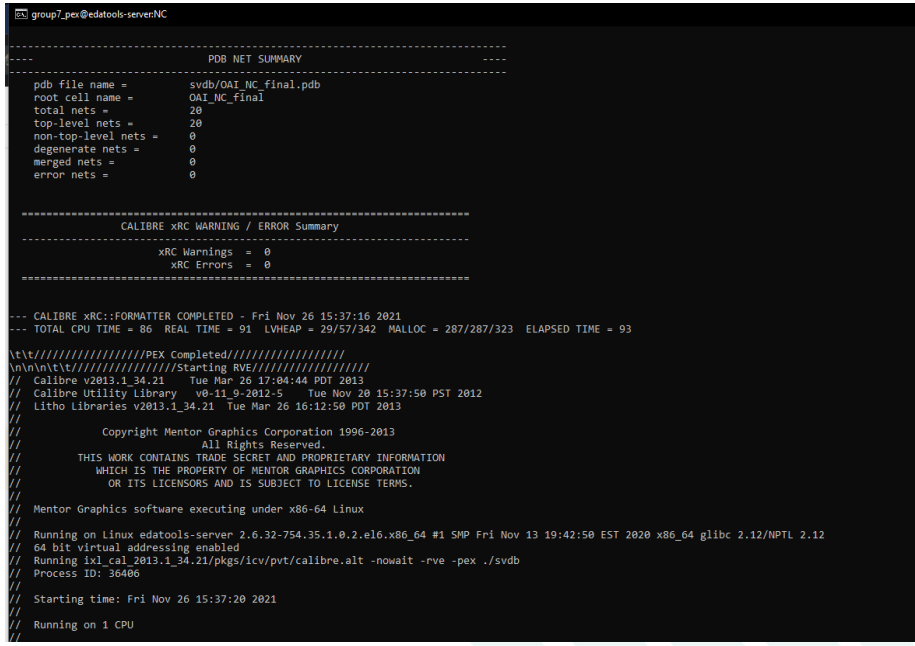

Non Complex







```
group7_pex@edatools-serverNC

------------------------------------------------------------------------
---                        PDB NET SUMMARY                           ---
------------------------------------------------------------------------
    pdb file name =         svdb/OAI_NC_final.pdb
    root cell name =        OAI_NC_final
    total nets =            20
    top-level nets =        20
    non-top-level nets =    0
    degenerate nets =       0
    merged nets =           0
    error nets =            0


  ======================================================================
                CALIBRE xRC WARNING / ERROR Summary
  ----------------------------------------------------------------------
                      xRC Warnings  =  0
                      xRC Errors    =  0
  ======================================================================


--- CALIBRE xRC::FORMATTER COMPLETED - Fri Nov 26 15:37:16 2021
--- TOTAL CPU TIME = 86  REAL TIME = 91  LVHEAP = 29/57/342  MALLOC = 287/287/323  ELAPSED TIME = 93

\t\t//////////////////PEX Completed//////////////////
\n\n\n\t\t//////////////////Starting RVE//////////////////
//  Calibre v2013.1_34.21     Tue Mar 26 17:04:44 PDT 2013
//  Calibre Utility Library   v0-11_9-2012-5     Tue Nov 20 15:37:50 PST 2012
//  Litho Libraries v2013.1_34.21  Tue Mar 26 16:12:50 PDT 2013
//
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//            OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under x86-64 Linux
//
//  Running on Linux edatools-server 2.6.32-754.35.1.0.2.el6.x86_64 #1 SMP Fri Nov 13 19:42:50 EST 2020 x86_64 glibc 2.12/NPTL 2.12
//  64 bit virtual addressing enabled
//  Running ixl_cal_2013.1_34.21/pkgs/icv/pvt/calibre.alt -nowait -rve -pex ./svdb
//  Process ID: 36406
//
//  Starting time: Fri Nov 26 15:37:20 2021
//
//  Running on 1 CPU
//
```
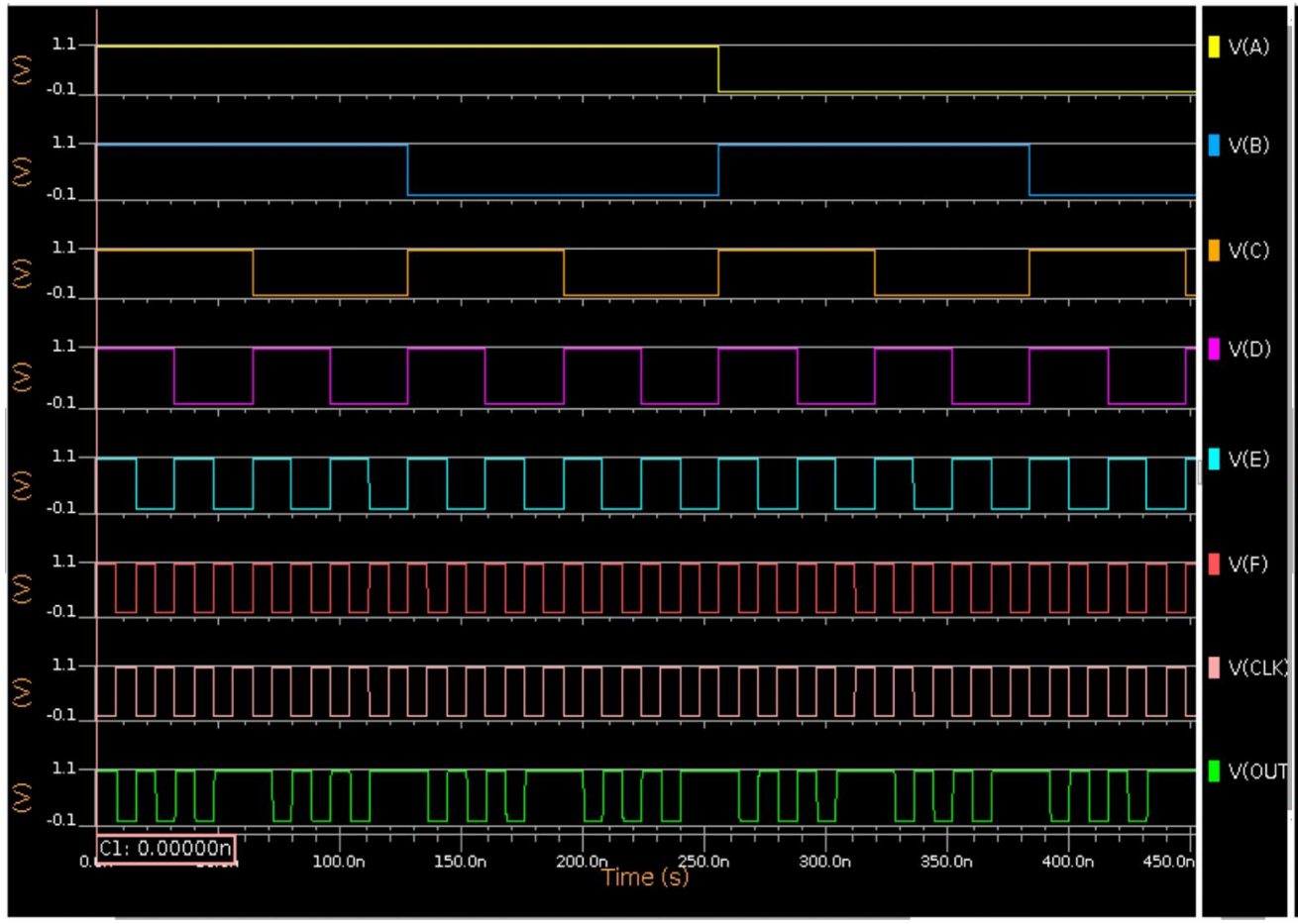
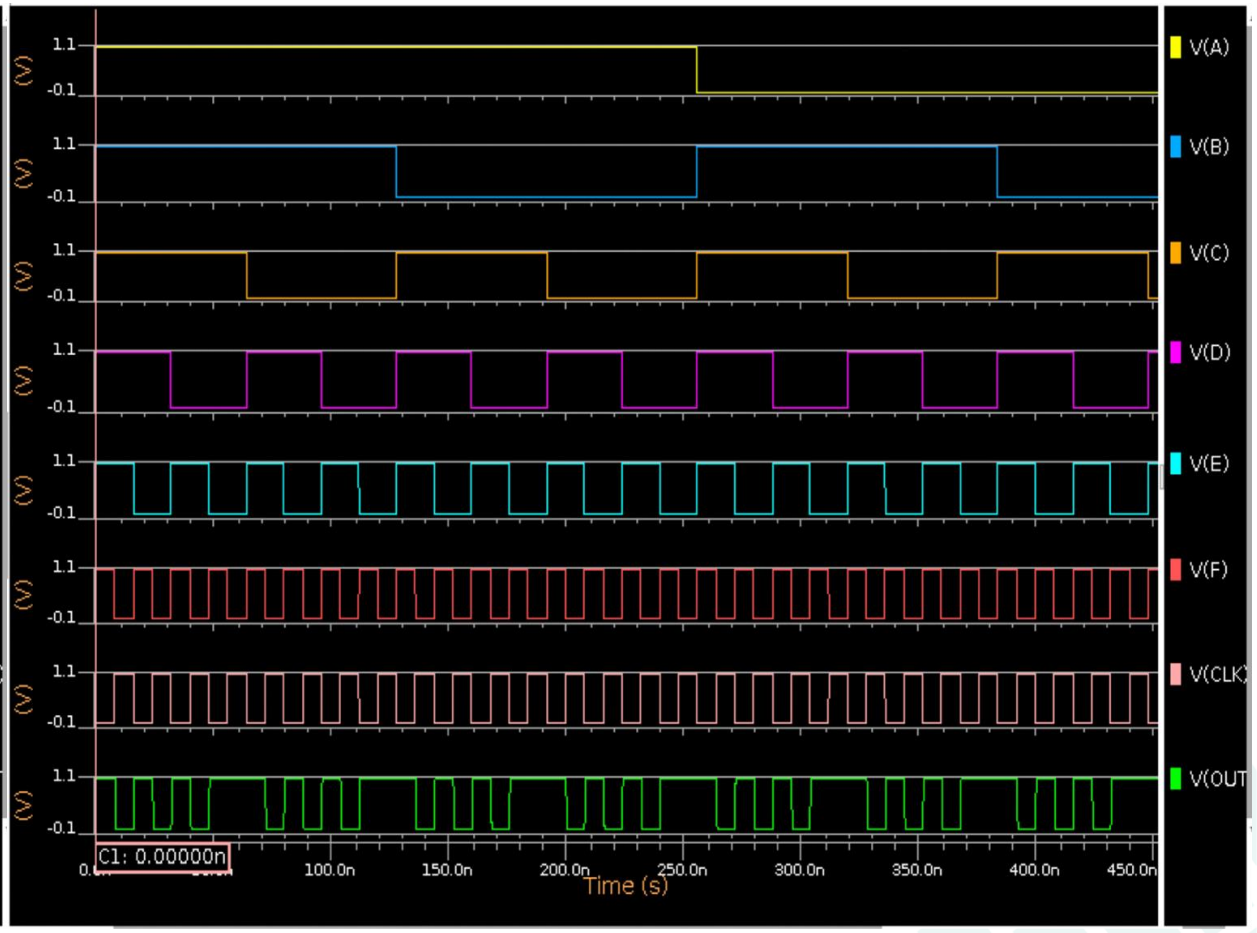

Simulation Waveforms

Complex



Non Complex



Same waveforms for both Complex and Non Complex Design verifies the functionality.

Complex–Pre & Post Layout

RISE AND FALL DELAYS

PVT CORNER ↓	T-fall (Pre-Layout)	T-fall (Post-Layout)	T-rise (Pre-Layout)	T-rise (Post-Layout)
SS, 1.08, 125	0.19676	0.19104	0.18563	0.1857
SS, 1.08, 25	0.17274	0.16806	0.1693	0.16947
SS, 1.08, -40	0.15475	0.15081	0.15409	0.15471
TT, 1.2, 25	0.11789	0.11541	0.12086	0.12134
FF, 1.32, 125	0.099496	0.097815	0.10355	0.10389
FF, 1.32, -40	0.07895	0.077754	0.083116	0.084044

Scale : Nano Seconds

Complex–Pre & Post Layout

CONTAMINATION AND PROPAGATION DELAYS

	Pre Condition (A,B,C,D,E,F): (1,1,1,0,0,0) Transition (D,E,F): (0->1)		Pre Condition (A,B,C,D,E,F): (0,0,0,0,0,1) Transition (C): (0->1)	
PVT CORNER	TCD (Pre-Layout)	TCD (Post-Layout)	TPD (Pre-Layout)	TPD (Post-Layout)
SS, 1.08, 125	0.23718	0.25207	0.32044	0.33923
SS, 1.08, 25	0.21462	0.22895	0.28825	0.30708
SS, 1.08, -40	0.19613	0.20946	0.25866	0.27682
TT, 1.2, 25	0.13817	0.14757	0.17409	0.18613
FF, 1.32, 125	0.10944	0.11670	0.13406	0.14322
FF, 1.32, -40	0.091383	0.097378	0.1067	0.11444

Scale : Nano Seconds

Non Complex–Pre & Post Layout

RISE AND FALL DELAYS

PVT CORNER	T-fall (Pre-Layout)	T-fall (Post-Layout)	T-rise (Pre-Layout)	T-rise (Post-Layout)
SS, 1.08, 125	0.19673	0.19139	0.18556	0.18528
SS, 1.08, 25	0.1727	0.16833	0.16931	0.16939
SS, 1.08, -40	0.15467	0.15104	0.15399	0.15479
TT, 1.2, 25	0.11788	0.11559	0.12079	0.12135
FF, 1.32, 125	0.099485	0.09799	0.10350	0.10389
FF, 1.32, -40	0.078937	0.07784	0.083098	0.084075

Scale : Nano Seconds

Non Complex–Pre & Post Layout

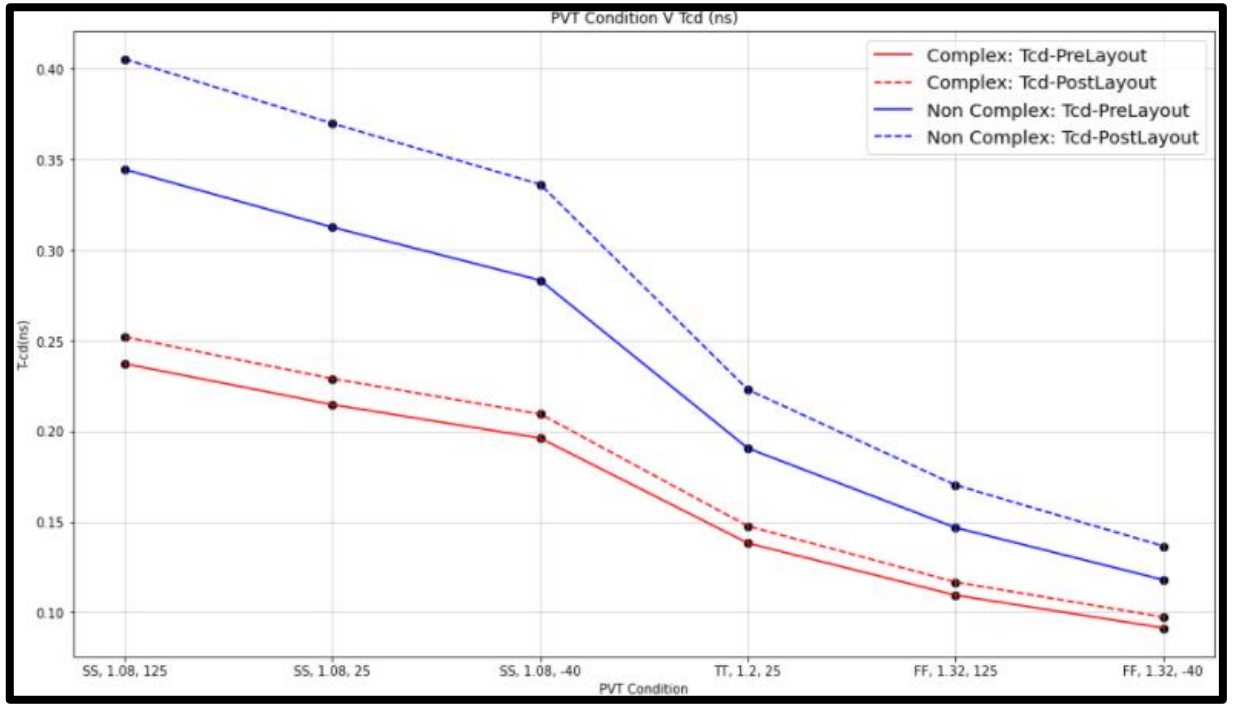
CONTAMINATION AND PROPAGATION DELAYS

PVT CORNER	TCD (Pre-Layout)	TCD (Post-Layout)	TPD (Pre-Layout)	TPD (Post-Layout)
SS, 1.08, 125	0.3444	0.40539	0.36448	0.42701
SS, 1.08, 25	0.31253	0.36982	0.33064	0.38931
SS, 1.08, -40	0.283283	0.33621	0.29953	0.35364
TT, 1.2, 25	0.19052	0.22288	0.19890	0.23232
FF, 1.32, 125	0.14672	0.17021	0.15198	0.17672
FF, 1.32, -40	0.11792	0.13656	0.12147	0.14106

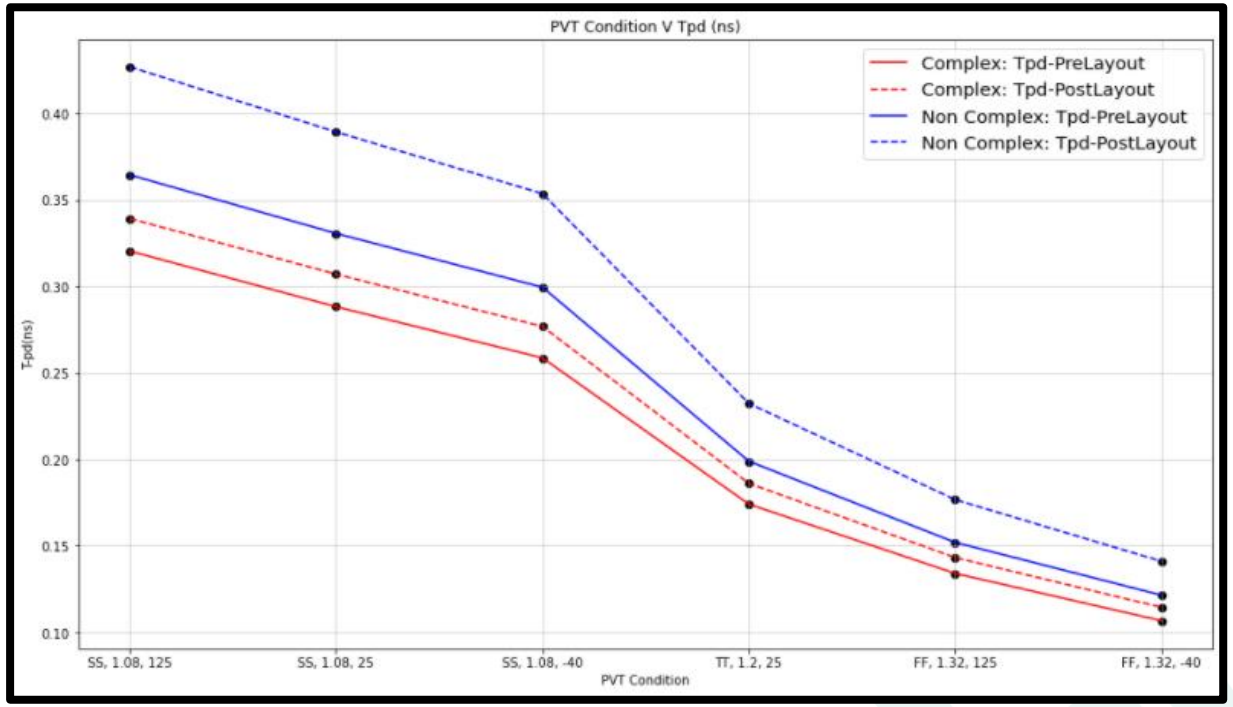
Scale : Nano Seconds

Delay Graphs

Contamination Delay



Propagation Delay



Complex Vs Non-Complex Design

	COMPLEX	NON COMPLEX	Remark
Number of Transistors	13	25	Increase in 12 transistors.
Area	6.72um^2	16.32um^2	2.42 times increase in area for non complex.
T_fall and T_rise	SS, 1.08, 125	SS, 1.08, 125	Not much change in T_rise and T_fall from complex to non complex
T_cd	FF, 1.32, -40	FF, 1.32, -40	Contamination delay increased in Non Complex by 16%
T_pd	SS, 1.08, 125	SS, 1.08, 125	Propagation delay increased in Non Complex by 17%

Leakage and Power Analysis

FF 1.32 125	COMPLEX		NON COMPLEX	
	Pre Layout	Post Layout	Pre Layout	Post Layout
Leakage	40.267 nA	46.778nA	229.36 nA	245.38 nA
Static Power	53.153 nW	61.74nW	302.76 nW	323.9016nW
Dynamic Power	6.1979 uW	6.557 uW	8.18 uW	8.6414 uW

- **Pre Layout vs Post Layout**
  - Not much change in Leakage and Power between pre and post layout simulations.

- **Complex vs Non Complex**
  - Leakage Current and Static Power increased 5 times from complex to non complex design.
  - Dynamic Power increased by 32% from complex to non complex design.

Worst PVT Corner: FF, 1.32, 125

PPA Analysis & Conclusion

- We have tried to minimize the area of our design and make a dense layout. Usage of shared diffusion in the nmos for the inputs and bending the nwell from between to accommodate nmos in the p-track region helped us reduce the area.
- We have also used shared diffusion regions for inverter in the domino logic to minimize the area.
- We have considered minimum DRCs wherever possible to reduce the overall horizontal width of our layout which in turn reduces area.
- Non Complex Logic uses more number of transistors and we found the delays increased as moved from complex to non complex designs.
- Complex Design is more power efficient than Non Complex Design.

ACKNOWLEDGMENT

Work Distribution

- **Complex Schematic:** Samaksh, Saksham
- **Complex Layout:** Samaksh, Saksham
- **Non Complex Schematic:** Sidharth, Mihir
- **Non Complex Layout:** Saksham, Samaksh, Sidharth
- **Eldo Scripting:** Mihir, Saksham, Samaksh, Sidharth
- **Simulations:** Samaksh, Saksham, Mihir
- **Graphs and Tables:** Sidharth
- **XCircuit and WaveDrom:** Mihir