

ASSIGNMENT 8

Samaksh Gupta
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RTL

```
module top (input clk, input rst, input [31:0] in1, input [31:0] in2, input control, output reg [31:0] out);

    reg [31:0] in1_stage1;
    reg [31:0] in2_stage1;
    reg [31:0] in1_stage2;
    reg [31:0] in2_stage2;

    always @(posedge clk) begin
        in1_stage1 <= in1;
        in2_stage1 <= in2;
    end

    always @(posedge clk) begin
        if(rst) begin in1_stage2 <= 0; end
        else begin
            if(control) begin in1_stage2 <= in1_stage1;
        end
    end
    end
    end

    always @(posedge clk) begin
        if(rst) begin in2_stage2 <= 0; end
        else begin
            if(control) begin in2_stage2 <= in2_stage1;
        end
    end
    end
    end

    always @(*) begin
        out = (in1_stage2 & in2_stage2) ^ 32'b1;
    end
endmodule
```

Instance Report (Yosys) {All constraints met}

```
14. Printing statistics.

==== top ===

    Number of wires:          330
    Number of wire bits:      547
    Number of public wires:   10
    Number of public wire bits: 227
    Number of memories:      0
    Number of memory bits:    0
    Number of processes:      0
    Number of cells:          352
        AND2_X1                31
        A0I211_X1               64
        DFF_X1                 128
        INV_X1                  64
        NAND2_X1                 1
        NOR2_X1                  64

Chip area for module '\top': 782.838000
```

Yosys Script

```
# reading the design using the Verilog frontend (icarus Verilog)
# read_verilog : Load modules from a Verilog file to the current design
#NOTE: in case of multiple .v files each file should be read individually
read_verilog top.v

# convert high-level behavioral parts ("processes") to d-type flip-flops and muxes
proc
# perform some simple optimizations
opt

# Resource Sharing
# share -force
show

# convert high-level memory constructs to d-type flip-flops and multiplexers
memory
opt

# convert design to (logical) gate-level netlists
techmap
opt

# technology mapping of flip-flops
#Map internal flip-flop cells to the flip-flop cells in the technology library specified in the given liberty file.
#dfflibmap -liberty NanGate_15nm_OCL_worst_low_conditional_nldm.lib
dfflibmap -liberty ../../libraries/Nangate45_typ.lib
opt

# use ABC to map remaining logic to cells from the cell library
abc -liberty ../../libraries/Nangate45_typ.lib
# abc -liberty NanGate_15nm_OCL_worst_low_conditional_nldm.lib
opt

# Print statistics
stat -liberty ../../libraries/Nangate45_typ.lib
# stat -liberty NanGate_15nm_OCL_worst_low_conditional_nldm.lib
# write synthesized design
write_verilog synth.v

#Create a graphviz DOT file
show
```

Netlist

The netlist is around 60 pages. Please click on 'Link' below to open the generated netlist.

[Link](#)

Constraints File

```
create_clock -name clk -period 5.0 [get_ports "clk"]
set_propagated_clock [get_clocks "clk"]
set_clock_transition -rise 0.05 [get_clocks "clk"]
set_clock_transition -fall 0.05 [get_clocks "clk"]
set_clock_uncertainty 0.05 [get_clocks "clk"]
set_clock_latency 0.05 [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "rst"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "rst"] -clock [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "in1"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "in1"] -clock [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "in2"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "in2"] -clock [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "control"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "control"] -clock [get_clocks "clk"]

set_input_transition -max 0.02 [get_ports rst]
set_input_transition -min 0.01 [get_ports rst]

set_input_transition -max 0.02 [get_ports in1]
set_input_transition -min 0.01 [get_ports in1]

set_input_transition -max 0.02 [get_ports in2]
set_input_transition -min 0.01 [get_ports in2]

set_input_transition -max 0.02 [get_ports control]
set_input_transition -min 0.01 [get_ports control]

set_output_delay -max 1.5 [get_ports "out"] -clock [get_clocks "clk"]
set_output_delay -min 0.8 [get_ports "out"] -clock [get_clocks "clk"]

#####
#This constraints file is structured in the similar way, I used for the course group project.
~
```

Die and Core Area

```
# gcd flow pipe cleaner
source "helpers.tcl"
source "flow_helpers.tcl"
source "Nangate45/Nangate45.vars"

set design "top"
set top_module "top"
set synth_verilog "synth.v"
set sdc_file "gcd_nangate45_2.sdc"
set die_area {0 0 90.13 90.8}
set core_area {10.07 11.2 85.25 81}

source -echo "flow.tcl"
~
```

Flow Script

- Pin Placement Command (random)

```
#####
# IO Placement (random)
place_pins -random -hor_layers $io_placer_hor_layer -ver_layers $io_placer_ver_layer
```

- Timing Report Generation Command

```
report_checks -path_delay min_max -format full_clock_expanded \
    -fields {input_pin slew capacitance} -digits 3
report_worst_slack -min -digits 3
report_worst_slack -max -digits 3
report_tns -digits 3
report_check_types -max_slew -max_capacitance -max_fanout -violators -digits 3
report_clock_skew -digits 3
report_power -corner $power_corner

report_floating_nets -verbose
report_design_area

utl::metric "worst_slack_min" [sta::worst_slack -min]
utl::metric "worst_slack_max" [sta::worst_slack -max]
utl::metric "tns_max" [sta::total_negative_slack -max]
utl::metric "clock_skew" [sta::worst_clock_skew -setup]
utl::metric "max_slew_violations" [sta::max_slewViolationCount]
utl::metric "max_fanout_violations" [sta::max_fanoutViolationCount]
utl::metric "max_capacitance_violations" [sta::max_capacitanceViolationCount]
# report clock period as a metric for updating limits
utl::metric "clock_period" [get_property [lindex [all_clocks] 0] period]
```

- Macro Placement | Tapcell Insertion | Power Planning Command

```
#####
# Macro Placement
if { [have_macros] } {
    global_placement -density $global_place_density
    macro_placement -halo $macro_place_halo -channel $macro_place_channel
}

#####
# Tapcell insertion
eval tapcell $tapcell_args

#####
# Power distribution network insertion
pdngen -verbose $pdn_cfg
```

- **Global Placement Command**

```
#####
# Global placement

foreach layer_adjustment $global_routing_layer_adjustments {
    lassign $layer_adjustment layer adjustment
    set_global_routing_layer_adjustment $layer $adjustment
}
set_routing_layers -signal $global_routing_layers \
    -clock $global_routing_clock_layers
set_macro_extension 2

global_placement -routability_driven -density $global_place_density \
    -pad_left $global_place_pad -pad_right $global_place_pad

# IO Placement
place_pins -hor_layers $io_placer_hor_layer -ver_layers $io_placer_ver_layer

# checkpoint
set_global_place_def [make_result_file ${design}_${platform}_global_place.def]
write_def $global_place_def
```

- **Repair Command**

```
#####
# Repair max slew/cap/fanout violations and normalize slews

source $layer_rc_file
set_wire_rc -signal -layer $wire_rc_layer
set_wire_rc -clock -layer $wire_rc_layer_clk
set_dont_use $dont_use

estimate_parasitics -placement

repair_design -slew_margin $slew_margin -cap_margin $cap_margin

repair_tie_fanout -separation $tie_separation $tie_lo_port
repair_tie_fanout -separation $tie_separation $tie_hi_port

set_placement_padding -global -left $detail_place_pad -right $detail_place_pad
detailed_placement

# post resize timing report (ideal clocks)
report_worst_slack -min -digits 3
report_worst_slack -max -digits 3
report_tns -digits 3
# Check slew repair
report_check_types -max_slew -max_capacitance -max_fanout -violators
```

```
#####
# Setup/hold timing repair

set_propagated_clock [all_clocks]

set_repair_timing_use_grt_parasitics 0
if { $repair_timing_use_grt_parasitics } {
    # Global route for parasitics - no guide file required
    global_route -congestion_iterations 100
    estimate_parasitics -global_routing
} else {
    estimate_parasitics -placement
}

repair_timing

# Post timing repair.
report_worst_slack -min -digits 3
report_worst_slack -max -digits 3
report_tns -digits 3
```

- Clock Tree Synthesis

```
#####
# Clock Tree Synthesis

# Clone clock tree inverters next to register loads
# so cts does not try to buffer the inverted clocks.
repair_clock_inverters

clock_tree_synthesis -root_buf $cts_buffer -buf_list $cts_buffer -sink_clustering_enable

# CTS leaves a long wire from the pad to the clock tree root.
repair_clock_nets

# place clock buffers
detailed_placement

# checkpoint
set cts_def [make_result_file ${design}_${platform}_cts.def]
write_def $cts_def
```

- Detailed Placement

```
#####
# Detailed Placement (final)

detailed_placement
# Capture utilization before fillers make it 100%
utl::metric "utilization" [format %.1f [expr [rsz::utilization] * 100]]
utl::metric "design_area" [sta::format_area [rsz::design_area] 0]
filler_placement $filler_cells
check_placement -verbose
```

- Global Routing

```
#####
# Global routing

pin_access
set_route_guide [make_result_file ${design}_${platform}.route_guide]
global_route -guide_file $route_guide \
    -congestion_iterations 100

set antenna_report [make_result_file ${design}_${platform}_ant.log]
set antenna_errors [check_antennas -report_violating_nets -report_file $antenna_report]

utl::metric "ANT::errors" $antenna_errors

if { $antenna_errors > 0 } {
    fail "found $antenna_errors antenna violations"
}

set verilog_file [make_result_file ${design}_${platform}.v]
write_verilog -remove_cells $filler_cells $verilog_file
```

- **Detailed Routing**

```
#####
# Detailed routing

set_thread_count [exec getconf_NPROCESSORS_ONLN]
detailed_route -guide $route_guide \
    -output_guide [make_result_file "${design}_${platform}_output_guide.mod"] \
    -output_drc [make_result_file "${design}_${platform}_route_drc.rpt"] \
    -output_maze [make_result_file "${design}_${platform}_maze.log"] \
    -verbose 0

set drv_count [detailed_route_num_drvs]
utl::metric "DRT::drv" $drv_count

set routed_def [make_result_file ${design}_${platform}_route.def]
write_def $routed_def
```

- **Extraction after Global Routing**

```
#####
# Extraction

if { $rcx_rules_file != "" } {
    define_process_corner -ext_model_index 0 X
    extract_parasitics -ext_model_file $rcx_rules_file

    set spef_file [make_result_file ${design}_${platform}.spef]
    write_spef $spef_file

    read_spef $spef_file
} else {
    # Use global routing based parasitics inlieu of rc extraction
    estimate_parasitics -global_routing
}
```

2. Floor Planning

```
# Assumes flow_helpers.tcl has been read.
read_libraries
read_verilog $synth_verilog
link design $top_module
read_sdc $sdc_file

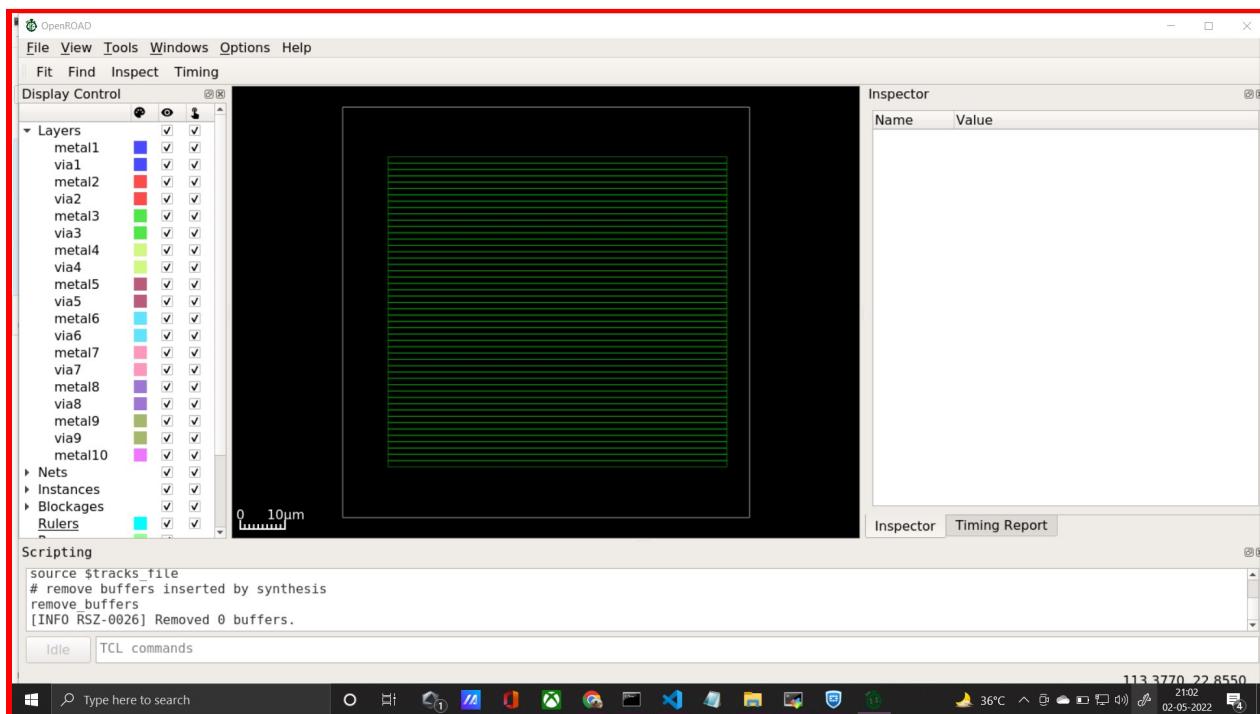
util::metric "ord_version" [ord::openroad_git_describe]
# Note that sta::network_instance_count is not valid after tapcells are added.
util::metric "instance_count" [sta::network_instance_count]

initialize_floorplan -site $site \
    -die_area $die_area \
    -core_area $core_area

source $tracks_file

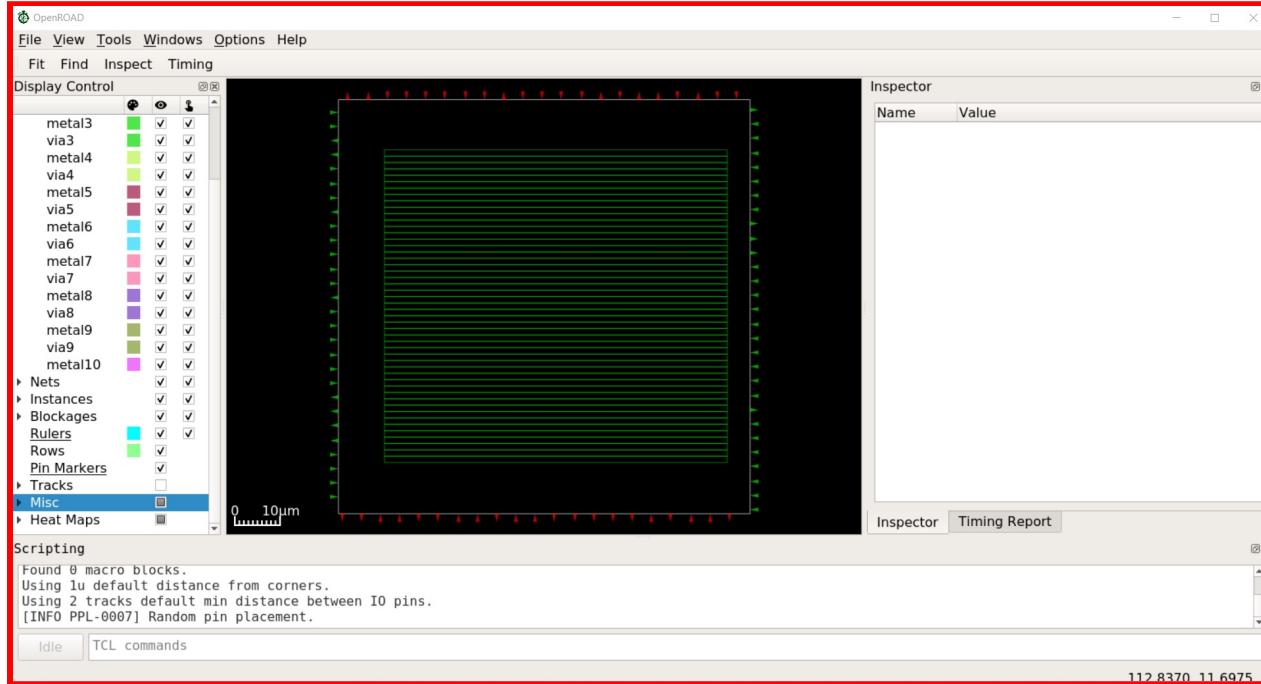
# remove buffers inserted by synthesis
remove_buffers
```

Die and Core Area have been defined before (Pg-3)

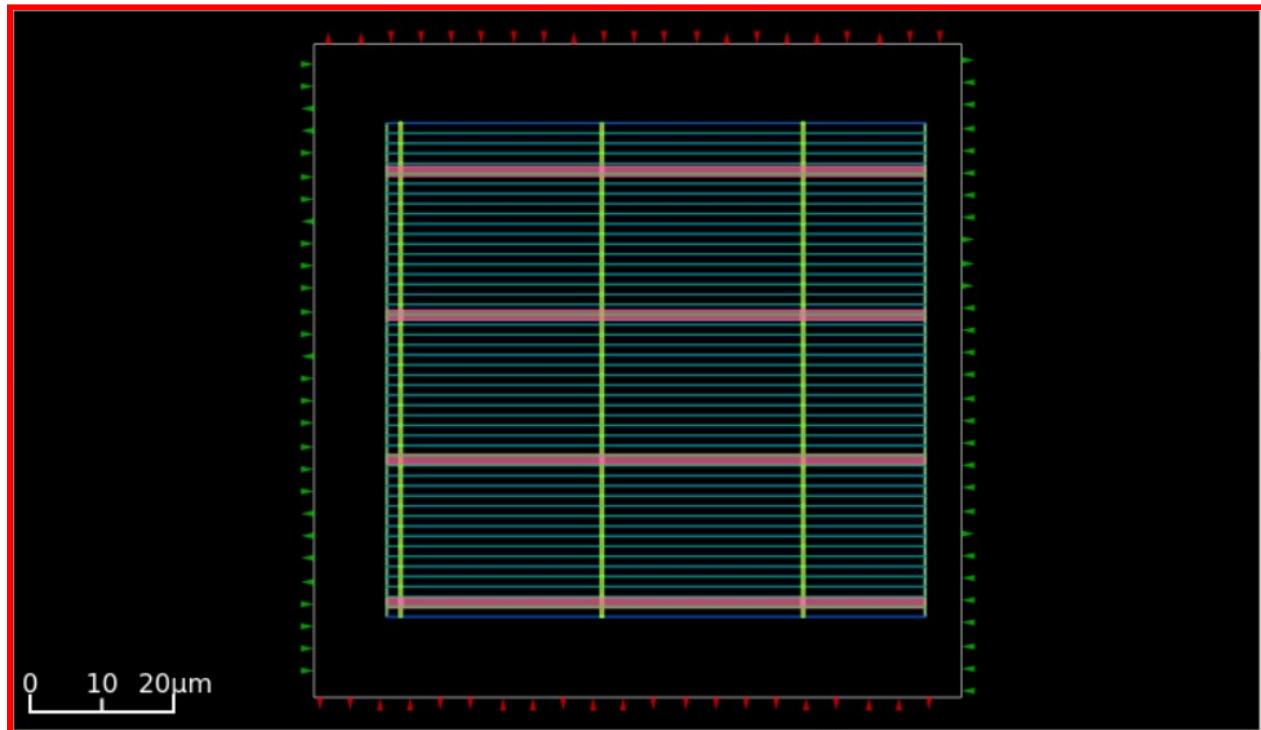


3. Pin Placement (Random)

~Command Shown Before



4. Power Planning



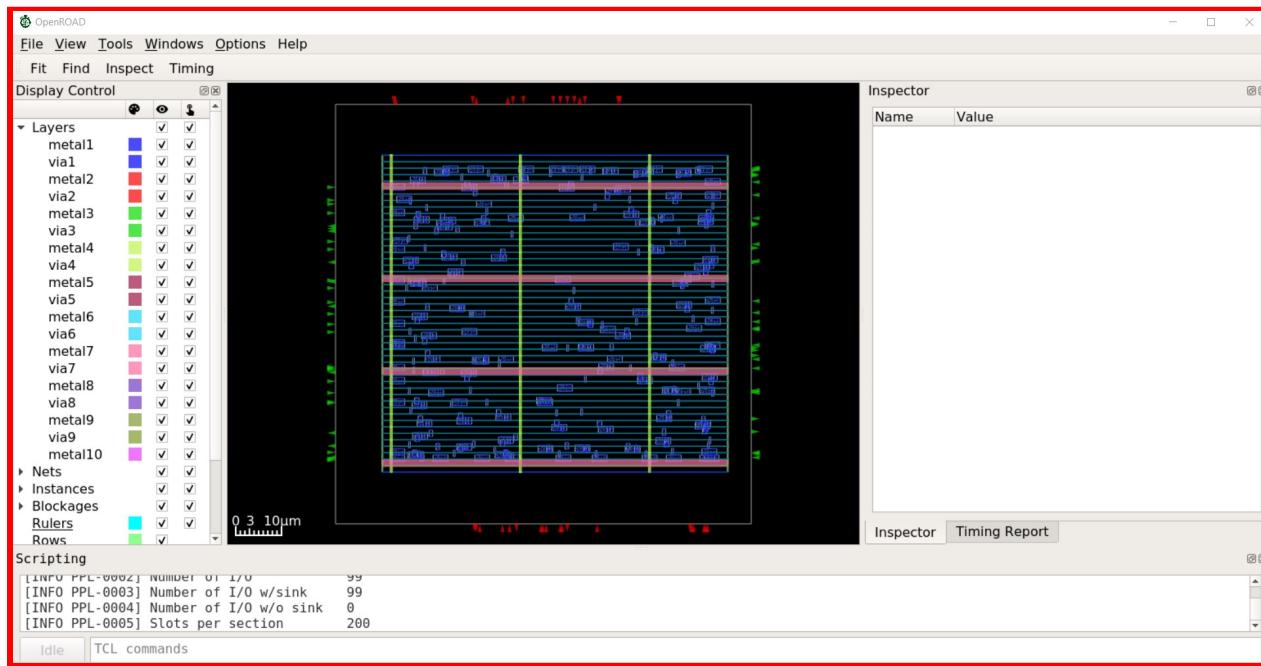
M1, M4, M7 have been used

```
Scripting
[INFO PDN-0016] Power Delivery Network Generator: Generating PDN
    config: Nangate45/Nangate45.pdn
[INFO PDN-0008] Design name is top.
[INFO PDN-0009] Reading technology data.
[INFO PDN-0011] ***** INFO *****
Type: stdcell, grid
    Stdcell Rails
        Layer: metall1 - width: 0.170 pitch: 2.400 offset: 0.000
    Straps
        Layer: metal4 - width: 0.480 pitch: 56.000 offset: 2.000
```

```
Type: stdcell, grid
Stdcell Rails
    Layer: metall1 - width: 0.170 pitch: 2.400 offset: 0.000
Straps
    Layer: metal4 - width: 0.480 pitch: 56.000 offset: 2.000
    Layer: metal7 - width: 1.400 pitch: 40.000 offset: 2.000
Connect: {metall1 metal4} {metal4 metal7}
```

5. Placement (Global, Legalization, Detailed)

a. Global



Timing Analysis after Global Placement

Hold Slack= 0.058

```
# checkpoint
set_global_place_def [make_result_file ${design}_${platform}_global_place.def]
write_def $global_place_def
report_checks -path_delay min_max -format full_clock_expanded \
-fields {input_pin slew capacitance} -digits 3
Startpoint: _640_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _544_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Cap Slew Delay Time Description
-----
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
1.859 0.007 0.094 0.144 v _640_/Q (DFF_X1)
0.007 0.000 0.144 v _320_/A (INV_X1)
1.965 0.007 0.012 0.156 ^ _320_/ZN (INV_X1)
0.007 0.000 0.156 ^ _385_/C1 (AOI211_X1)
1.372 0.007 0.013 0.169 v _385_/ZN (AOI211_X1)
0.007 0.000 0.169 v _544_/D (DFF_X1)
0.169 v _544_/D (DFF_X1)
0.169 v _544_/D (DFF_X1)
0.169 data arrival time

0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.100 0.100 clock uncertainty
0.000 0.100 0.100 clock reconvergence pessimism
0.100 ^ _544_/CK (DFF_X1)
0.011 0.111 0.111 library hold time
0.111 data required time
0.111 data required time
-0.169 data arrival time
-----
0.058 slack (MET)
```

Setup Slack= 3.319

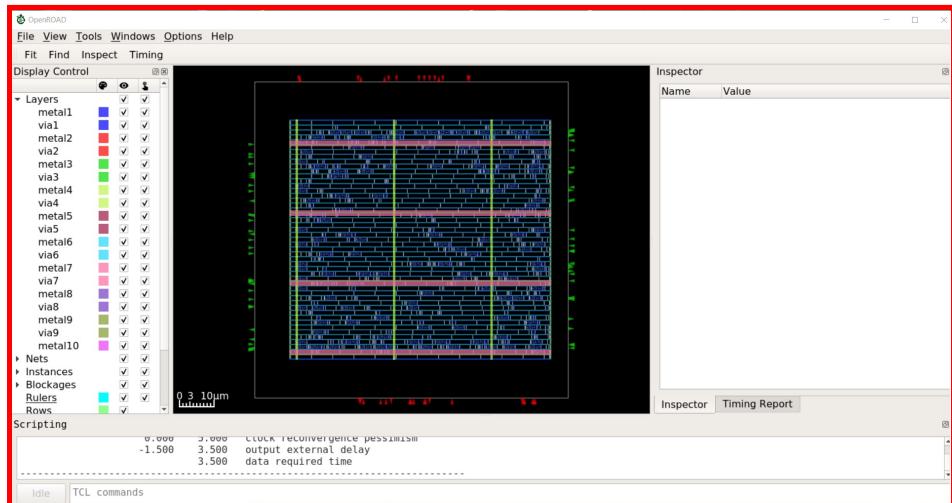
```
Startpoint: _586_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: out[10] (output port clocked by clk)
Path Group: clk
Path Type: max

Cap Slew Delay Time Description
-----
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
3.325 0.050 0.000 0.050 ^ _586_/CK (DFF_X1)
0.011 0.103 0.153 ^ _586_/Q (DFF_X1)
0.011 0.000 0.153 ^ _521_/A2 (AND2_X1)
0.310 0.006 0.027 0.181 ^ _521_/ZN (AND2_X1)
0.006 0.000 0.181 ^ out[10] (out)
0.181 data arrival time

0.050 5.000 5.000 clock clk (rise edge)
0.050 5.050 5.050 clock network delay (ideal)
-0.050 5.000 5.000 clock uncertainty
0.000 5.000 5.000 clock reconvergence pessimism
-1.500 3.500 3.500 output external delay
3.500 data required time
3.500 data required time
3.500 data required time
-0.181 data arrival time
-----
3.319 slack (MET)
```

Both Hold and Setup slacks are positive. We have no violation post placement in the design.

b. Detailed Placement



Timing Analysis after Detailed Placement

Hold Slack= 0.058

```

Startpoint: 640 (rising edge-triggered flip-flop clocked by clk)
Endpoint: 544 (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Cap Slew Delay Time Description
-----+
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.000 0.050 ^ 640 /CK (DFF_X1)
1.859 0.007 0.094 0.144 v _640 /0 (DFF_X1)
0.007 0.000 0.144 v _320 /A (INV_X1)
1.965 0.007 0.012 0.156 ^ _320 /ZN (INV_X1)
0.007 0.000 0.156 ^ _385 /C1 (AOI211_X1)
1.372 0.007 0.013 0.169 v _385 /ZN (AOI211_X1)
0.007 0.000 0.169 v 544 /0 (DFF_X1)
0.169 data arrival time

0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.100 0.100 clock uncertainty
0.000 0.100 0.100 clock reconvergence pessimism
0.100 ^ 544 /CK (DFF_X1)
0.011 0.111 library hold time
0.011 data required time

0.111 data required time
-0.169 data arrival time

0.058 slack (MET)
-----+

```

Setup Slack= 3.319

```

Startpoint: 586 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out[10] (output port clocked by clk)
Path Group: clk
Path Type: max

Cap Slew Delay Time Description
-----+
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.000 0.050 ^ 586 /CK (DFF_X1)
3.325 0.011 0.103 0.153 ^ 586 /0 (DFF_X1)
0.011 0.000 0.153 ^ _521 /A2 (AND2_X1)
0.310 0.006 0.027 0.181 ^ _521 /ZN (AND2_X1)
0.006 0.000 0.181 ^ out[10] (out)
0.181 data arrival time

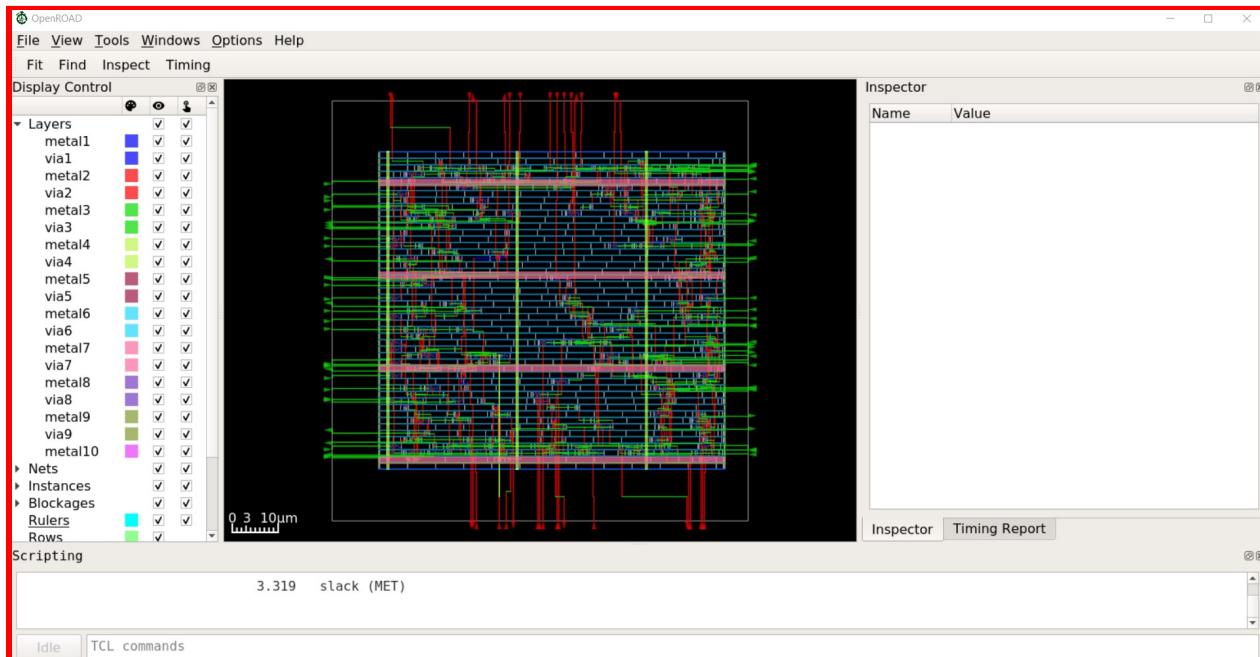
0.050 5.000 5.000 clock clk (rise edge)
0.050 5.050 5.050 clock network delay (ideal)
-0.050 5.000 5.000 clock uncertainty
0.000 5.000 5.000 clock reconvergence pessimism
-1.500 3.500 3.500 output external delay
3.500 data required time

3.500 data required time
-0.181 data arrival time

3.319 slack (MET)
-----+

```

Global + Detailed Routing



Power and Area Report

```
report_power -corner $power_corner
Group           Internal Power   Switching Power   Leakage Power   Total Power
-----  
Sequential      1.28e-04    4.89e-06    1.01e-05    1.43e-04    49.8%  
Combinational   7.11e-05    6.58e-05    6.75e-06    1.44e-04    50.2%  
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%  
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%  
-----  
Total          1.99e-04    7.07e-05    1.69e-05    2.87e-04    100.0%
```

```
report_floating_nets -verbose
report_design_area
Design area 814 u^2 16% utilization.
```

Timing Report

Hold Slack= 0.05

```
#####
# Final Report
report checks -path_delay min_max -format full_clock_expanded \
-fields {input_pin slew capacitance} -digits 3
Startpoint: in2[10] (input port clocked by clk)
Endpoint: _650_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min
Cap Slew Delay Time Description
-----
0.000 0.000 clock clk (rise edge)
0.000 0.000 clock network delay (propagated)
0.200 0.200 ^ input external delay
1.981 0.010 0.000 0.200 ^ in2[10] (in)
0.010 0.000 0.200 ^ _650_/D (DFF_X1)
0.200 0.200 data arrival time
0.000 0.000 clock clk (rise edge)
0.000 0.000 clock source latency
8.453 0.000 0.000 ^ clk (in)
0.001 0.001 0.001 ^ clkbuf_0_clk/A (BUF_X4)
67.012 0.020 0.052 0.053 ^ clkbuf_0_clk/Z (BUF_X4)
0.039 0.003 0.057 ^ clkbuf_4.5_0_clk/A (BUF_X4)
15.574 0.012 0.033 0.089 ^ clkbuf_4.5_0_clk/Z (BUF_X4)
0.012 0.001 0.090 ^ _650_/CK (DFF_X1)
0.050 0.140 clock uncertainty
0.000 0.140 clock reconvergence pessimism
0.009 0.150 library hold time
0.150 data required time
0.150 data required time
0.200 data arrival time
0.050 slack (MET)
```

Setup Slack = 3.234

```
Startpoint: _580_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: out[4] (output port clocked by clk)
Path Group: clk
Path Type: max
Cap Slew Delay Time Description
-----
0.000 0.000 clock clk (rise edge)
0.000 0.000 clock source latency
8.453 0.000 0.000 ^ clk (in)
0.001 0.001 0.001 ^ clkbuf_0_clk/A (BUF_X4)
67.012 0.039 0.053 0.053 ^ clkbuf_0_clk/Z (BUF_X4)
0.039 0.003 0.057 ^ clkbuf_4.15_0_clk/A (BUF_X4)
14.023 0.011 0.032 0.088 ^ clkbuf_4.15_0_clk/Z (BUF_X4)
0.011 0.001 0.089 ^ _580_/CK (DFF_X1)
3.111 0.011 0.093 0.182 ^ _580_/Z (DFF_X1)
0.011 0.000 0.182 ^ 515./A2 (AND2_X1)
2.417 0.010 0.034 0.216 ^ 515./ZN (AND2_X1)
0.010 0.000 0.216 ^ out[4] (out)
0.216 data arrival time
5.000 5.000 clock clk (rise edge)
0.000 5.000 clock network delay (propagated)
-0.050 4.950 clock uncertainty
0.000 4.950 clock reconvergence pessimism
-1.500 3.450 output external delay
3.450 data required time
3.450 data required time
-0.216 data arrival time
3.234 slack (MET)
```

7. Results Post Routing

We have only 16% utilisation of the entire die. Thus, we could change the die size and re-run the tool to get better utilisation.

Total Power consumed: 0.287mW

Both hold and setup slack came out to be positive in the end.

CHANGING THE POSITION OF PINS

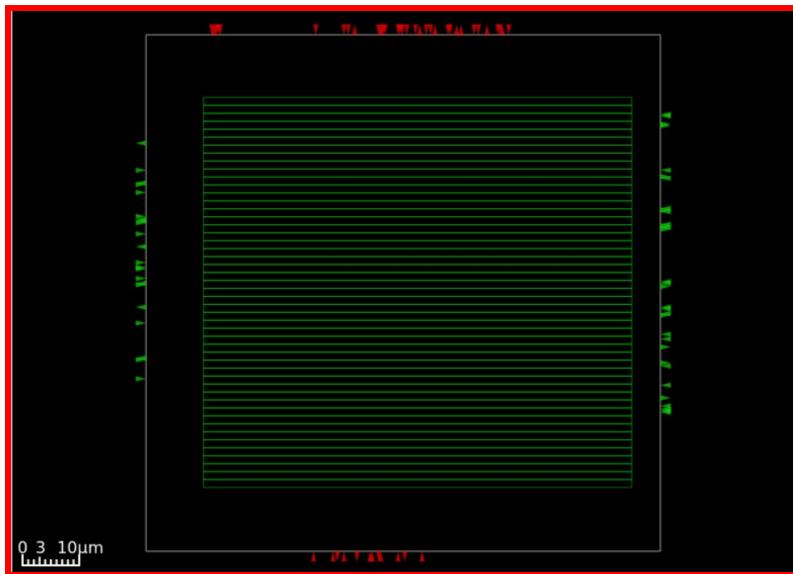
2, 3. Floor Planning + Pin Placement

Command to manually place each and every pin:-

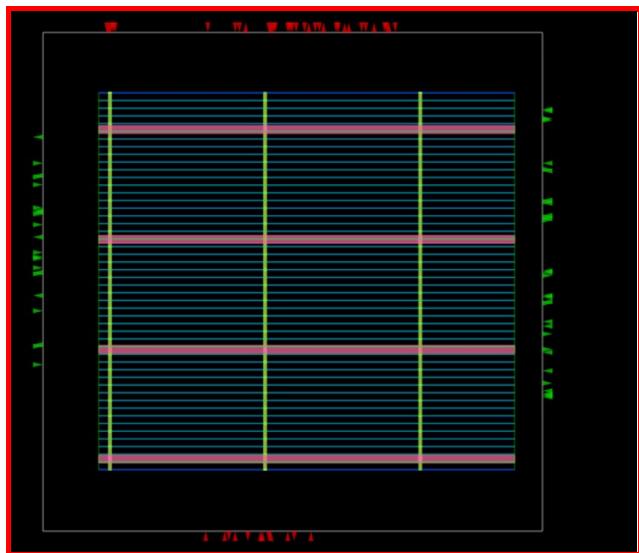
```
→ place_pin -pin_name in1[0] -layer metalx -location {x y} -pin_size {h w}
```

Randomise using a seed value :-

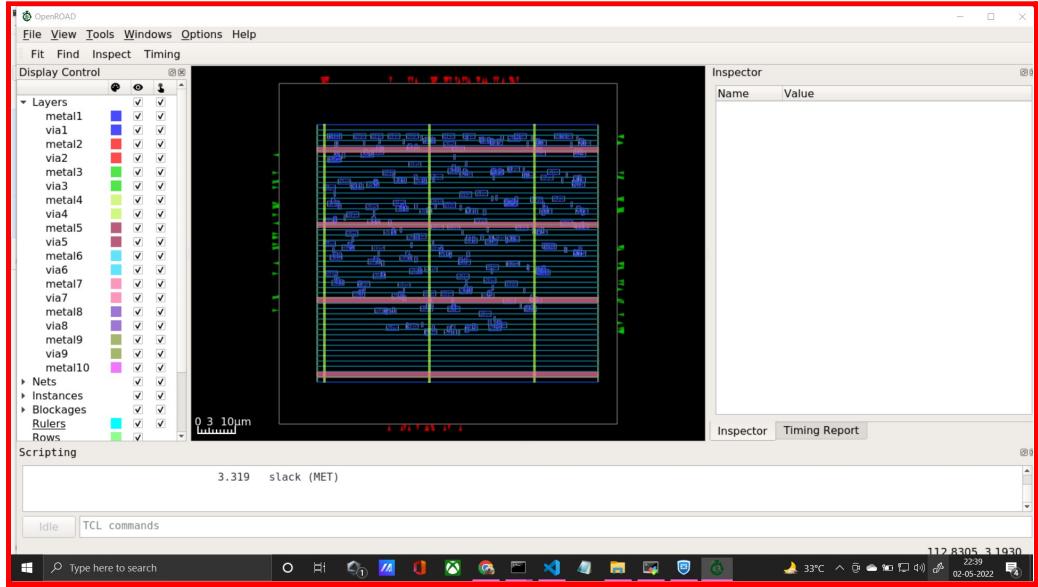
```
→ place_pins -random_seed 2 -hor_layers $io_placer_hor_layer -ver_layers  
$io_placer_ver_la
```



4. Power Planning



5. a) Global Placement



Hold: 0.058

Timing Report for Hold Path					
Startpoint:	.640_ (rising edge-triggered flip-flop clocked by clk)				
Endpoint:	.544_ (rising edge-triggered flip-flop clocked by clk)				
Path Group:	clk				
Path Type:	min				
Cap	Slew	Delay	Time	Description	

0.050	0.000	0.000	clock clk (rise edge)		
	0.050	0.050	clock network delay (ideal)		
0.050	0.000	0.050 ^ .640/_CK (DFF_X1)			
1.859	0.007	0.094	.144 v .640/_0 (DFF_X1)		
	0.007	0.000	.144 v .320/_A (INV_X1)		
1.965	0.007	0.012	.156 ^ .320/_ZN (INV_X1)		
	0.007	0.000	.156 ^ .385/_C1 (A01211_X1)		
1.372	0.007	0.013	.169 v .385/_ZN (A01211_X1)		
	0.007	0.000	.169 v .544/_0 (DFF_X1)		
		0.169	data arrival time		

0.050	0.000	0.000	clock clk (rise edge)		
	0.050	0.050	clock network delay (ideal)		
0.050	0.100	clock uncertainty			
0.000	0.100	clock reconvergence pessimism			
	0.100 ^ .544/_CK (DFF_X1)				
0.011	0.111	library hold time			
	0.111	data required time			

	0.111	data required time			
	-0.169	data arrival time			

	0.058	slack (MET)			

Setup: 3.319

Timing Report for Setup Path					
Setup Path from .586_ to .out[10]					
Startpoint:	.586_ (rising edge-triggered flip-flop clocked by clk)				
Endpoint:	.out[10] (output port clocked by clk)				
Path Group:	clk				
Path Type:	max				
Cap	Slew	Delay	Time	Description	

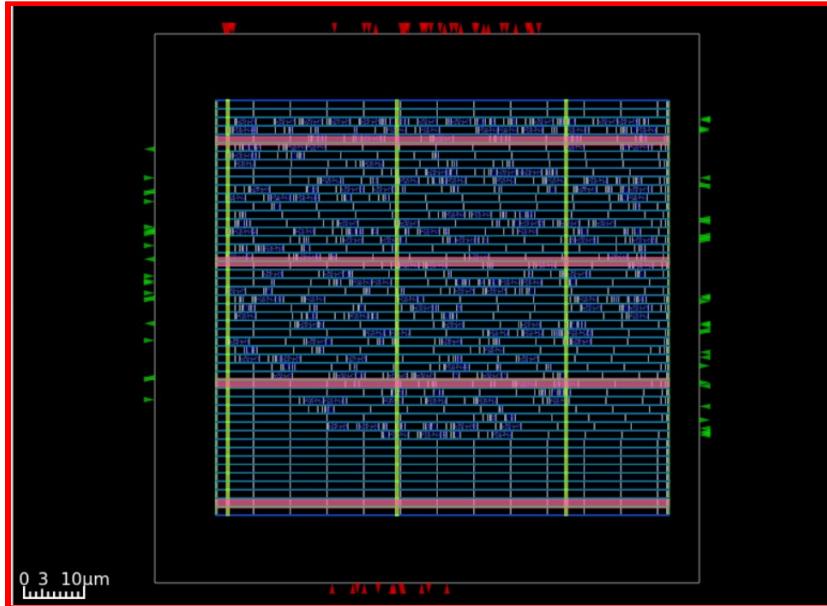
0.050	0.000	0.000	clock clk (rise edge)		
	0.050	0.050	clock network delay (ideal)		
0.050	0.000	0.050 ^ .586/_CK (DFF_X1)			
3.325	0.011	0.103	.153 ^ .586/_0 (DFF_X1)		
	0.011	0.000	.153 ^ .521/_A (AND2_X1)		
0.310	0.006	0.027	.181 ^ .521/_ZN (AND2_X1)		
	0.006	0.000	.181 ^ .out[10] (out)		
		0.181	data arrival time		

0.050	5.000	5.000	clock clk (rise edge)		
	0.050	5.050	clock network delay (ideal)		
-0.050	5.000	clock uncertainty			
0.000	5.000	clock reconvergence pessimism			
-1.500	3.500	output external delay			
	3.500	data required time			

	3.500	data required time			
	-0.181	data arrival time			

	3.319	slack (MET)			

b) Detailed Placement



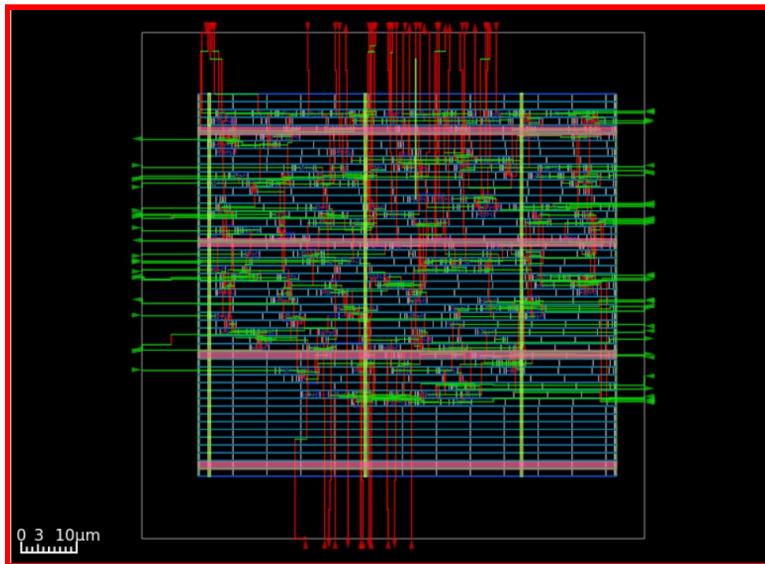
Hold: 0.058

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Setup: 3.319

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6. Routing



Hold: 0.051

Startpoint: _671 (rising edge-triggered flip-flop clocked by clk)				
Endpoint: 575 (rising edge-triggered flip-flop clocked by clk)				
Path Group: clk				
Path Type: min				
Cap	Slew	Delay	Time	Description
		0.000	0.000	clock clk (rise edge)
		0.000	0.000	clock source latency
9.315	0.000	0.001	0.001 ^ clk (in)	
		0.001	0.001 ^ clkbuf_0_0_clk/A (BUF_X4)	
64.245	0.038	0.051	0.052 ^ clkbuf_0_0_clk/Z (BUF_X4)	
		0.038	0.003	clkbuf_4_14_0_clk/A (BUF_X4)
16.866	0.010	0.009	0.055 ^ clkbuf_4_14_0_clk/Z (BUF_X4)	
		0.010	0.009 ^ _671/_CK (DFF_X1)	
1.706	0.006	0.083	0.168 v _671/_Q (DFF_X1)	
		0.006	0.009 ^ _351/_A (INV_X1)	
1.856	0.007	0.007	0.168 v _351/_Z (INV_X1)	
		0.007	0.008 ^ _575/_Z (DFF_X1)	
1.186	0.007	0.014	0.179 v _575/_Z (DFF_X1)	
		0.007	0.008 ^ _447/_ZN (A01211_X1)	
		0.007	0.193 v _575/_D (DFF_X1)	
		0.007	0.193 v _575/_Q (DFF_X1)	
			0.193	data arrival time
			0.000	clock clk (rise edge)
			0.000	clock source latency
9.315	0.000	0.000	0.000 ^ clk (in)	
		0.001	0.001 ^ clkbuf_0_0_clk/A (BUF_X4)	
64.245	0.038	0.051	0.052 ^ clkbuf_0_0_clk/Z (BUF_X4)	
		0.038	0.003	clkbuf_4_15_0_clk/A (BUF_X4)
15.659	0.012	0.032	0.087 ^ clkbuf_4_15_0_clk/Z (BUF_X4)	
		0.012	0.001 ^ _575/_CK (DFF_X1)	
		0.012	0.138	clock uncertainty
		0.009	0.138	clock reconvergence pessimism
		0.004	0.143	library hold time
			0.143	data required time
			-0.143	data required time
			-0.193	data arrival time
			0.051	slack (MET)

Setup: 3.235

Startpoint: 592 (rising edge-triggered flip-flop clocked by clk)				
Endpoint: out[16] (output port clocked by clk)				
Path Group: clk				
Path Type: max				
Cap	Slew	Delay	Time	Description
		0.000	0.000	clock clk (rise edge)
		0.000	0.000	clock source latency
9.315	0.000	0.000	0.000 ^ clk (in)	
		0.001	0.001 ^ clkbuf_0_0_clk/A (BUF_X4)	
64.245	0.038	0.051	0.052 ^ clkbuf_0_0_clk/Z (BUF_X4)	
		0.038	0.002	clkbuf_4_2_0_clk/A (BUF_X4)
14.346	0.011	0.032	0.086 ^ clkbuf_4_2_0_clk/Z (BUF_X4)	
		0.011	0.001 ^ _592/_CK (DFF_X1)	
3.626	0.012	0.094	0.180 ^ _592/_Q (DFF_X1)	
		0.012	0.000 ^ _527/_A2 (AND2_X1)	
2.434	0.010	0.034	0.214 ^ _527/_ZN (AND2_X1)	
		0.010	0.000 ^ out[16] (out)	
			0.215	data arrival time
		5.000	5.000	clock clk (rise edge)
		0.000	5.000	clock network delay (propagated)
		-0.050	4.950	clock uncertainty
		0.000	4.950	clock reconvergence pessimism
		-1.500	3.450	output external delay
			3.450	data required time
		3.450	data required time	
		-0.215	data arrival time	
		3.235	slack (MET)	

Power

```
report_power -corner $power_corner
Group           Internal Power   Switching Power   Leakage Power   Total Power
-----
Sequential      1.34e-04    4.93e-06    1.01e-05    1.49e-04  88.4%
Combinational   9.08e-06    5.20e-06    5.28e-06    1.96e-05  11.6%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00  0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00  0.0%
-----
Total          1.43e-04    1.01e-05    1.54e-05    1.69e-04  100.0%
          84.9%       6.0%       9.1%
```

Area

```
report_floating_nets -verbose
report_design_area
Design area 783 u^2 15% utilization.
```

7. Results Post Routing

We have only 15% utilisation of the entire die. Thus, we could change the die size and re-run the tool to get better utilisation.

Total Power consumed: 0.169mW

Both hold and setup slack came out to be positive in the end.

Analysis

Since, I kept my constraints fairly loose and the uncertainty in the clock was relatively low, my design never had any violations. Both hold and setup slacks were positive in every step of the design flow.

Post routing, we saw a decrease in the slack. This makes sense as when we route, and there are capacitances which come into the picture. We are putting extra metal that has resistance and that comes into consideration too. As we go deeper in the design flow, we come closer to the reality... hence a decrease in setup and hold slack made sense post routing.

Pin placement plays a role in determining the timing, power and area of the overall design. We can clearly see that all the Quality measures vary in the two cases.

Area

In case 2, our pins are placed more densely than in case 1. As a result, the cells could've been placed closer to each other and thus reducing the area of our design from $814\mu^2$ to $783\mu^2$.

Power

The power consumption of the second design came down to 0.169mW from 0.27mW. This result was surprising to me. I expected power to go down since the overall area went down and that meant less routing requirements. But because the pins are more densely located, and majorly these pins are imputed together, the amount of metal needed would've gone down by a greater amount; thus, the power consumption fell by a huge amount.

Timing

The worst path for both hold and setup changed when the pin location was changed. Which is understandable. Since we place the cells according to some logic in placement, we do consider pin location too. Depending on how we place our cells in the design, we end up with different slacks.

However, the overall slack post routing ended up being almost the same for the two cases. It is difficult to comment on, by just looking at the top level of the design. But it is possible to have almost the same slack.

Constraints for negative slack post-placement

```
create_clock -name clk -period 2.0 [get_ports "clk"]
set_propagated_clock [get_clocks "clk"]
set_clock_transition -rise 0.05 [get_clocks "clk"]
set_clock_transition -fall 0.05 [get_clocks "clk"]
set_clock_uncertainty 0.25 [get_clocks "clk"]
set_clock_latency 0.05 [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "rst"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "rst"] -clock [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "in1"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "in1"] -clock [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "in2"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "in2"] -clock [get_clocks "clk"]

set_input_delay -max 0.4 [get_ports "control"] -clock [get_clocks "clk"]
set_input_delay -min 0.2 [get_ports "control"] -clock [get_clocks "clk"]

set_input_transition -max 0.02 [get_ports rst]
set_input_transition -min 0.01 [get_ports rst]

set_input_transition -max 0.02 [get_ports in1]
set_input_transition -min 0.01 [get_ports in1]

set_input_transition -max 0.02 [get_ports in2]
set_input_transition -min 0.01 [get_ports in2]

set_input_transition -max 0.02 [get_ports control]
set_input_transition -min 0.01 [get_ports control]

set_output_delay -max 1.5 [get_ports "out"] -clock [get_clocks "clk"]
set_output_delay -min 0.8 [get_ports "out"] -clock [get_clocks "clk"]

#####
#This constraints file is structured in the similar way, I used for the course group project.
~  
~  
~
```

Post-Global Placement

Hold is negative

```
# checkpoint
set_global_place_def [make_result_file ${design}_${platform}_global_place.def]
write_def $global_place_def
report_checks -path_delay min_max -format full_clock_expanded \
  -fields {input_pin slew capacitance} -digits 3
Startpoint: _640_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _544_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min
Cap Slew Delay Time Description
-----
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.000 0.050 ^ _640/_CK (DFF_X1)
1.859 0.007 0.094 0.144 v _640/_Q (DFF_X1)
0.007 0.000 0.144 v _320/_A (INV_X1)
1.965 0.007 0.012 0.156 ^ _320/_ZN (INV_X1)
0.007 0.000 0.156 ^ _385/_C1 (A01211_X1)
1.372 0.007 0.013 0.169 v _385/_ZN (A01211_X1)
0.007 0.000 0.169 v _544/_D (DFF_X1)
0.169 0.169 v _544 data arrival time

0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.250 0.300 0.300 clock uncertainty
0.000 0.300 0.300 clock reconvergence pessimism
0.300 ^ _544/_CK (DFF_X1)
0.011 0.311 library hold time
0.311 data required time
0.311 data required time
-0.169 data arrival time
-----
-0.142 slack (VIOLATED)
```

```
Startpoint: _586_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: out[10] (output port clocked by clk)
Path Group: clk
Path Type: max
Cap Slew Delay Time Description
-----
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.000 0.050 ^ _586/_CK (DFF_X1)
3.325 0.011 0.103 0.153 ^ _586/_Q (DFF_X1)
0.011 0.000 0.153 ^ _521/_A2 (AND2_X1)
0.310 0.006 0.027 0.181 ^ _521/_ZN (AND2_X1)
0.006 0.000 0.181 ^ out[10] (out)
0.181 data arrival time

0.050 2.000 2.000 clock clk (rise edge)
0.050 2.050 2.050 clock network delay (ideal)
-0.250 1.800 clock uncertainty
0.000 1.800 clock reconvergence pessimism
-1.500 0.300 output external delay
0.300 data required time
0.300 data required time
-0.181 data arrival time
-----
0.119 slack (MET)
```

Post-Detail Placement

Hold is 0

Startpoint: int[10] (input port clocked by clk)					
Endpoint: _618_ (rising edge-triggered flip-flop clocked by clk)					
Path Group: clk					
Path Type: min					
Cap	Slew	Delay	Time	Description	

			0.000	clock clk (rise edge)	
			0.000	clock network delay (propagated)	
			0.200	0.200 ^ input external delay	
1.784	0.010	0.000	0.200	^ int[10] (in)	
			0.000	^ hold1082/A (BUF_X1)	
1.009	0.006	0.020	0.220	^ hold1082/Z (BUF_X1)	
			0.006	^ hold1083/A (BUF_X1)	
0.993	0.006	0.019	0.239	^ hold1083/Z (BUF_X1)	
			0.006	^ hold1084/A (BUF_X1)	
1.353	0.006	0.020	0.259	^ hold1084/Z (BUF_X1)	
			0.006	^ hold1085/A (BUF_X1)	
1.353	0.006	0.020	0.279	^ hold1085/Z (BUF_X1)	
			0.006	^ hold1086/A (BUF_X1)	
1.353	0.006	0.020	0.299	^ hold1086/Z (BUF_X1)	
			0.006	^ hold1087/A (BUF_X1)	
1.030	0.006	0.019	0.318	^ hold1087/Z (BUF_X1)	
			0.006	^ hold1365/A (BUF_X1)	
1.970	0.007	0.021	0.339	^ hold1365/Z (BUF_X1)	
			0.007	^ _618_ /D (DFP_X1)	
			0.339	data arrival time	
			0.339	data required time	

			0.000	clock clk (rise edge)	
			0.000	clock source latency	
8.470	0.000	0.000	0.000	^ clk (in)	
			0.001	0.000 0.000 ^ clkbuf_0_clk/A (BUF_X4)	
65.113	0.039	0.053	0.053	^ clkbuf_0_clk/Z (BUF_X4)	
			0.039	0.000 0.054 ^ clkbuf_4_3_0_clk/A (BUF_X4)	
6.539	0.008	0.027	0.081	^ clkbuf_4_3_0_clk/Z (BUF_X4)	
			0.008	0.000 0.081 ^ _618_ /CK (DFP_X1)	
			0.250	0.331 clock uncertainty	
			0.000	0.331 clock reconvergence pessimism	
			0.008	0.339 library hold time	
			0.339	data required time	

			0.339	data required time	
			-0.339	data arrival time	
			0.000	slack (MET)	

Setup: 0.036

Startpoint: _567_ (rising edge-triggered flip-flop clocked by clk)					
Endpoint: out[23] (output port clocked by clk)					
Path Group: clk					
Path Type: max					
Cap	Slew	Delay	Time	Description	

			0.000	clock clk (rise edge)	
			0.000	clock source latency	
8.470	0.000	0.000	0.000	^ clk (in)	
			0.001	0.000 0.000 ^ clkbuf_0_clk/A (BUF_X4)	
65.113	0.039	0.053	0.053	^ clkbuf_0_clk/Z (BUF_X4)	
			0.039	0.000 0.054 ^ clkbuf_4_2_0_clk/A (BUF_X4)	
13.575	0.011	0.032	0.086	^ clkbuf_4_2_0_clk/Z (BUF_X4)	
			0.011	0.000 0.086 ^ _567_ /CK (DFP_X1)	
2.913	0.011	0.092	0.178	^ _567_ /Q (DFP_X1)	
			0.011	0.000 0.178 ^ _534_ /A1 (AND2_X1)	
3.325	0.012	0.035	0.213	^ _534_ /Z/N (AND2_X1)	
			0.012	0.000 0.214 out[23] (out)	
			0.214	data arrival time	
			2.000	clock clk (rise edge)	
			0.000	2.000 clock network delay (propagated)	
			-0.250	1.750 clock uncertainty	
			0.000	1.750 clock reconvergence pessimism	
			-1.500	0.250 output external delay	
			0.250	data required time	

			0.250	data required time	
			-0.214	data arrival time	
			0.036	slack (MET)	

POST ROUTING

Hold

Path Group: clk				
Path Type: min				
Cap	Slew	Delay	Time	Description
		0.000	0.000	clock clk (rise edge)
		0.000	0.000	clock network delay (propagated)
		0.200	0.200	^ input external delay
2.170	0.010	0.000	0.200	^ inl[23] (in)
	0.010	0.000	0.200	^ hold1088/A (BUF_X1)
1.018	0.006	0.020	0.221	^ hold1088/Z (BUF_X1)
	0.006	0.000	0.221	^ hold1089/A (BUF_X1)
1.018	0.006	0.019	0.239	^ hold1089/Z (BUF_X1)
	0.006	0.000	0.239	^ hold1090/A (BUF_X1)
1.164	0.006	0.019	0.258	^ hold1090/Z (BUF_X1)
	0.006	0.000	0.258	^ hold1091/A (BUF_X1)
1.588	0.007	0.020	0.279	^ hold1091/Z (BUF_X1)
	0.007	0.000	0.279	^ hold1092/A (BUF_X1)
1.123	0.006	0.019	0.298	^ hold1092/Z (BUF_X1)
	0.006	0.000	0.298	^ hold1093/A (BUF_X1)
1.018	0.006	0.019	0.317	^ hold1093/Z (BUF_X1)
	0.006	0.000	0.317	^ hold1366/A (BUF_X1)
1.792	0.007	0.021	0.338	^ hold1366/Z (BUF_X1)
	0.007	0.000	0.338	^ _631_/_D (DFF_X1)
			0.338	data arrival time
		0.000	0.000	clock clk (rise edge)
		0.000	0.000	clock source latency
9.312	0.000	0.000	0.000	^ clk (in)
	0.001	0.001	0.001	^ clkbuf_0_clk/A (BUF_X4)
65.256	0.038	0.052	0.052	^ clkbuf_0_clk/Z (BUF_X4)
	0.038	0.002	0.054	^ clkbuf_4_3_0_clk/A (BUF_X4)
6.649	0.008	0.027	0.082	^ clkbuf_4_3_0_clk/Z (BUF_X4)
	0.008	0.000	0.082	^ _631_/_CK (DFF_X1)
		0.250	0.332	clock uncertainty
		0.000	0.332	clock reconvergence pessimism
		0.007	0.339	library hold time
			0.339	data required time
		0.339	data required time	
		-0.338	data arrival time	
		-0.001	slack (VIOLATED)	

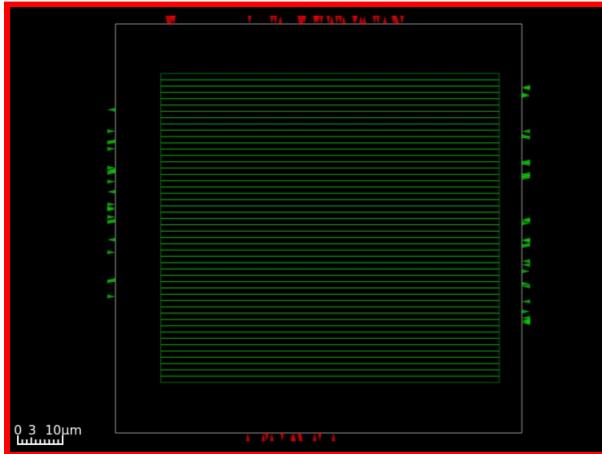
Setup

Startpoint: _596_ (rising edge-triggered flip-flop clocked by clk)				
Endpoint: out[20] (output port clocked by clk)				
Path Group: clk				
Path Type: max				
Cap	Slew	Delay	Time	Description
		0.000	0.000	clock clk (rise edge)
		0.000	0.000	clock source latency
9.312	0.000	0.000	0.000	^ clk (in)
	0.001	0.001	0.001	^ clkbuf_0_clk/A (BUF_X4)
65.256	0.038	0.052	0.052	^ clkbuf_0_clk/Z (BUF_X4)
	0.038	0.003	0.055	^ clkbuf_4_15_0_clk/A (BUF_X4)
16.622	0.012	0.033	0.088	^ clkbuf_4_15_0_clk/Z (BUF_X4)
	0.012	0.002	0.090	^ _596_/_CK (DFF_X1)
3.236	0.011	0.094	0.184	^ _596_/_Q (DFF_X1)
	0.011	0.000	0.184	^ _531_/_A2 (AND2_X1)
1.833	0.009	0.032	0.216	^ _531_/_ZN (AND2_X1)
	0.009	0.000	0.216	^ out[20] (out)
			0.216	data arrival time
		2.000	2.000	clock clk (rise edge)
		0.000	2.000	clock network delay (propagated)
	-0.250	1.750	clock uncertainty	
	0.000	1.750	clock reconvergence pessimism	
	-1.500	0.250	output external delay	
		0.250	data required time	
		-0.216	data arrival time	
		0.034	slack (MET)	

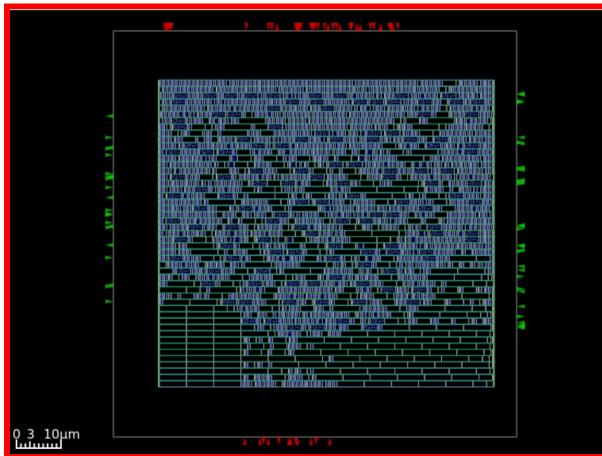
Power and Area

```
report_power -corner $power_corner
Group          Internal Power   Switching Power   Leakage Power   Total Power
-----
Sequential      3.19e-04        1.04e-05       1.01e-05       3.40e-04    36.1%
Combinational   3.44e-04        2.22e-04       3.62e-05       6.03e-04    63.9%
Macro          0.00e+00        0.00e+00       0.00e+00       0.00e+00    0.0%
Pad            0.00e+00        0.00e+00       0.00e+00       0.00e+00    0.0%
-----
Total           6.63e-04        2.33e-04       4.63e-05       9.43e-04    100.0%
          70.4%          24.7%          4.9%
report_floating_nets -verbose
report_design_area
Design area 1911  $\mu\text{m}^2$  37% utilization.
```

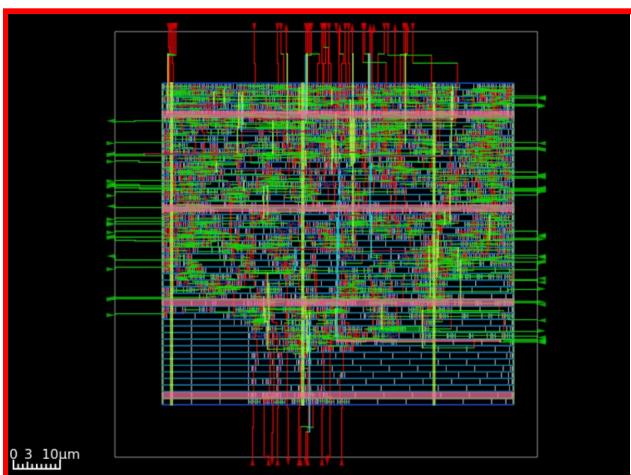
Floor Planning + Pin Placement



Post Detailed Placement



Post Routing



For a different Pin Placement

Post placement (Global)

Hold: Negative

```
set_global_place_def [make_result_file ${design}_${platform}_global_place.def]
write_def $global_place_def
report_checks -path_delay min_max -format full_clock_expanded \
  -fields {input_pin slew capacitance} -digits 3
Startpoint: _640_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _544_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Cap Slew Delay Time Description
-----
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.000 0.050 ^ _640/_CK (DFF_X1)
1.859 0.007 0.094 0.144 v _640/_Q (DFF_X1)
0.007 0.000 0.144 v _320/_A (INV_X1)
1.965 0.007 0.012 0.156 ^ _320/_ZN (INV_X1)
0.007 0.000 0.156 ^ _385/_C1 (AOI211_X1)
1.372 0.007 0.013 0.169 v _385/_ZN (AOI211_X1)
0.007 0.000 0.169 v _544/_D (DFF_X1)
0.007 0.000 0.169 v _544/_D (DFF_X1)
0.000 0.000 0.169 data arrival time

0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.250 0.300 0.300 clock uncertainty
0.000 0.300 0.300 clock reconvergence pessimism
0.000 0.300 ^ _544/_CK (DFF_X1)
0.011 0.311 0.311 library hold time
0.011 0.311 0.311 data required time

0.311 0.311 data required time
-0.169 -0.169 data arrival time

-0.142 slack (VIOLATED)
```

setup

```
Startpoint: _586_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: out[10] (output port clocked by clk)
Path Group: clk
Path Type: max

Cap Slew Delay Time Description
-----
0.050 0.000 0.000 clock clk (rise edge)
0.050 0.050 0.050 clock network delay (ideal)
0.050 0.000 0.050 ^ _586/_CK (DFF_X1)
3.325 0.011 0.103 0.153 ^ _586/_Q (DFF_X1)
0.011 0.000 0.153 ^ _521/_A2 (AND2_X1)
0.310 0.006 0.027 0.181 ^ _521/_ZN (AND2_X1)
0.006 0.000 0.181 ^ out[10] (out)
0.006 0.000 0.181 data arrival time

0.050 2.000 2.000 clock clk (rise edge)
0.050 2.050 2.050 clock network delay (ideal)
-0.250 1.800 1.800 clock uncertainty
0.000 1.800 1.800 clock reconvergence pessimism
-1.500 0.300 0.300 output external delay
0.300 0.300 data required time

0.300 0.300 data required time
-0.181 -0.181 data arrival time

0.119 0.119 slack (MET)
```

Post Placement (Detailed)

Hold: no longer negative

```
check_placement -verbose
report_checks -path delay min_max -format full_clock_expanded \
  -fields {input_pin slew capacitance} -digits 3
Startpoint: in2[30] (input port clocked by clk)
Endpoint: _670_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Cap Slew Delay Time Description
-----+
0.000 0.000 clock clk (rise edge)
0.000 0.000 clock network delay (propagated)
0.200 0.200 ^ input external delay
1.869 0.010 0.000 0.200 ^ in2[30] (in)
0.010 0.000 0.200 ^ hold1/A (BUF_X1)
1.006 0.006 0.020 0.220 ^ hold1/Z (BUF_X1)
0.006 0.000 0.220 ^ hold2/A (BUF_X1)
1.006 0.006 0.019 0.239 ^ hold2/Z (BUF_X1)
0.006 0.000 0.239 ^ hold3/A (BUF_X1)
1.006 0.006 0.019 0.258 ^ hold3/Z (BUF_X1)
0.006 0.000 0.258 ^ hold4/A (BUF_X1)
1.006 0.006 0.019 0.277 ^ hold4/Z (BUF_X1)
0.006 0.000 0.277 ^ hold5/A (BUF_X1)
1.006 0.006 0.019 0.295 ^ hold5/Z (BUF_X1)
0.006 0.000 0.295 ^ hold6/A (BUF_X1)
1.006 0.006 0.019 0.314 ^ hold6/Z (BUF_X1)
0.006 0.000 0.314 ^ hold7/A (BUF_X1)
1.030 0.006 0.019 0.333 ^ hold7/Z (BUF_X1)
0.006 0.000 0.333 ^ hold1352/A (BUF_X1)
1.263 0.006 0.019 0.352 ^ hold1352/Z (BUF_X1)
0.006 0.000 0.352 ^ _670_/_D (DFF_X1)
0.006 0.000 0.352 ^ _670_/_D (DFF_X1)
0.000 0.000 data arrival time

0.000 0.000 clock clk (rise edge)
0.000 0.000 clock source latency
8.755 0.000 0.000 0.000 ^ clk (in)
0.001 0.000 0.000 ^ clkbuf_0_clk/A (BUF_X4)
67.544 0.040 0.054 0.055 ^ clkbuf_0_clk/Z (BUF_X4)
0.040 0.001 0.001 0.055 ^ clkbuf_4_10_0_clk/A (BUF_X4)
0.040 0.001 0.025 0.055 ^ clkbuf_4_10_0_clk/Z (BUF_X4)
15.981 0.012 0.033 0.089 ^ clkbuf_4_10_0_clk/A (BUF_X4)
0.012 0.033 0.089 ^ clkbuf_4_10_0_clk/Z (BUF_X4)
0.012 0.000 0.089 ^ _670_/_CK (DFF_X1)
0.012 0.000 0.089 ^ _670_/_CK (DFF_X1)
0.250 0.339 ^ clock uncertainty
0.000 0.339 ^ clock reconvergence pessimism
0.008 0.348 library hold time
0.348 data required time
-----+
0.348 data required time
-0.352 data arrival time
-----+
0.005 slack (MET)
```

```
0.000 0.000 clock clk (rise edge)
0.000 0.000 clock source latency
8.755 0.000 0.000 0.000 ^ clk (in)
0.001 0.000 0.000 ^ clkbuf_0_clk/A (BUF_X4)
67.544 0.040 0.054 0.055 ^ clkbuf_0_clk/Z (BUF_X4)
0.040 0.001 0.001 0.055 ^ clkbuf_4_10_0_clk/A (BUF_X4)
0.040 0.001 0.025 0.055 ^ clkbuf_4_10_0_clk/Z (BUF_X4)
15.981 0.012 0.033 0.089 ^ clkbuf_4_10_0_clk/A (BUF_X4)
0.012 0.033 0.089 ^ clkbuf_4_10_0_clk/Z (BUF_X4)
0.012 0.000 0.089 ^ _670_/_CK (DFF_X1)
0.012 0.000 0.089 ^ _670_/_CK (DFF_X1)
0.250 0.339 ^ clock uncertainty
0.000 0.339 ^ clock reconvergence pessimism
0.008 0.348 library hold time
0.348 data required time
-----+
0.348 data required time
-0.352 data arrival time
-----+
0.005 slack (MET)
```

Setup

```
Startpoint: _572_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: out[28] (output port clocked by clk)
Path Group: clk
Path Type: max

Cap Slew Delay Time Description
-----+
0.000 0.000 clock clk (rise edge)
0.000 0.000 clock source latency
8.755 0.000 0.000 0.000 ^ clk (in)
0.001 0.000 0.000 ^ clkbuf_0_clk/A (BUF_X4)
67.544 0.040 0.054 0.055 ^ clkbuf_0_clk/Z (BUF_X4)
0.040 0.001 0.001 0.055 ^ clkbuf_4_2_0_clk/A (BUF_X4)
11.942 0.010 0.031 0.086 ^ clkbuf_4_2_0_clk/Z (BUF_X4)
0.010 0.000 0.087 ^ clkbuf_4_2_0_clk/A (BUF_X4)
0.014 0.096 0.182 ^ _572_/_Q (DFF_X1)
0.014 0.000 0.182 ^ _572_/_Q (DFF_X1)
4.054 0.014 0.096 0.182 ^ _572_/_Q (DFF_X1)
0.014 0.000 0.182 ^ _539_/_A (AND2_X1)
1.748 0.009 0.032 0.215 ^ _539_/_Z (AND2_X1)
0.009 0.000 0.215 ^ out[28] (out)
0.009 0.000 0.215 data arrival time

2.000 2.000 clock clk (rise edge)
0.000 2.000 clock network delay (propagated)
-0.250 1.750 clock uncertainty
0.000 1.750 clock reconvergence pessimism
-1.500 0.250 output external delay
0.250 data required time
-----+
0.250 data required time
-0.215 data arrival time
-----+
0.035 slack (MET)
```

Post Routing

Hold not violated for this pin placement

Endpoint: _631_ (rising edge-triggered flip-flop clocked by clk)					
Path Group: clk					
Path Type: min					
Cap	Slew	Delay	Time	Description	
		0.000	0.000	clock clk (rise edge)	
		0.000	0.000	clock network delay (propagated)	
		0.200	0.200	^ input external delay	
1.737	0.010	0.000	0.200	^ in1[23] (in)	
1.156	0.006	0.000	0.200	^ hold57/A (BUF_X1)	
1.156	0.006	0.021	0.221	^ hold57/Z (BUF_X1)	
1.156	0.006	0.000	0.221	^ hold58/A (BUF_X1)	
1.212	0.006	0.019	0.240	^ hold58/Z (BUF_X1)	
1.188	0.006	0.000	0.240	^ hold59/A (BUF_X1)	
1.188	0.006	0.019	0.240	^ hold59/Z (BUF_X1)	
1.167	0.006	0.000	0.260	^ hold60/A (BUF_X1)	
1.167	0.006	0.010	0.270	^ hold60/Z (BUF_X1)	
1.167	0.006	0.000	0.270	^ hold61/A (BUF_X1)	
1.196	0.006	0.019	0.298	^ hold61/Z (BUF_X1)	
1.196	0.006	0.000	0.298	^ hold62/A (BUF_X1)	
1.276	0.006	0.020	0.318	^ hold62/Z (BUF_X1)	
1.080	0.006	0.000	0.318	^ hold63/A (BUF_X1)	
1.080	0.006	0.019	0.337	^ hold63/Z (BUF_X1)	
1.295	0.006	0.000	0.337	^ hold1357/A (BUF_X1)	
1.295	0.006	0.020	0.356	^ hold1357/Z (BUF_X1)	
1.295	0.006	0.000	0.356	^ _631_D (DFF_X1)	
1.295	0.006	0.000	0.356	data arrival time	
		0.000	0.000	clock clk (rise edge)	
		0.000	0.000	clock source latency	
8.480	0.000	0.000	0.000	^ clk (in)	
8.480	0.000	0.001	0.001	^ clkbuf_0_clk/A (BUF_X4)	
67.218	0.039	0.053	0.053	^ clkbuf_0_clk/Z (BUF_X4)	
67.218	0.039	0.053	0.053	^ clkbuf_0_clk/A (BUF_X4)	
67.218	0.039	0.053	0.053	^ clkbuf_0_clk/Z (BUF_X4)	
15.751	0.012	0.033	0.033	0.057 ^ clkbuf_4_5_0_clk/A (BUF_X4)	
15.751	0.012	0.001	0.091	0.057 ^ clkbuf_4_5_0_clk/Z (BUF_X4)	
15.751	0.012	0.001	0.091	^ _631_/_CK (DFF_X1)	
15.751	0.012	0.001	0.091	0.250 clock uncertainty	
15.751	0.012	0.001	0.091	0.000 0.341 clock reconvergence pessimism	
15.751	0.012	0.001	0.091	0.008 0.349 library hold time	
15.751	0.012	0.001	0.091	0.349 data required time	
		0.349	0.349	library hold time	
		-0.356	-0.356	data arrival time	
		0.007	0.007	slack (MET)	

Setup

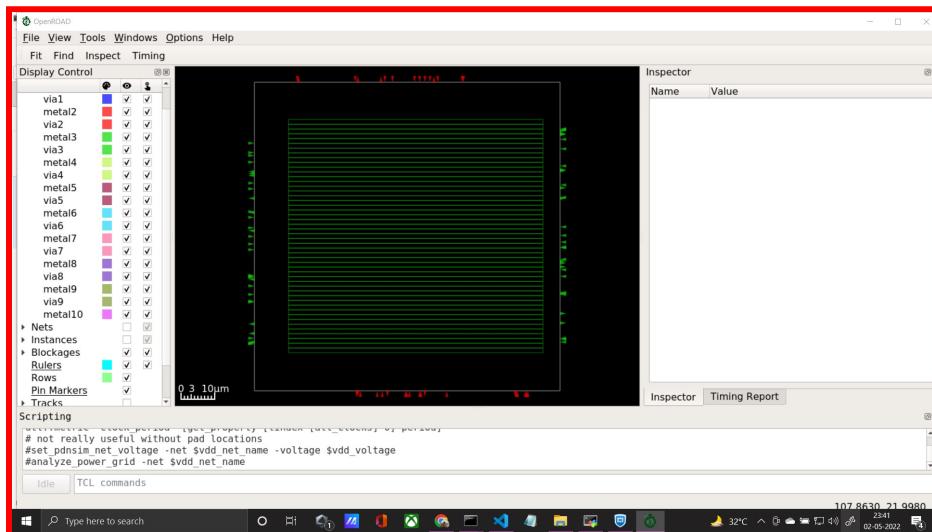
Startpoint: _580_ (rising edge-triggered flip-flop clocked by clk)					
Endpoint: out[4] (output port clocked by clk)					
Path Group: clk					
Path Type: max					
Cap	Slew	Delay	Time	Description	
		0.000	0.000	clock clk (rise edge)	
		0.000	0.000	clock source latency	
8.480	0.000	0.000	0.000	^ clk (in)	
8.480	0.001	0.001	0.001	^ clkbuf_0_clk/A (BUF_X4)	
67.218	0.039	0.053	0.053	^ clkbuf_0_clk/Z (BUF_X4)	
67.218	0.039	0.053	0.053	^ clkbuf_0_clk/A (BUF_X4)	
67.218	0.039	0.053	0.053	^ clkbuf_0_clk/Z (BUF_X4)	
14.578	0.011	0.032	0.089	0.057 ^ clkbuf_4_15_0_clk/A (BUF_X4)	
14.578	0.011	0.001	0.090	0.057 ^ clkbuf_4_15_0_clk/Z (BUF_X4)	
14.578	0.011	0.001	0.090	^ _580_/_CK (DFF_X1)	
3.372	0.011	0.093	0.183	0.000 -0.250 clock uncertainty	
3.372	0.011	0.000	0.184	0.000 -0.250 clock reconvergence pessimism	
2.949	0.011	0.035	0.219	0.000 -0.250 output external delay	
2.949	0.011	0.000	0.219	0.000 -0.250 data required time	
		2.000	2.000	clock clk (rise edge)	
		0.000	2.000	clock network delay (propagated)	
		-0.250	1.750	clock uncertainty	
		0.000	1.750	clock reconvergence pessimism	
		-1.500	0.250	output external delay	
		0.250	0.250	data required time	
		0.250	0.250	data required time	
		-0.219	0.219	data arrival time	
		0.031	0.031	slack (MET)	

Power and Area

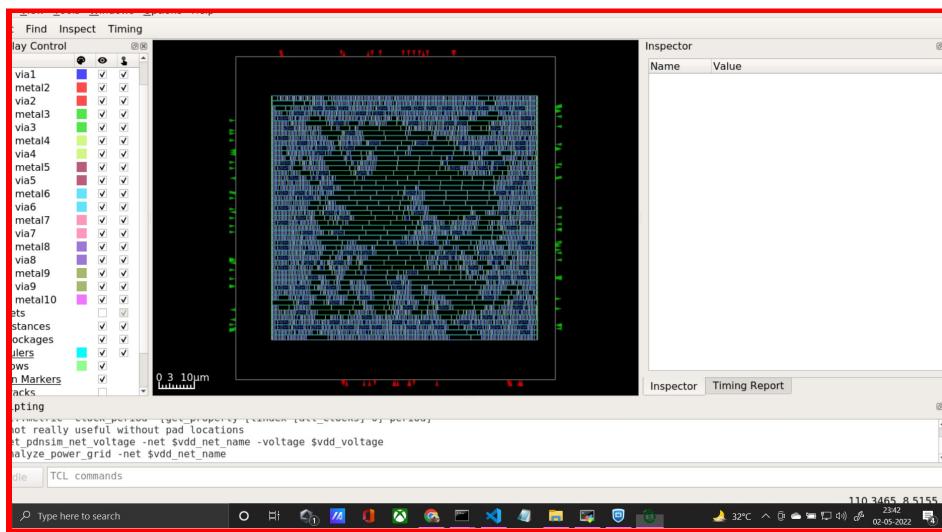
```
report_power -corner $power_corner
Group           Internal Power   Switching Power   Leakage Power   Total Power
-----
Sequential      3.19e-04    1.11e-05    1.01e-05    3.41e-04    35.9%
Combinational   3.44e-04    2.27e-04    3.62e-05    6.08e-04    64.1%
Macro          0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
Pad            0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.0%
-----
Total          6.64e-04    2.38e-04    4.63e-05    9.49e-04   100.0%
70.0%          25.1%        4.9%
```

report_floating_nets -verbose
 report_design_area
 Design area 1911 μm^2 37% utilization.

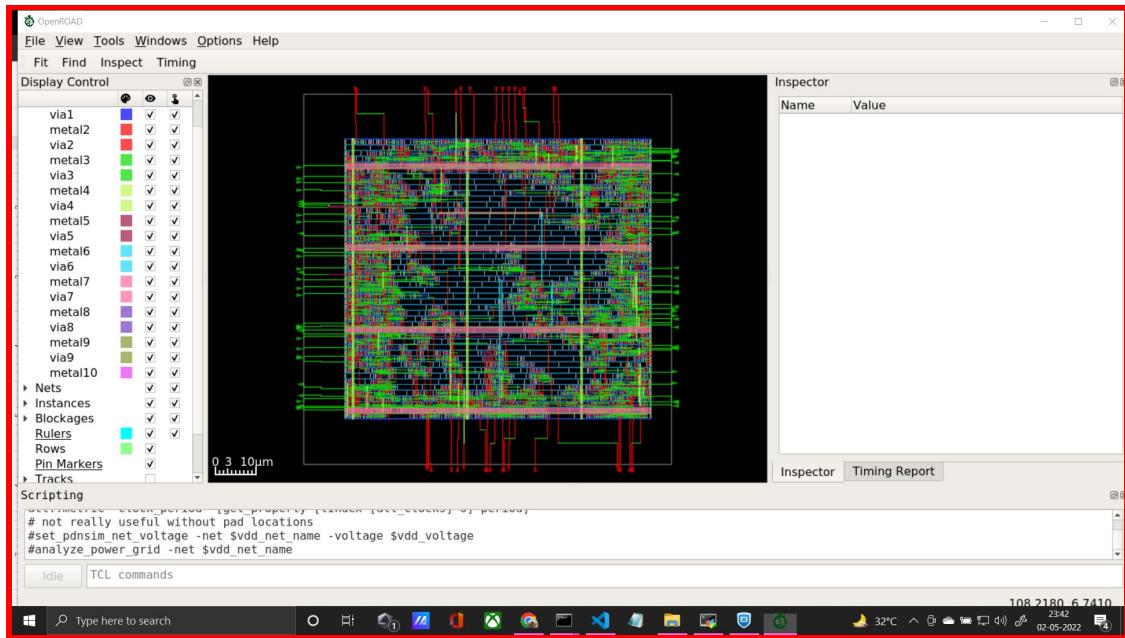
Floor Planning + Pins



Detailed Placement



Post Routing



Analysis

Post routing, we saw a decrease in the slack. This makes sense as when we route, and there are capacitances which come into the picture. We are putting extra metal that has resistance and that comes into consideration too. As we go deeper in the design flow, we come closer to the reality... hence a decrease in setup and hold slack made sense post routing.

Pin placement plays a role in determining the timing, power and area of the overall design. We can clearly see that all the Quality measures vary in the two cases.

Area

No change

Power

Increased by a very small amount.

Timing

The worst path for both hold and setup changed when the pin location was changed. Which is understandable. Since we place the cells according to some logic in placement, we do consider pin location too. Depending on how we place our cells in the design, we end up with different slacks.

The slack in both cases post placement was negative for hold. In design 1, this slack never got positive and remained negative till the end of routing. However, for pin configuration of design 2, this slack actually changed to positive. Thus showing us pin placement can affect the hold slack of our system.

Resources

[**https://github.com/The-OpenROAD-Project/OpenROAD**](https://github.com/The-OpenROAD-Project/OpenROAD)

Given in Ass8 pdf:

Website:

[**https://theopenroadproject.org/**](https://theopenroadproject.org/)

OpenRoad Community:

[**https://gitter.im/The-OpenROAD-Project/community**](https://gitter.im/The-OpenROAD-Project/community)