



**DEPARTMENT OF COMPUTER ENGINEERING**  
**UNIT TEST-II**

**Class: SE**

**Semester: III**

**Subject: DL&COA**

**Date: 19/10/2022**

**Time: 2:30 - 4:00 pm**

**Max marks: 40**

**Note the following instructions**

1. Attempt all questions (Q.1, Q.2, Q.3)
2. Draw neat diagrams wherever necessary.
3. Write everything in ink (no pencil) only.
4. Assume data, if missing, with justification.

Q.1	Attempt any two			
(a)	Describe hardwire control unit and specify its advantages.	[5]	CO4	L2
(b)	Explain a micro-program for fetch routine of instruction cycle	[5]	CO4	L2
(c)	Compare Hardwired and microprogrammed control unit	[5]	CO4	L2
(d)	Explain different techniques for design of control unit of computer	[5]	CO4	L2
Q.2(a)	Consider a direct mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find-  1. Size of main memory, 2. Tag directory size	[10]	CO5	L3
	OR			
Q.2(a)	Consider a fully associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-  1. Number of bits in tag, 2. Tag directory size	[10]	CO5	L3
Q.2(b)	Determine the characteristics of memory.	[5]	CO5	L2
	OR			
Q.2(b)	Show the memory hierarchy in computer system.	[5]	CO5	L2
Q.3 (a)	Illustrate Flynn's classification.	[10]	CO6	L2
	OR			
Q.3 (b)	Illustrate various types of pipeline Hazards.	[10]	CO6	L2
Q.3 (c)	The microprocessor has integer and floating-point instructions. The floating-point instructions are enhanced and 3 times faster than before and integer instructions are unenhanced. If there are 20% of floating instructions in the program then find the overall speedup.	[5]	CO6	L3
	OR			
Q.3 (d)	A program having 10 instructions is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1ns. Calculate the time required to execute the program on non-pipeline and pipeline processor and calculate speed-up.	[5]	CO6	L3

